Characterization of Zynq-Based Data Acquisition Architecture for the 129,024-Channel UHR PET Scanner Dedicated to Human Brain Imaging

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The UHR Brain PET Scanner DAQ

The Ultra-High Resolution (UHR) positron emission tomography (PET) scanner is the latest LabPET II-based device being designed at Université de Sherbrooke for brain imaging. This new scanner uses the already established LabPET II technology capable of submillimeter spatial resolution in preclinical imaging.

Ultra-High Resolution Brain PET Scanner

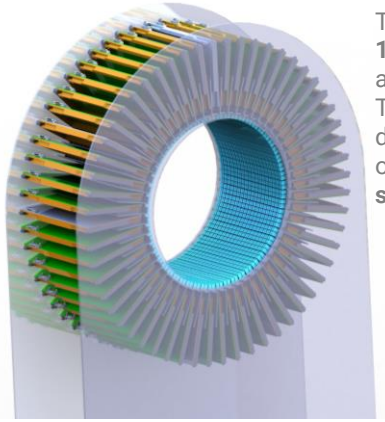

Fig. 1: 3D Render of the UHR brain PET Scanner

The UHR brain PET scanner combines **1,008 LabPET II detection modules** for a total of **129,024 individual channels**. The modules form a tube with a diameter of 390 mm and an axial length of 235 mm. This scanner can achieve a **spatial resolution of 1.3 mm**.

The UHR should handle a maximum count rate of **1,740 events per second per channel (~15 Gb/s)** during calibration procedures and **440 events per second per channel (~3.6 Gb/s)** during regular operation with an activity of 400 MBq inside the boar.

LabPET II Detection Module

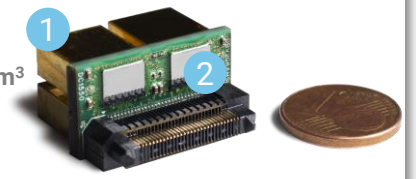

Fig. 2: 128 channel LabPET II detection module.

1. 4 x 8 array of **1.12 x 1.12 x 12 mm³** LYSO scintillators **individually coupled** to a monolithic avalanche photodiode.
2. **64-channel 180 nm CMOS** custom readout ASIC with time-over-threshold digitization for energy measurement and **312.5 ps TDC** for events timestamping. This ASIC can handle up to **4000 events per channel per second** and send them over a single **LVDS line at 100 Mb/s**.

Data Acquisition Proof of Concept

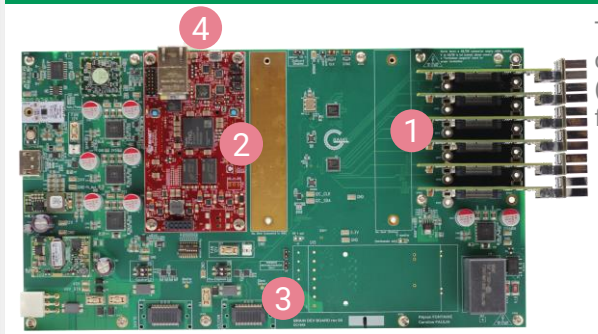

Fig. 4: BrainDev PCB: Proof of concept for the UHR data acquisition system based on a Xilinx Zynq-7020 and containing 12 LabPET II ASIC.

To validate the concept and begin the firmware development of the UHR DAQ, the BrainDEV (Fig. 4) PCB includes a reduced version of all the features present in the UHR DAQ.

1. **6 LabPET II** detection modules
2. Avnet Microzed with **a Zynq 7020**
3. **Synchronization** port for coincidence acquisitions.
4. **Gigabit Ethernet** for data recording on a **network file system** NFSv4.

Firmware architecture

1. Events from the ASIC are deserialized inside the PL. The data are then corrected and sent to the **Xilinx DMA engine** through **AXI-Stream**.
2. The DMA engine store the data inside a ring buffer under the direction of a **custom kernel driver** based on **Linux DMA API.**
3. The User-Space application configures and monitors the peripherals of the DAQ including the LP2 ASICs through the ARM **interfaces** and **AXI-lite**.
4. The data is transferred to the user-space using **mmap** and stored on the acquisition computer using **NFSv4**.

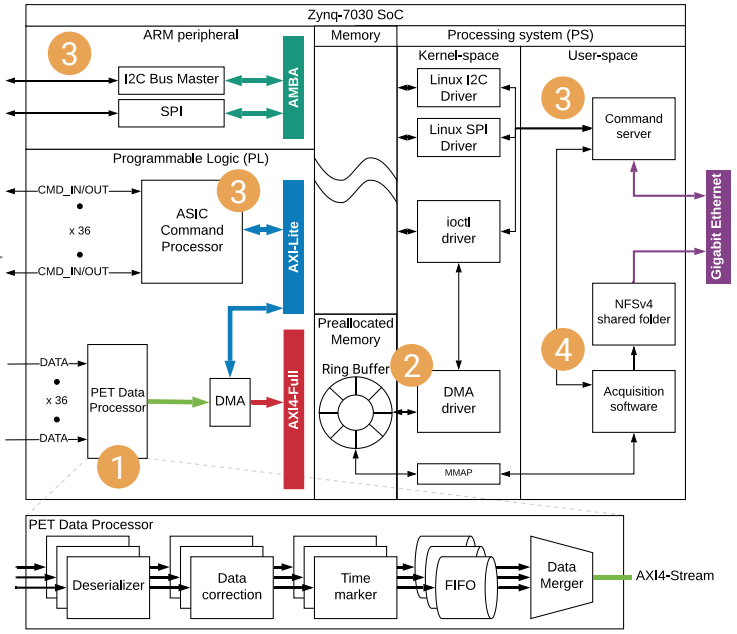

Fig. 5: Architecture of the embedded software for the UHR DAQ.

Results

Using **iperf 3** the data rate between the DAQ and the acquisition computer was established at **~600 Mb/s**.

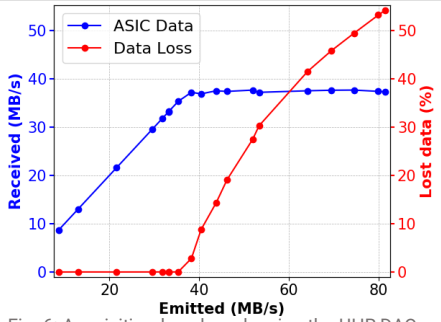

Fig. 6: Acquisition benchmark using the UHR DAQ.

The data rate from the ASIC to the acquisition computer was measured at **283 Mb/s.**

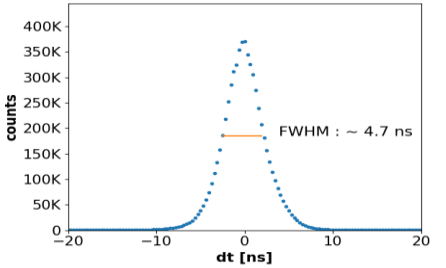

Fig. 7: Time resolution of two BrainDev in coincidence.

The time resolution of 2 BrainDEV in coincidence with one detector module on each board was measured **at 4.7 ns FWHM.**