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Redesign of the ATLAS Tile Calorimeter link Daughterboard for the HL-LHC

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The Phase-2 ATLAS upgrade for the High Luminosity Large Hadron Collider (HL-LHC) has motivated progressive redesigns of the ATLAS Tile Calorimeter (TileCal) read-out link and control board (Daughterboard). The Daughterboard (DB) communicates with the off-detector electronics via two 4.6 Gbps downlinks and two pairs of 9.6 Gbps uplinks. Configuration commands and LHC timing is received through the downlinks by two CERN radiation hard GBTx ASICs and propagated through Ultrascale+ FPGAs to the front-end. Simultaneously, the FPGAs send continuous high-speed readout of digitized PMT samples, slow control and monitoring data through the uplink. The design minimizes single points of failure and reduces sensitivity to SEUs and radiation damage by employing a double-redundant scheme, using Triple Mode Redundancy (TMR) and Xilinx Soft Error Mitigation (SEM) in the FPGAs, adopting Cyclic Redundancy Check (CRC) error verification in the uplinks and Forward Error Correction (FEC) in the downlinks. We present a DB redesign that brings an enhanced timing scheme, and improved radiation tolerance by mitigating Single Event Latch-up (SEL) induced errors and implementing a more robust power-up and current monitoring scheme.

Minioral

Yes

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No

Are you a student?

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