Redesign of the ATLAS Tile Calorimeter Link Daughterboard for the HL-LHC.

22nd IEEE Real Time Conference

The **HL-LHC** and the **ATLAS** Hadronic **Tile Calorimeter (TileCal).**

TileCal is a sampling calorimeter composed of plastic scintillator tiles as active material interleaved with steel plates as absorber. The detector is divided in four cylindrical barrels composed of 64 wedge-shaped modules each (Figure 1). The scintillators in each module are grouped in pseudo-projective cells. Light from two sides of a cell is collected by wavelength shifting fibers and read out by two photomultiplier tubes (PMTs).
The HL-LHC will have an instantaneous luminosity of 5 times the LHC nominal design value. The present TileCal read-out electronics will be incapable of dealing with the higher radiation levels and increased rates of pileup. R&D is ongoing aimed to replace a TileCal electronics with a improved design that will provide continuous digital read-out of all TileCal with lower electronic noise and better timing stability, therefore better energy resolution and less sensitivity to out-of-time pileup [1].

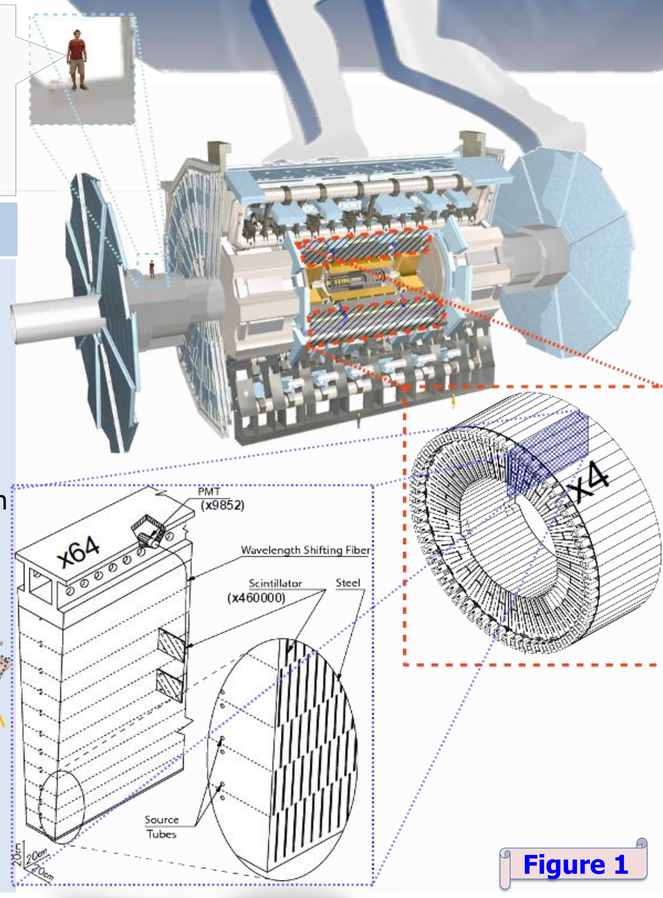

Figure 1

The **TileCal read-out system** for the **HL-LHC**.

The **TileCal read-out system** for the **HL-LHC** [1] consists of two sections: **on-detector and off-detector electronics.** The **on-detector** system (Figure 2) will digitize two gains of the shaped analogue signal from each TileCal PMT at **40 MHz**. The mechanics design is modularized in **896 Minidrawers (MDs),** each **MD** (Figure 3) serves up to **12 channels** by means of:

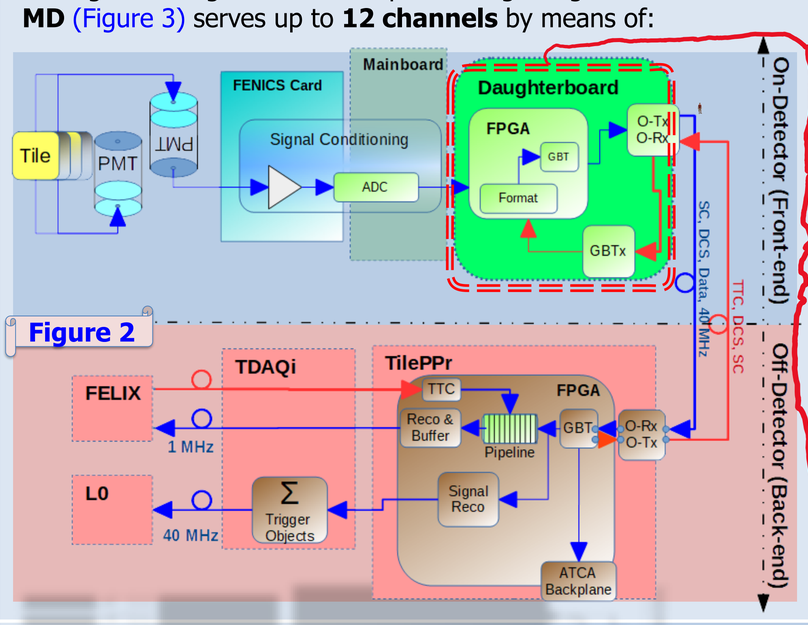

Figure 2

- **12 Photomultiplier (PMTs)** to turn light pulses into electric signals,
- **12 Front-End Boards (FEBs)** to shape and condition the PMT signals,
- **a Mainboard (MB)** to digitize the **two gains** of each shaped PMT signal with a gain ratio of 1:32,
- **a Daughterboard (DB)** (Figure 4) to distribute **LHC synchronized timing**, configuration commands and control signals to the front-end, and to **continuously transmit** the digital data from all the MB channels to the off-detector systems via multi-Gbps optical links.

The data is sent to the **off-detector** system (Figure 2) to be stored in pipelines, reconstructed and triggered-out by:

- **Tile Preprocessors (TilePPr)**
- **Trigger and DAQ interface (TDAQi)**,
- the ATLAS **Front-End Link eXchange** system **(FELIX)**

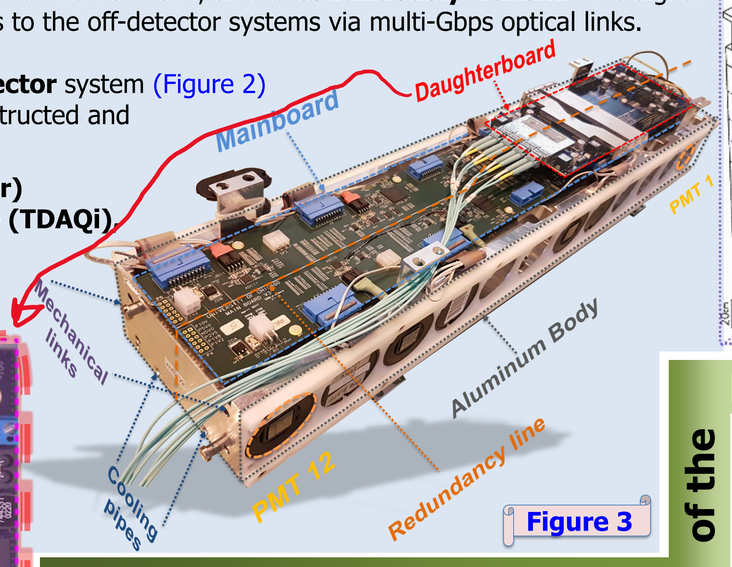

Figure 3

The **Daughterboard revision 5** [5].

- **Double Redundancy - 2x** fully independent sides to eliminate many possible single failure points .
- Power circuitries to handle voltage distribution and current monitoring.
- **Cs** interfaces (5V) to control the Cs calibration system.
- **xADC** interfaces to digitize added external sensors.
- **HVOpto** interfaces to control and monitor the **internal HV** option.
- **400 pin FMC** to interface with the MB.
- **Kintex Ultrascale+ FPGAs** to drive all the DB digital logic that distributes clocks and commands to the MB and sends the digitized PMTs data to the PPr via multi-Gbps optic links .
- **48 bit ID chips** to provide unique hardware ID number per side per DB.
- **GBTxs** to provide high quality **LHC synchronized clocks** to drive the GTY transceivers and the Front-End digitizing logic, as well as Front-End **configuration commands, remote reset** and **remote JTAG** control.
- **JTAG** interfaces to allow **FPGAs and PROMs reconfiguration**.
- **GBTx I2C** interface to control and monitor **GBTxs registers**.
- **4x SFPs** (allowing nominal running with either one or two working links)
  - **2x RX** – one to each GBTx to receive GBT FEC protected words.
  - **4x TX** – two from each FPGA to transmit GBT CRC protected words.

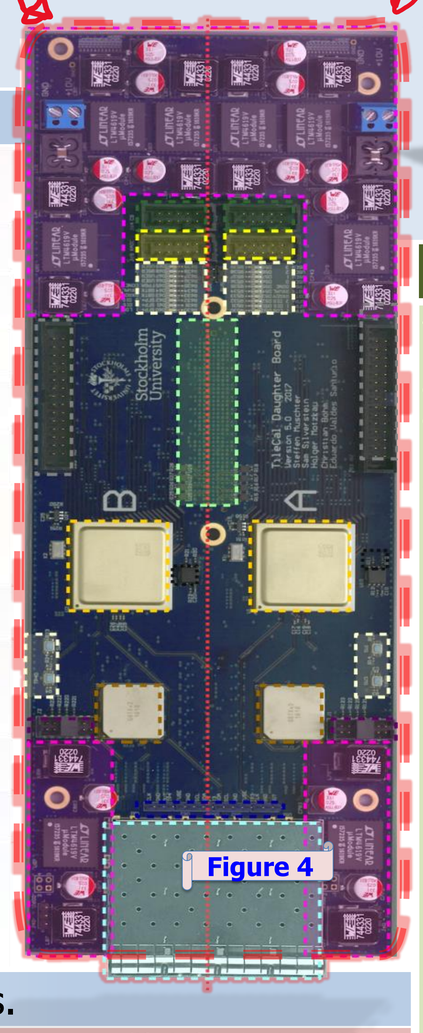

Figure 4

Radiation tests results.

- The design proved to **withstand** up to **20 kRad of TID**, being enough to qualify it for the HL-LHC lifetime for the initially expected doses. **New dose estimates** were obtained by **new simulations** with **updated geometry** require the board to be re-tested up to **72 kRad** or **16 kRad** with **annealing**.
- The **NIEL** test was performed with a **52 MeV proton** beam, hence the target fluence was achieved while simultaneously exposing the board to **768.2 kRad** of **equivalent TID**. Therefore, the **test** was **inconclusive** and needs to be re-done in a facility capable of achieving the target fluence **of 9.00 × 10^{12} n ×cm^{-2}** with **neutrons**.
- The **SEU** tests resulted in **4934 SEUs** over a fluence of **2.05 × 10^{11} protons cm^{-2}**, of which only **11 SEUs could not be corrected by the Xilinx Soft Error Mitigation (SEM) IP solution**. The uncorrectable SEU rates predict that **1.4 ±30% uncorrectable errors** are expected **per DB per year**. With Xilinx SEM and the TMR, it is expected that correctable SEUs will not affect nominal runs.
- The **SEE** tests showed that the **Kintex Ultrascale+ 16 nm FinFET** technology is **susceptible to SEL** with SEL-fluence rate increased from **2 × 10^{-11} SEL-fluence rate at 58 MeV** to **2.36 × 10^{-10} rate at 226 MeV protons** (Figure 5).
- The over-currents due to SEEs did not cause noticeable damage, however **SELs are not acceptable**.

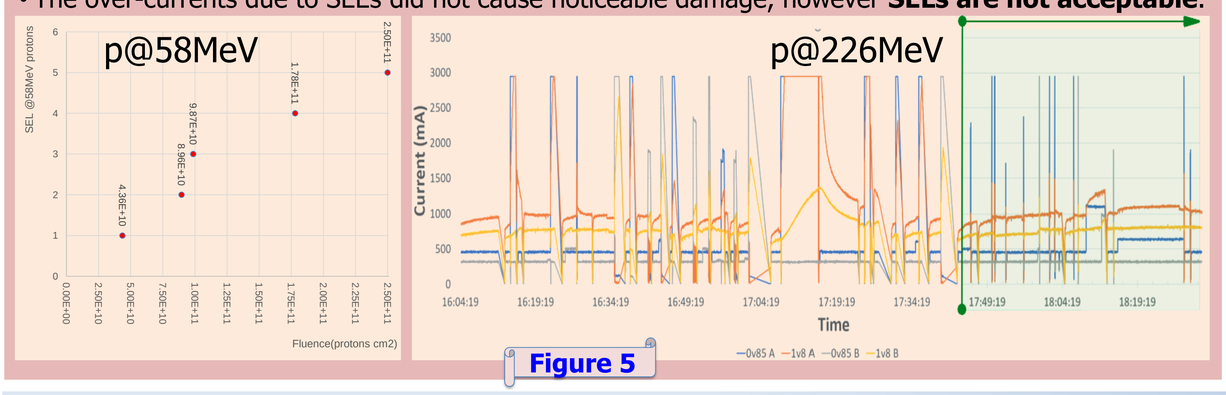

Figure 5

The **Redesign** of the **Daughterboard**

The redesign of the DB 5 into **DB 6** aims to **solve** the **radiation issues** found, and to incorporate **more robust timing** and extra features to **minimize single points of failure** even further (Figure 6). Backwards compatibility with previous interfaces will be kept.

- Migrating to the **SEL-resistant 20 nm TSMC planar technology Ultrascale FPGA** family where SELs have not been observed [3]. Increased level of SEU rates [2] within the capabilities of SEM and TMR to mitigate.
- Migrate the power-on sequence done by means of an RC circuit to a chain of DC-DC converters integrated with an **SEL current limiting circuitry** that will increment the robustness of the board to the presence of isolated SEL.
- **Improve the firmware clocking and timing scheme** by using the Ultrascale XYPHY BITSLICE byte architecture for the ADC read-out and the complex clock-diverse network, to allow better timing closure and avoid congestion during the firmware implementation [5] (Figure 7).
- Buffer and control all JTAG interfaces through a flash based **ProASIC FPGAs**, to avoid undesired digital noise from a GBTx Eports during a failing-downlink situation.
- Migrate from large electrolytic capacitors at the DC-DC regulators **to conductive polymer capacitors**, which have been observed to be radiation tolerant with no impact to performance after 200 kRad at 500 rad/h [4].

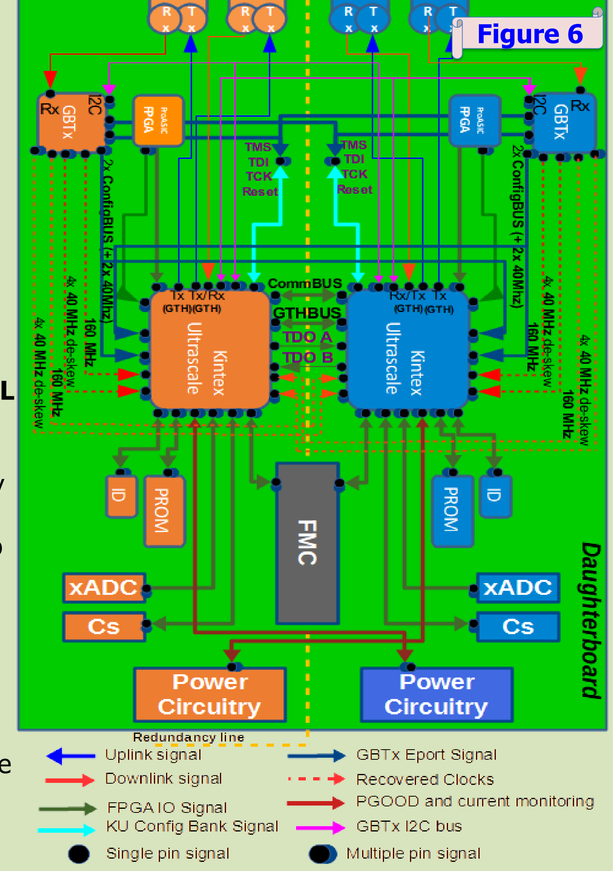

Figure 6

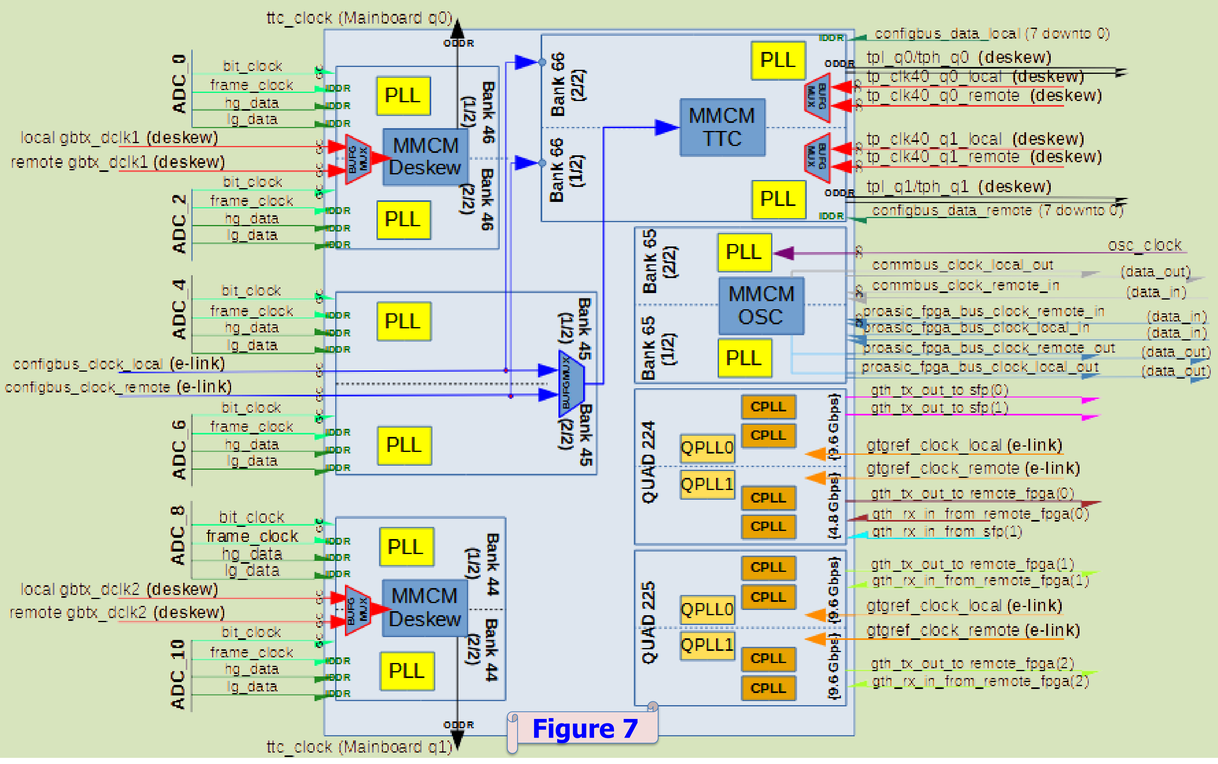

Figure 7

Conclusions.

The DB 5 cannot entirely fulfill the HL-LHC radiation requirements because of the design being incapable to mitigate the Kintex Ultrascale+ 16 nm FinFET process sensitivity to SEL appearances. DB 6 will migrate to a more SEL-resistant FPGA, add extra protection to SEL appearances and increase radiation tolerance by using conductive polymer capacitors. DB 6 must be tested for TID, NIEL and SEE to qualify it as mandated by ATLAS policies. DB 6 will further improve and optimize the already complex DB clocking scheme. DB6 will add an extra layer of hardware control and monitoring to minimize single points of failure and allow mitigation of any unexpected issue appearances during nominal runs. Around 930 DB6s will be produced as the contribution of Stockholm University to the HL-LHC era for TileCal.

Relevant references.

[1] ATLAS collaboration. Technical Design Report for the Phase-II Upgrade of the ATLAS Tile Calorimeter. CERN-LHCC- 234 2017-019, ATLAS-TDR-028, 2018
[2] Single Event Upset Characterization of the Zynq UltraScale+ MPSoC Using Proton Irradiation, 2017 IEEE Radiation Effects Data Workshop (REDW), DOI: 238 10.1109/NSREC.2017.8115448
[3] Single-Event Latch-Up: Increased Sensitivity From Planar to FinFET, 2017 IEEE Radiation, IEEE Transactions on Nuclear Science 2018, DOI: 10.1109/TNS.2017.2779831
[4] Capacitors for Spacecraft: Withstanding a Harsh Radiation Environment, https://www.ttiinc.com/content/tti244inc/en/resources/marketeye/categories/passives/me-slovick-20160809.html.
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[6] UltraScale Architecture Clocking Resources User Guide. https://www.xilinx.com/support/documentation/user_guides/ug572-ultrascale-clocking.pdf.

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