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Design of the Compact Processing Module for the ATLAS Tile Calorimeter

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The LHC plans a series of upgrades towards a High Luminosity LHC (HL-LHC) to increase up to 5-7 times the current nominal instantaneous luminosity. The ATLAS experiment will accommodate the detector and data acquisition system to the HL-LHC requirements during the Long Shutdown 3 (2024-2026), where the on- and off-detector electronics of Tile Calorimeter (TileCal) will be completely replaced with a new readout electronics system with new interfaces to the full-digital ATLAS trigger system.

In the HL-LHC era, the on-detector electronics will stream digitized data from the PMTs to 128 Compact Processing Modules (CPMs) operated in 32 ATCA carrier blades located in the counting rooms, requiring a total bandwidth of 40 Tbps to read out the entire detector.

The CPMs will be the core of the off-detector electronics, being responsible for the high-speed communication with the on-detector electronics and ATLAS DAQ system, clock distribution, data acquisition, and core processing functionalities. Each CPM is equipped with 8 Samtec FireFly modules connected to a Xilinx Kintex UltraScale FPGA for data buffering, online digital processing and on-detector electronics control. A Xilinx Artix 7 FPGA performs slow control functionalities for the clocking circuitry, power monitoring, Ethernet configuration, and monitors the phase drifts of the distributed clock.

This contribution presents the design of the first CPMs for the ATLAS Tile Calorimeter and its integration into the ATLAS TDAQ system. The results of the early performance testing with the on-detector electronics and ATLAS DAQ system are discussed, as well as the layout design and firmware architecture.

Minioral

No

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No

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No

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