Design of the Compact Processing Module for the ATLAS Tile Calorimeter

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on behalf of the ATLAS Tile Calorimeter System

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OUTLINE

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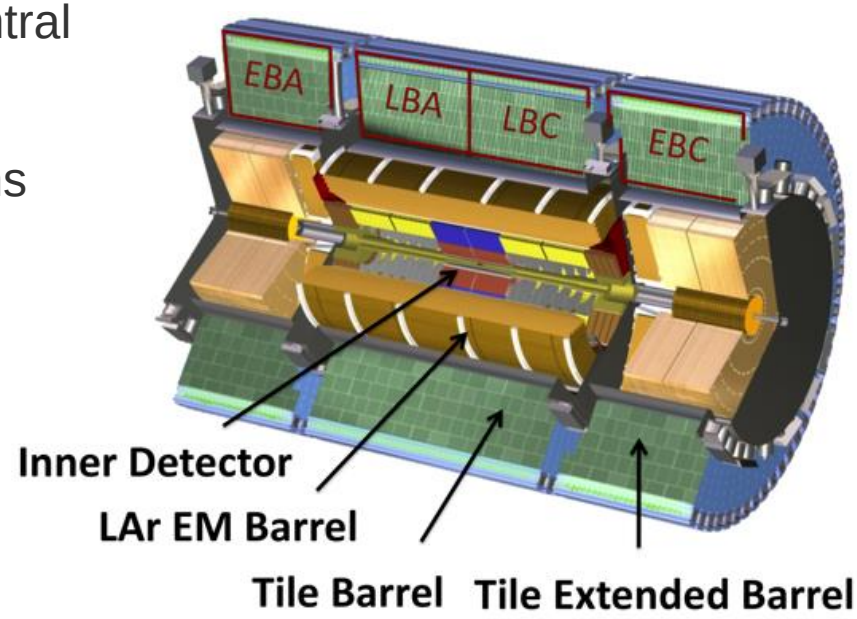
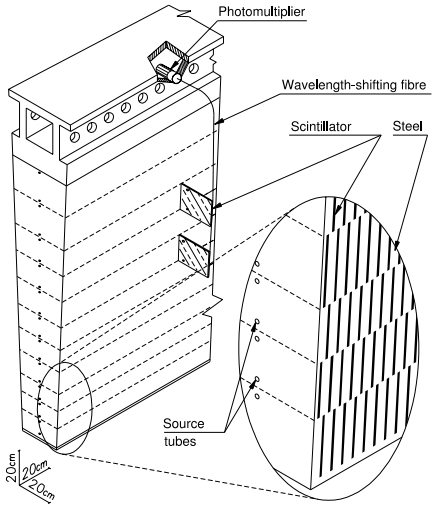
  - PHASE II UPGRADE
- COMPACT PROCESSING MODULE
  - HARDWARE AND PCB LAYOUT
  - CLOCK AND READOUT ARCHITECTURE
  - SIGNAL INTEGRITY AND CLOCK DISTRIBUTION TESTS
- SUMMARY

ATLAS Tile Calorimeter

- Segmented calorimeter made of steel plates and plastic scintillator tiles covering the most central region of the ATLAS experiment
- Measures energies of hadrons, jets, τ-leptons and E_T^{miss}
- 4 partitions: EBA, LBA, LBC, EBC
- Each partition has 64 modules
  - One drawer hosts up to 48 PMTs
  - Electronics is located in extractable "*drawers*" at the outermost part of the module

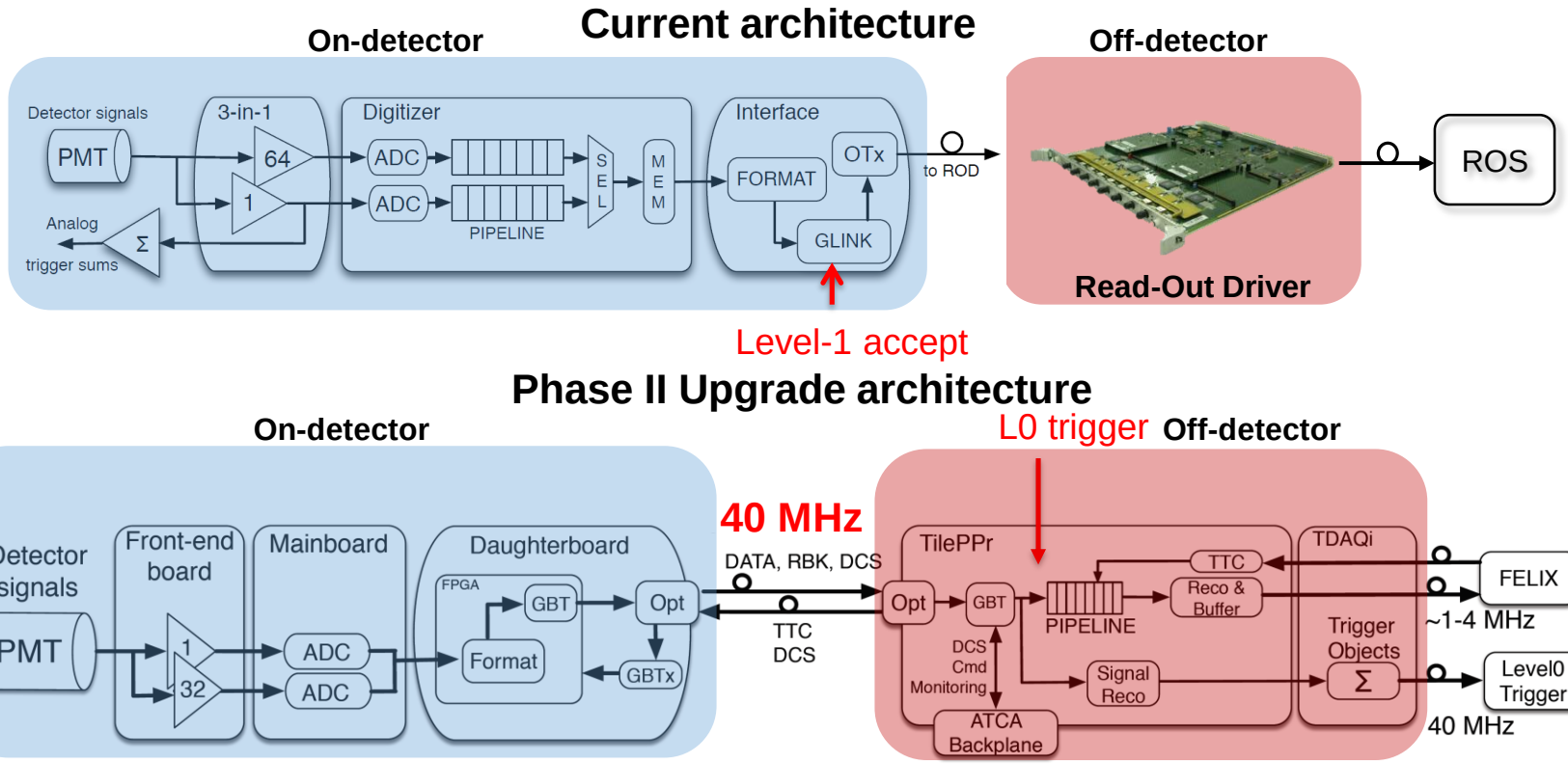




- Light produced by a charged particle passing through the plastic scintillating tiles is read out via wavelength shifting fibers to PhotoMultiplier Tubes (PMTs) inside the drawer
- Around 10,000 readout channels

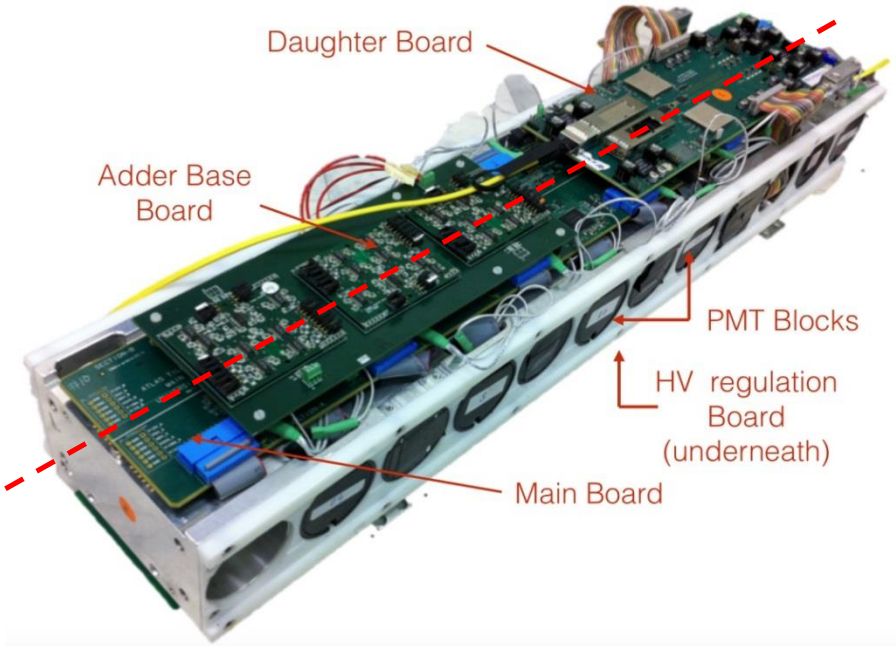
TileCal Phase II Upgrade

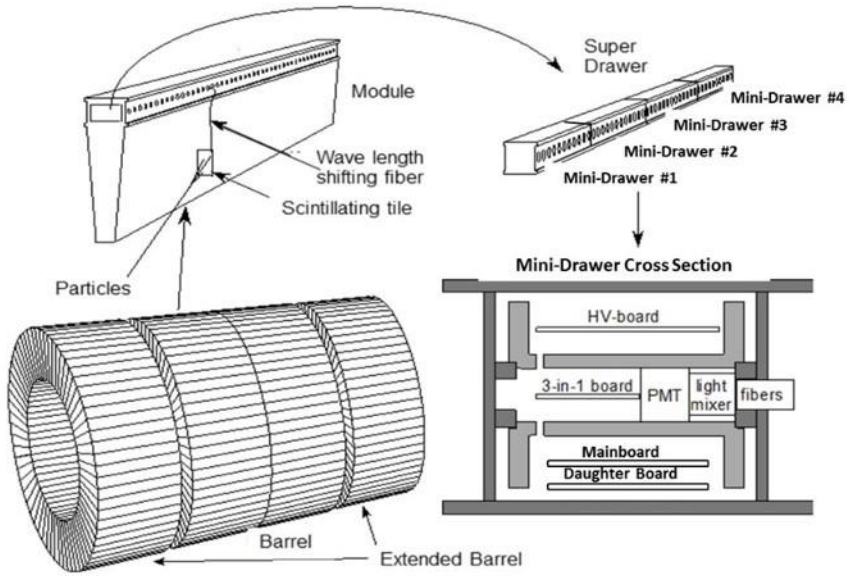
- **Large Hadron Collider plans to increase the instantaneous luminosity by a factor 5-7 around 2027→ High Luminosity-LHC**
- **Phase-II Upgrade: New readout strategy**
  - On-detector electronics will transmit full digital data to the off-electronics at the LHC frequency → **<u>40 Tbps to read out the entire detector and ~6,000 optical fibres</u>**
  - Buffer pipelines are moved to off-detector electronics
  - Redundancy in data links and power distribution → improve system reliability



Phase II on-detector electronics

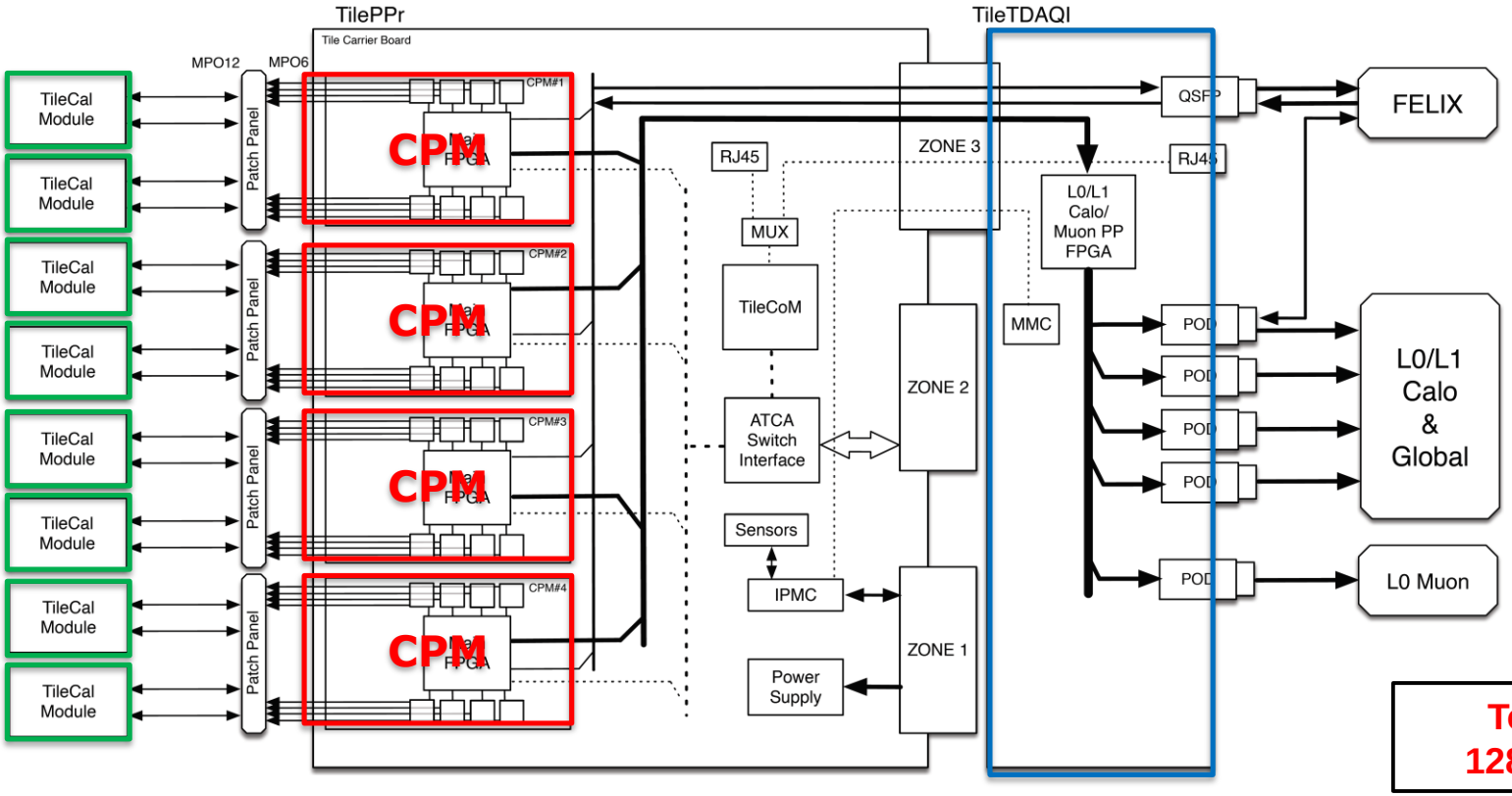
- The Phase II module is composed of 4 mini-drawers (up tp 48 PMTs). Each mini-drawer has 2 independent read out sections for redundant cell readout
  - 12 PMTs + 12 front-end boards reading out 6 TileCal cells
  - 1 × MainBoard: operation of the front-end boards
  - 1 × DaughterBoard: data high speed link with the off-detector electronics
  - 1 × High Voltage distribution board
  - 2 × Low Voltage Power Supply bricks: low voltage power distribution, one for each independent side → 8 bricks form a Low Voltage Power Supply (LVPS).





Phase II off-detector electronics

- **The Tile PreProcessor is the core element of the off-detector electronics**
  - Data processing and handling from on-detector electronics
  - Provides clocks and configuration for the TileCal modules
  - Interface with the ATLAS trigger and readout systems (FELIX)

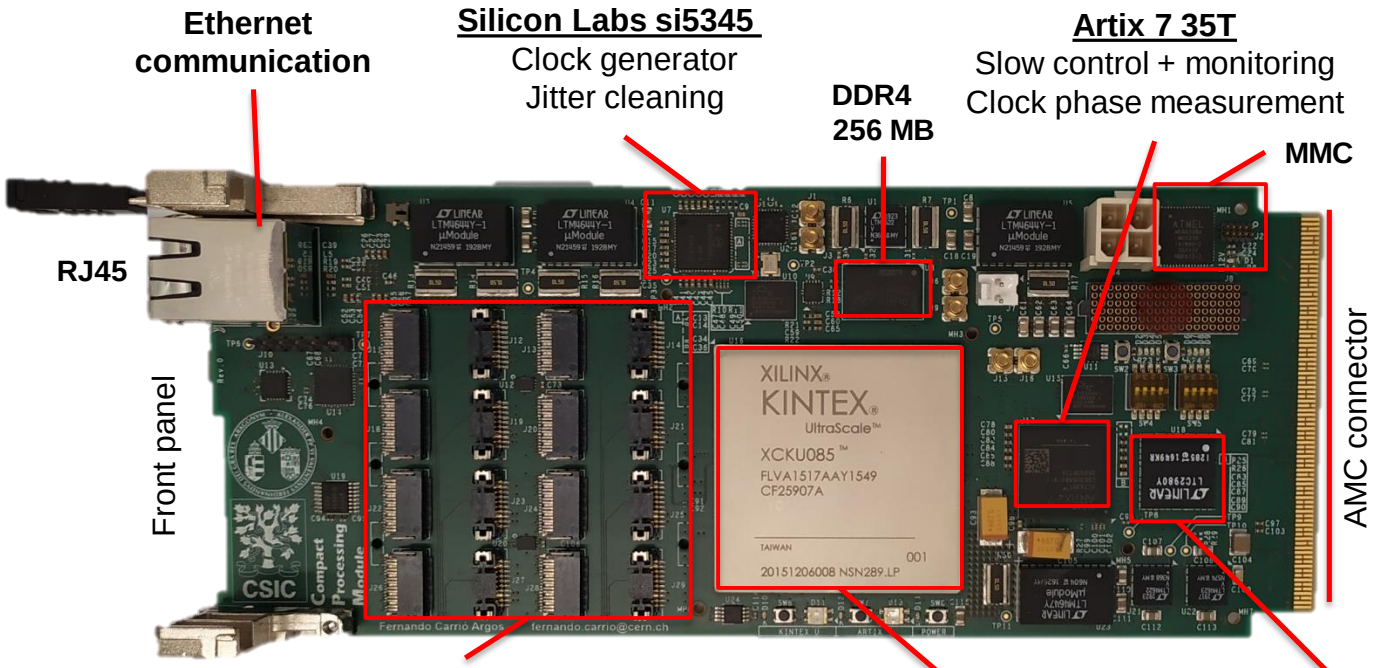


Total of 128 CPMs

- **32 TilePPr** boards in 4 ATCA shelves**:** ATCA carrier + **4 Compact Processing Modules**
- **32 TileTDAQ-I:** Interfaces with L0Calo, Global, L0Muon and FELIX system

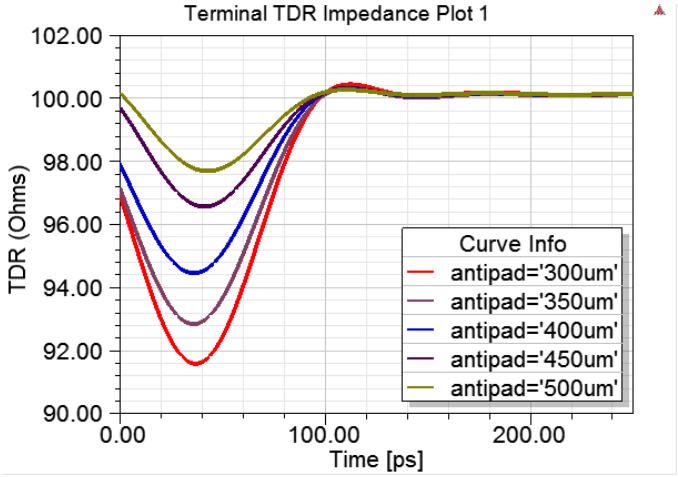
Compact Processing Module - Overview

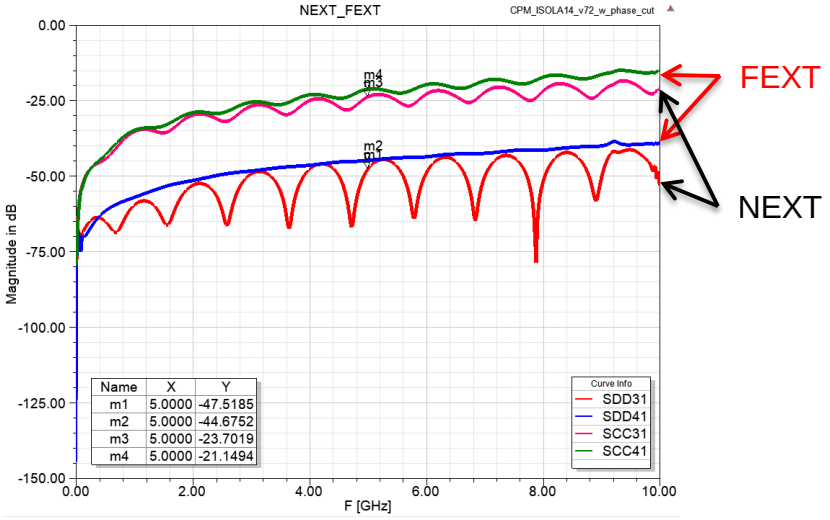
- **Single AMC board** with full-size form factor
  - **32 channels** through **8 Samtec Firefly modules** → Up to **400 Gbps** via optics
  - **14 channels** through AMC connector → Up to **175 Gbps** via electrical backplane
  - **Kintex KU085 for proto(v1), KU115 for final design**
- High bandwidth readout system

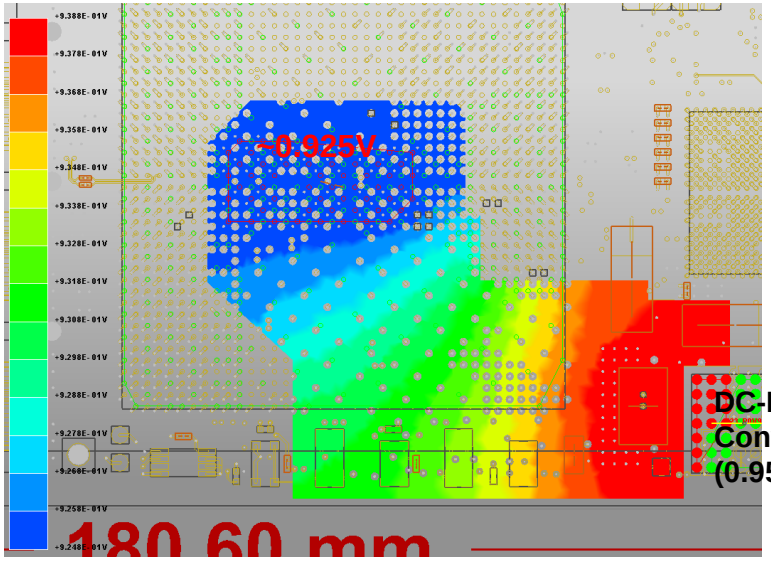


PCB layout design

- Total of 14 layers → 1.6 mm thickness
  - 8 layers for PWR/GND, 6 layers for signals
  - ISOLA FR408HR ($\varepsilon_r = 3.68$, $\tan\delta = 0.0092$)
- High-speed layout design and optimization
  - Supression of impedance discontinuities: Differential vias, connections, DC-blocking caps
  - Skew compensation to mitigate differential to common mode conversion
- IR voltage drop simulation on power rails

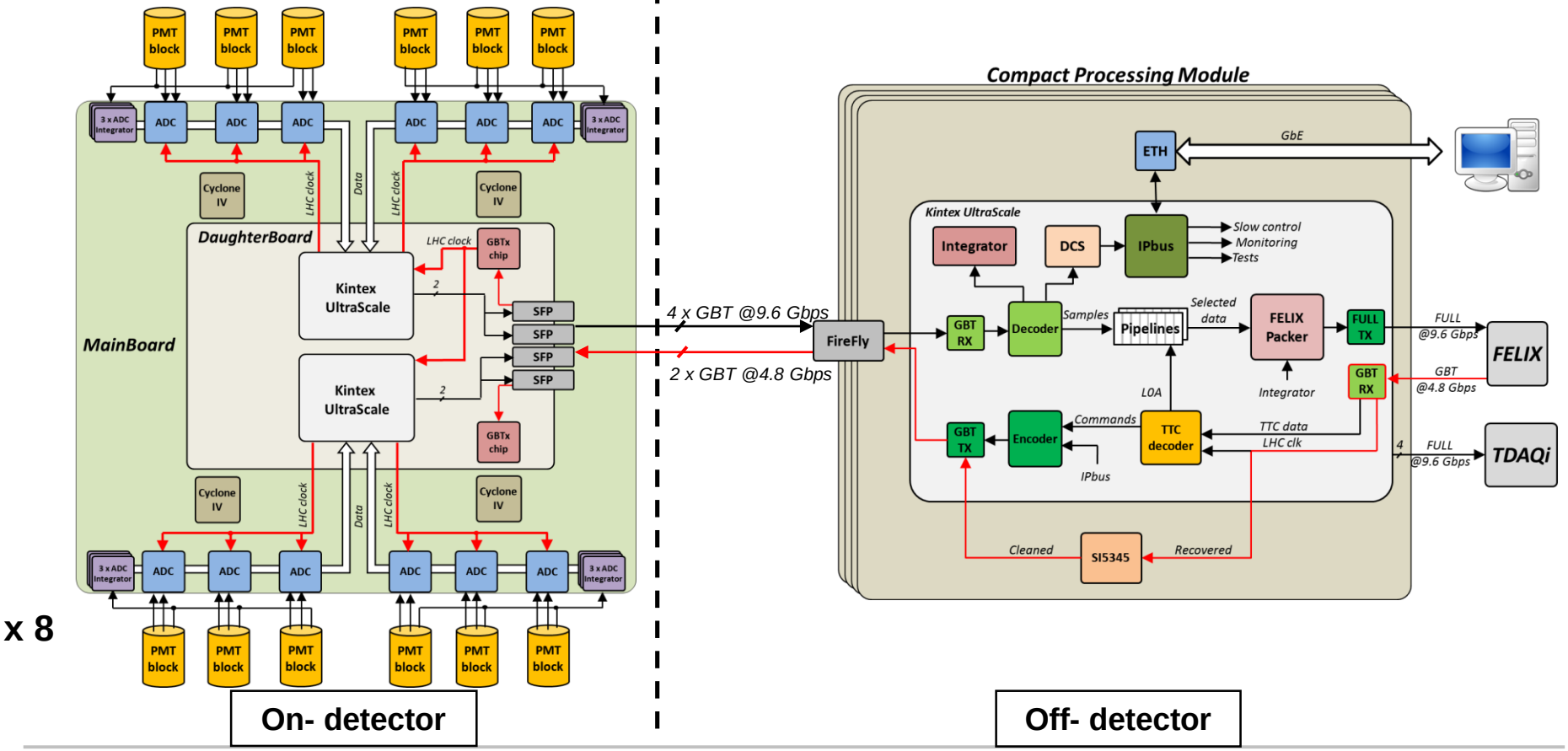






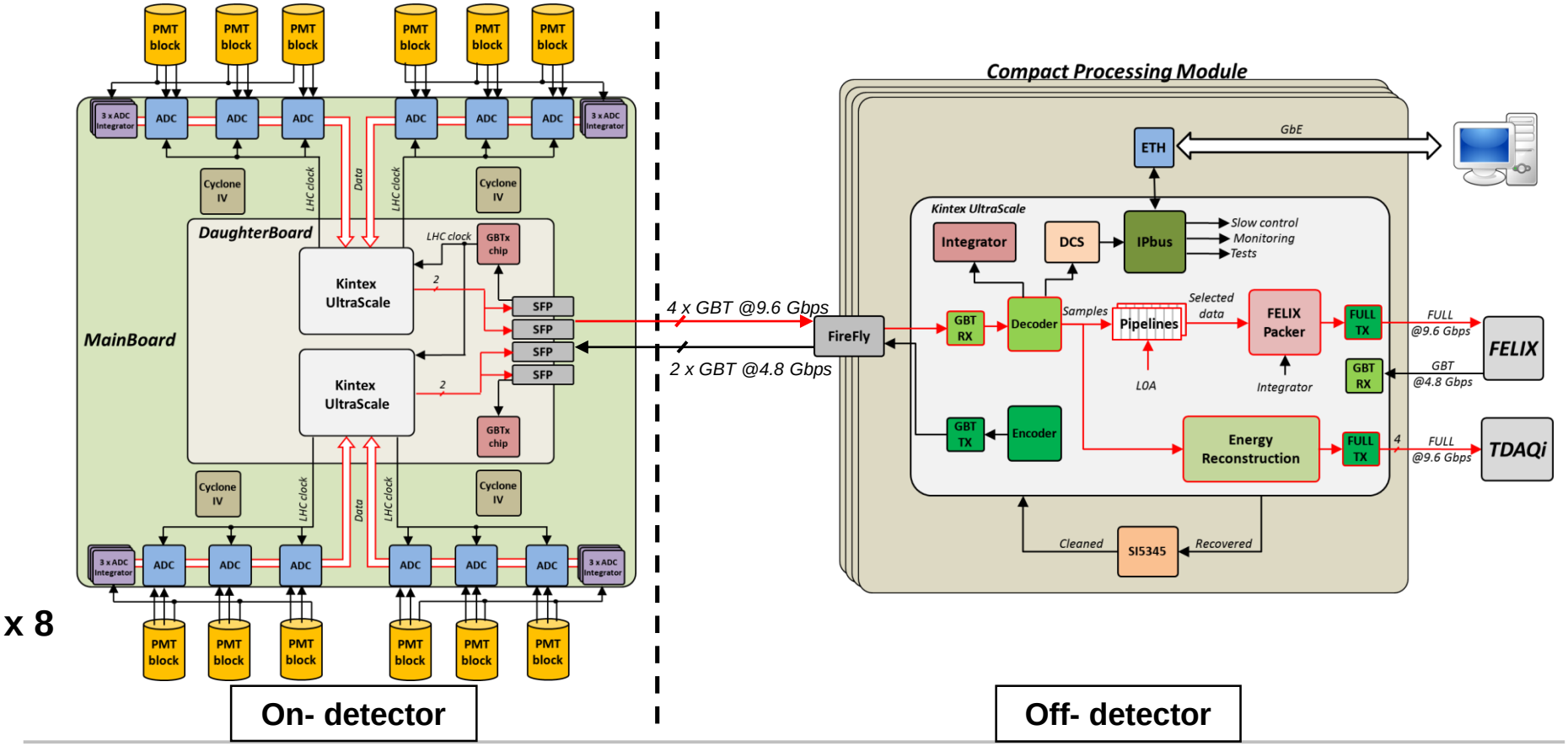
On-detector Readout and Operation

- High-speed interface with on-detector electronics - DaughterBoard
  - 32 links@4.8/9.6 Gbps , GigaBit Transceiver (GBT) protocol
  - Operation and readout of 2 TileCal modules per CPM → 8 mini-drawers
    - Up to 96 PMT channels with two gains
    - Configuration, TTC and LHC clock distribution
  - Data buffering of 10 μs per channel and gain



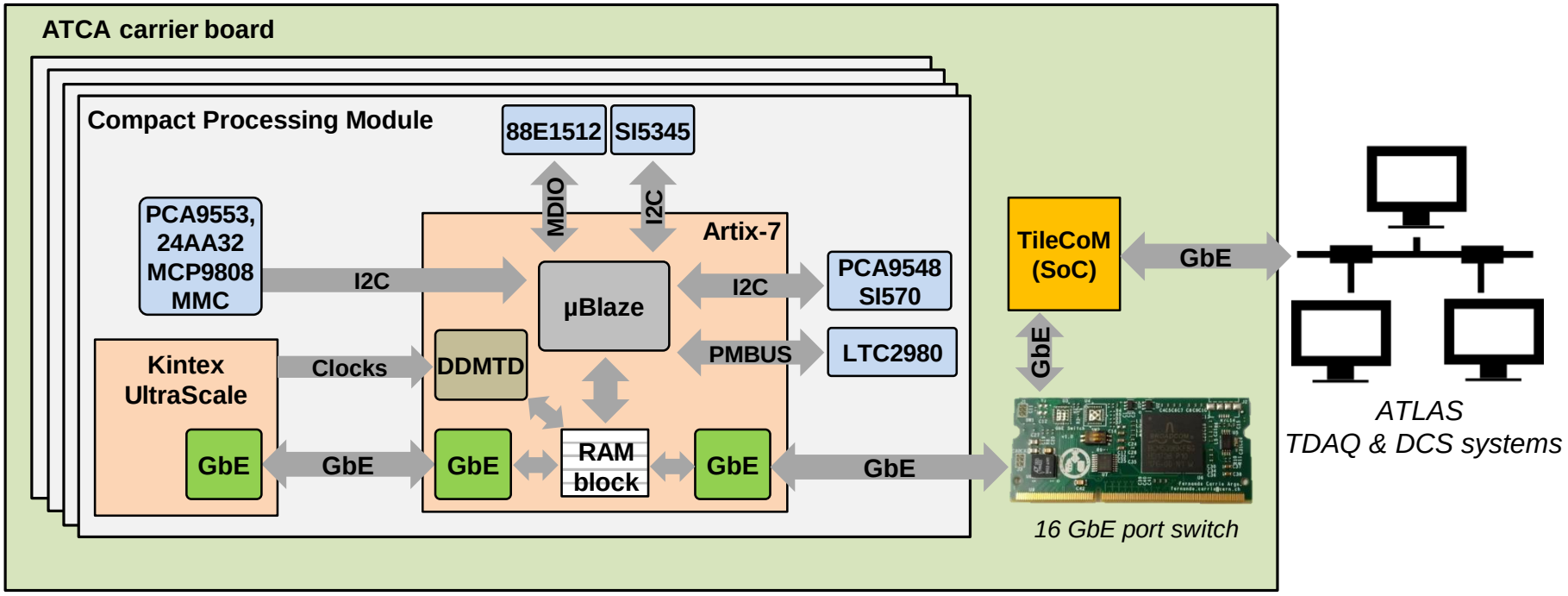
Trigger and DAQ path

- High-speed interface with ATLAS trigger system and FELIX
  - FULL mode protocol → 8B/10B encoding, 9.6 Gbps
  - Real-time energy reconstruction to TDAQi @40 MHz
    - 4 FULL mode links@9.6 Gbps
  - Transmission of Level-0/1 trigger selected events to FELIX @1 MHz
    - 1 FULL mode link@9.6 Gbps



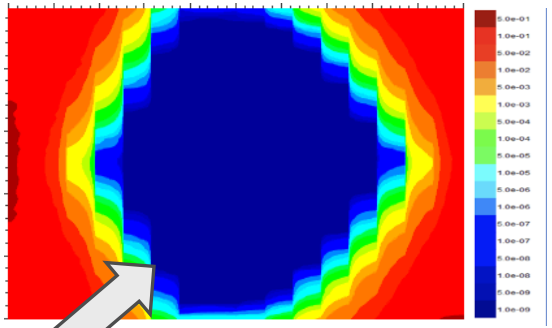
Detector Control System and configuration

- The Artix 7 FPGA controls and monitors all on-board peripherals
  - Clock unit & power system configuration
  - On-board monitoring
    - V/I monitoring, temperature sensors, optical modules, clocks
    - Receives on-detector monitoring data through Kintex UltraScale FPGA
  - Monitors phase drifts in the distributed LHC clock using the DDMTD circuit
- Communication with TDAQ and DCS systems through the ATCA carrier board



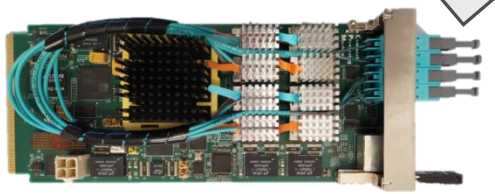
Signal integrity measurements

- Samtec Firefly modules @ 4.8 Gbps & 9.6 Gbps
  - Keysight DCA-X86100D sampling oscilloscope
  - Acceptable jitter values measured with PRBS-31 data pattern
- Bit Error Rate tests
  - Test bench with two CPMs, local clocks and 1.5-meter fibers
  - 32 links at 9.6 Gbps with PRBS31 pattern during one week
  - Total BER better than $1.6 \cdot 10^{-17}$ for a confidence level of 95%



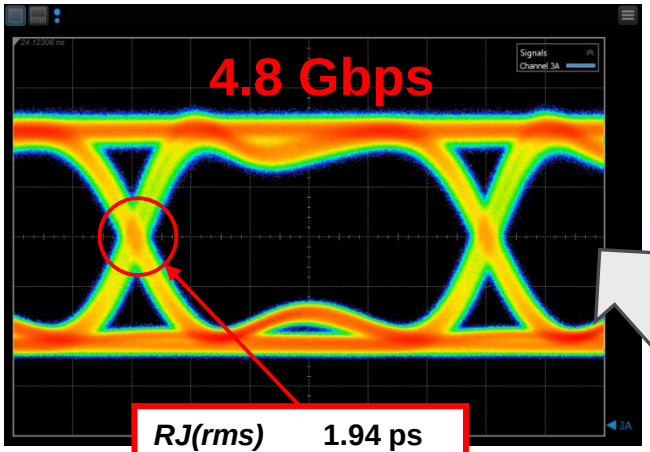
IBERT @ 9.6 Gbps (FPGA internal)

Eye Width	**191.84 ps**
Eye Height	**73.15%**

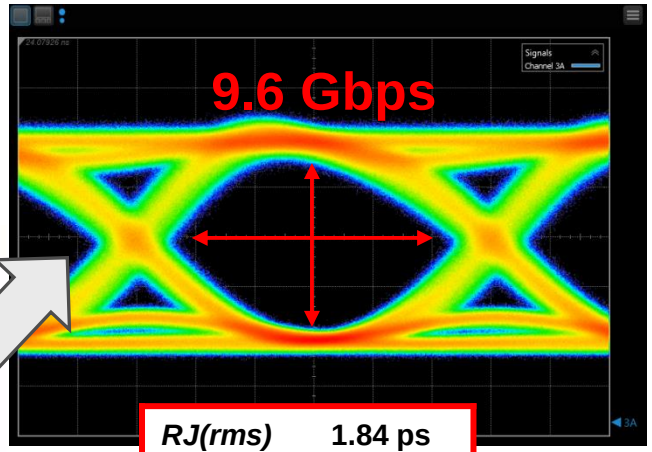


PRBS-31 @ 4.8 Gbps @ 9.6 Gbps

Eye Width	**85.92 ps**
Eye Height	**87.10%**



RJ(rms)	**1.94 ps**
DJ (δ-δ)	**2.40 ps**
TJ (10^{-12})	**28.84 ps**

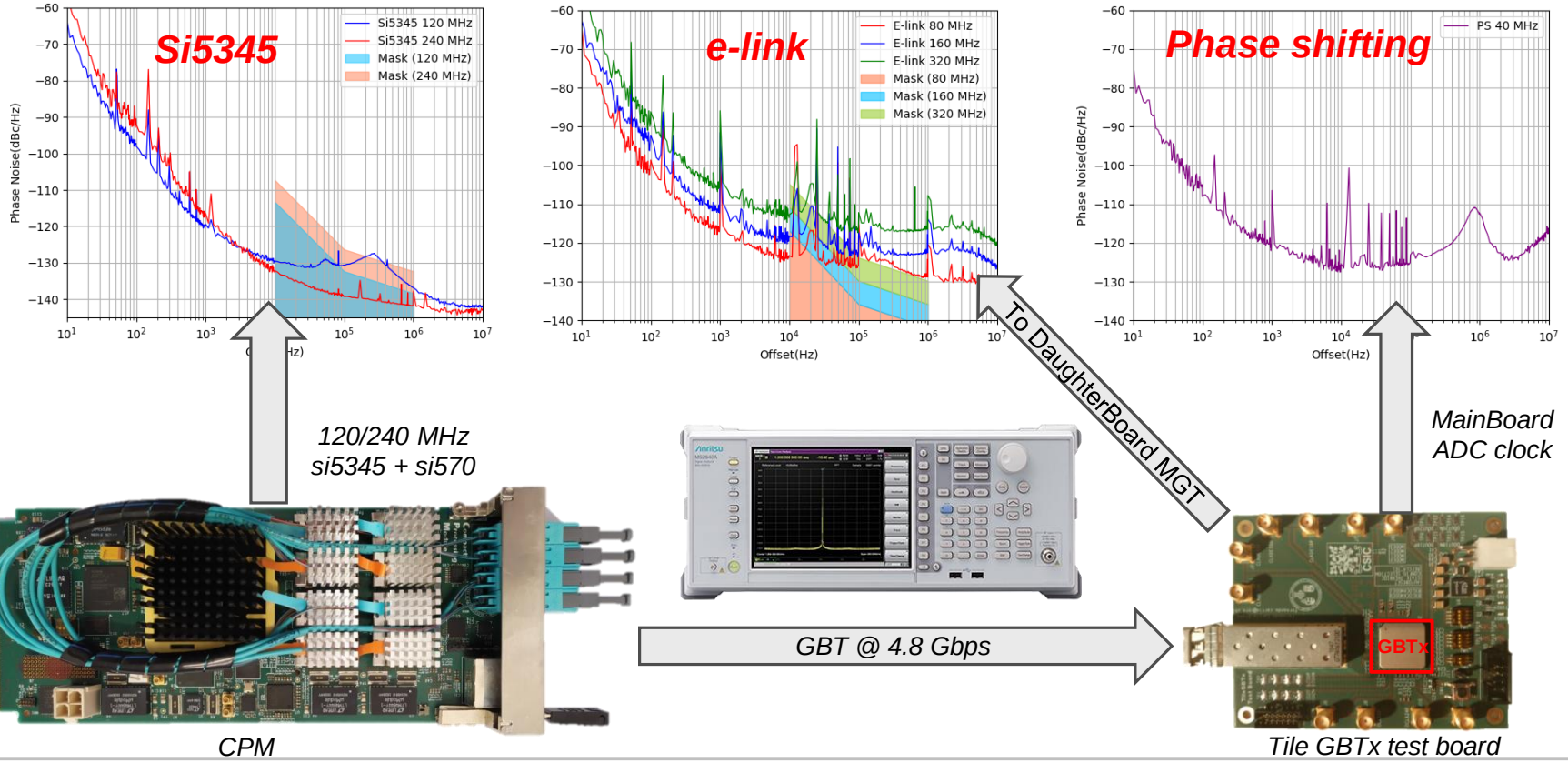


RJ(rms)	**1.84 ps**
DJ (δ-δ)	**5.85 ps**
TJ (10^{-12})	**30.96 ps**

Clock distribution qualifications

- Measure the quality of the distributed clock by the Daughterboard GBTx chips
  - Sampling clocks distributed to the MainBoard ADCs
  - Clocks driving the Multi Gigabit Transceivers in the Daughterboard FPGAs (Kintex UltraScale)

- Measurements done with an Anritsu MS2840A signal analyzer
  - Higher phase noise values than Xilinx recommends for GTH clocks → Additional TX jitter
    - Stable communication with DaughterBoard v5 was demonstrated using e-link



Summary

- New conditions imposed by HL-LHC requires a complete redesign of the TileCal on-detector and off-detector electronics
- Off-detector electronics for the Phase II Upgrade
  - 32 ATCA carrier and 128 Compact Processing Modules to read out TileCal
  - Total bandwidth of 40 Tbps between on-detector and off-detector
- Each Compact Processing Module
  - Clock distribution, readout and control of up to 2 TileCal modules
  - Triggered detector data transmission to FELIX
  - Reconstructed cell energy transmission to trigger system for trigger decision
- First prototypes are being validated
  - Single AMC board with full-size form factor
    - Kintex UltraScale, Artix-7 and 8 Samtec Firefly modules
  - Good signal integrity performance
  - Low noise clock distributed to on-detector electronics

THANK YOU FOR YOUR ATTENTION!