A New Scheme of Redundant Timing Crosschecking for Frontend Systems

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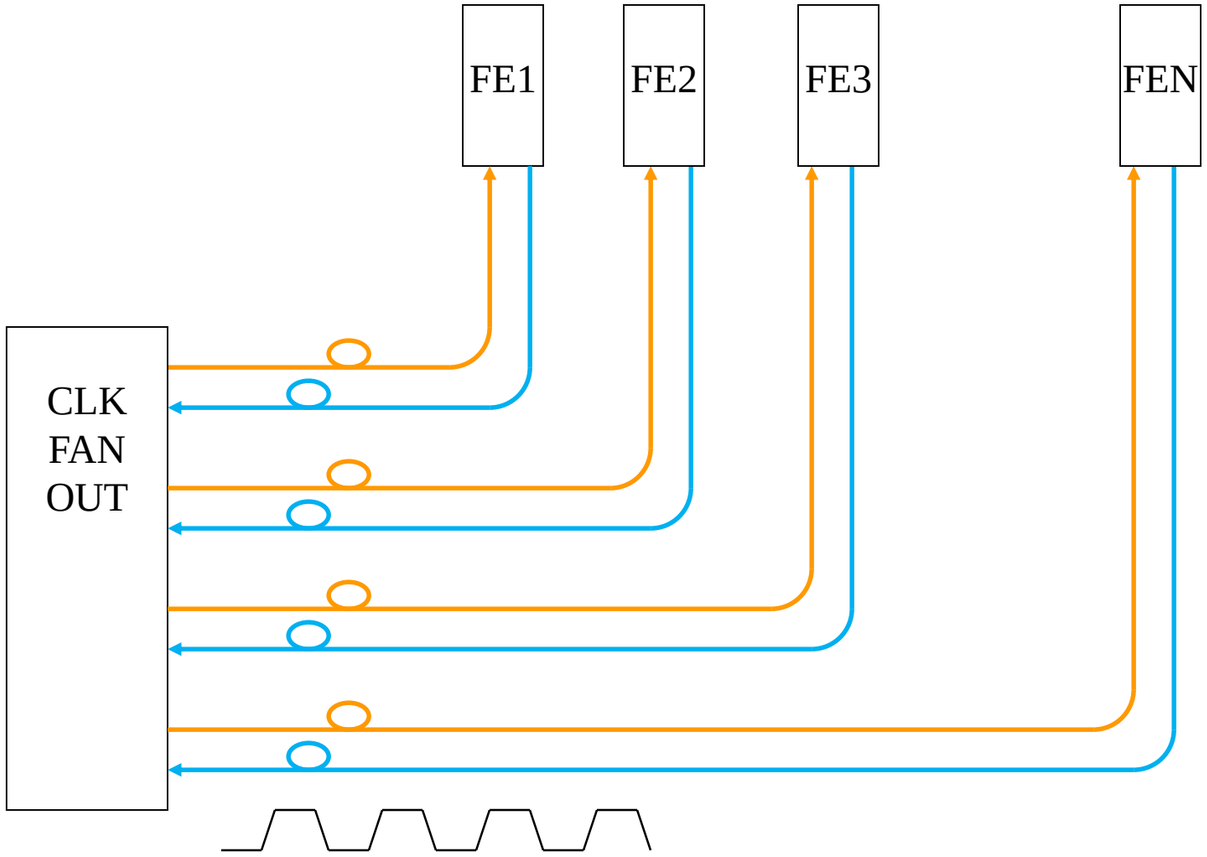
Fermilab

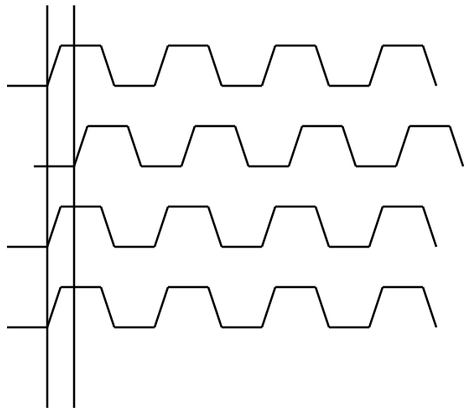
Oct. 2020

Introduction

- Establishing Common Timing Reference Across Entire System
- No Delay-Match Cables Required
- Cross Checking
- Redundant

Timing Distribution to Front-end Digitizers

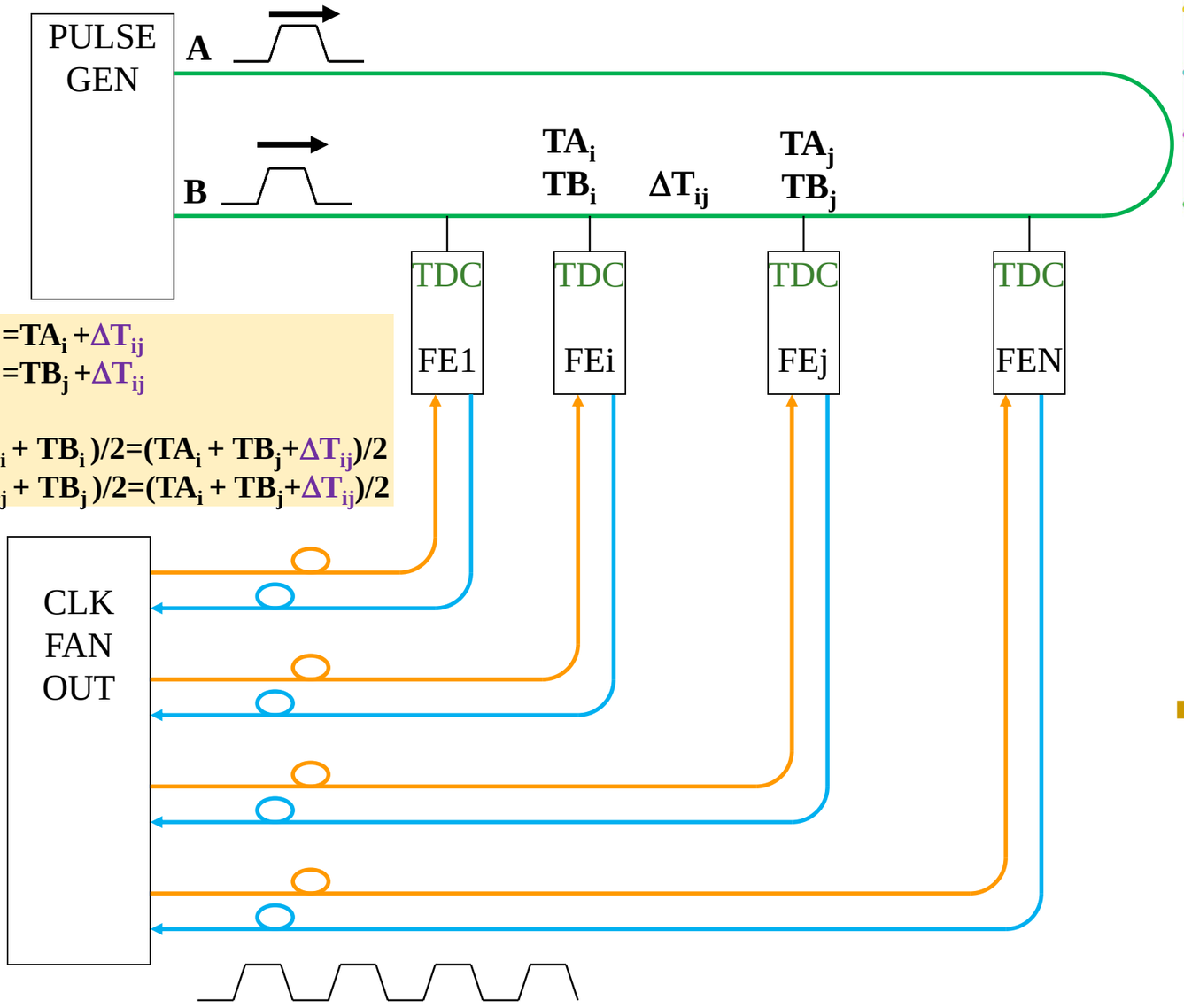




- Assume fibers are used to distribute clock to the front-end digitizers, with return path to compensate temperature variation.
- Clock skews between front-end modules may not be fully compensated due to temperature difference of silicon devices.
- It would be good to have some redundant cross checking between modules.

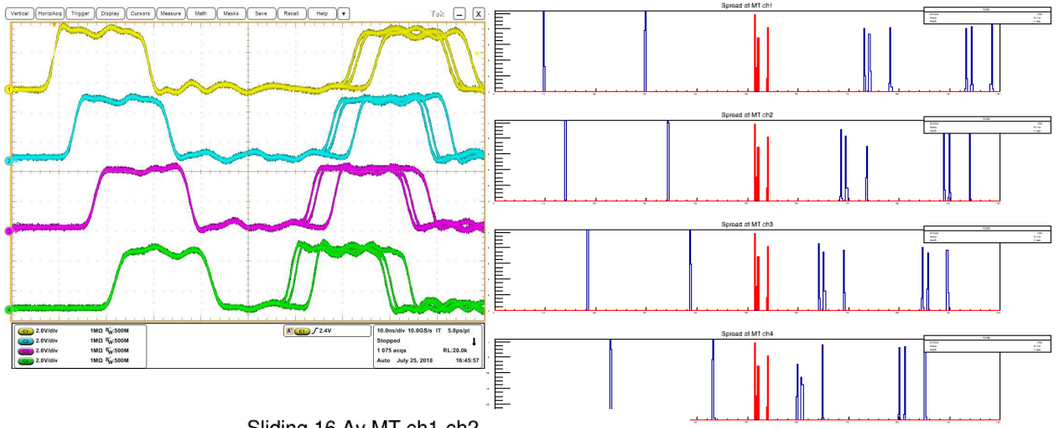
The Scheme Reported 2019

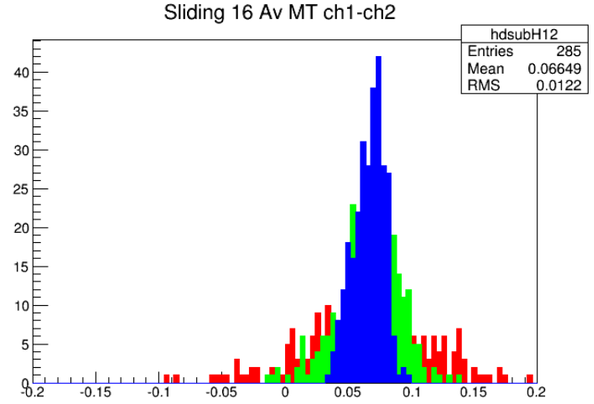
Sending Pulses from Cable Ends



$TA_j = TA_i + \Delta T_{ij}$
$TB_i = TB_j + \Delta T_{ij}$

$(TA_i + TB_i)/2 = (TA_i + TB_j + \Delta T_{ij})/2$
$(TA_j + TB_j)/2 = (TA_i + TB_j + \Delta T_{ij})/2$

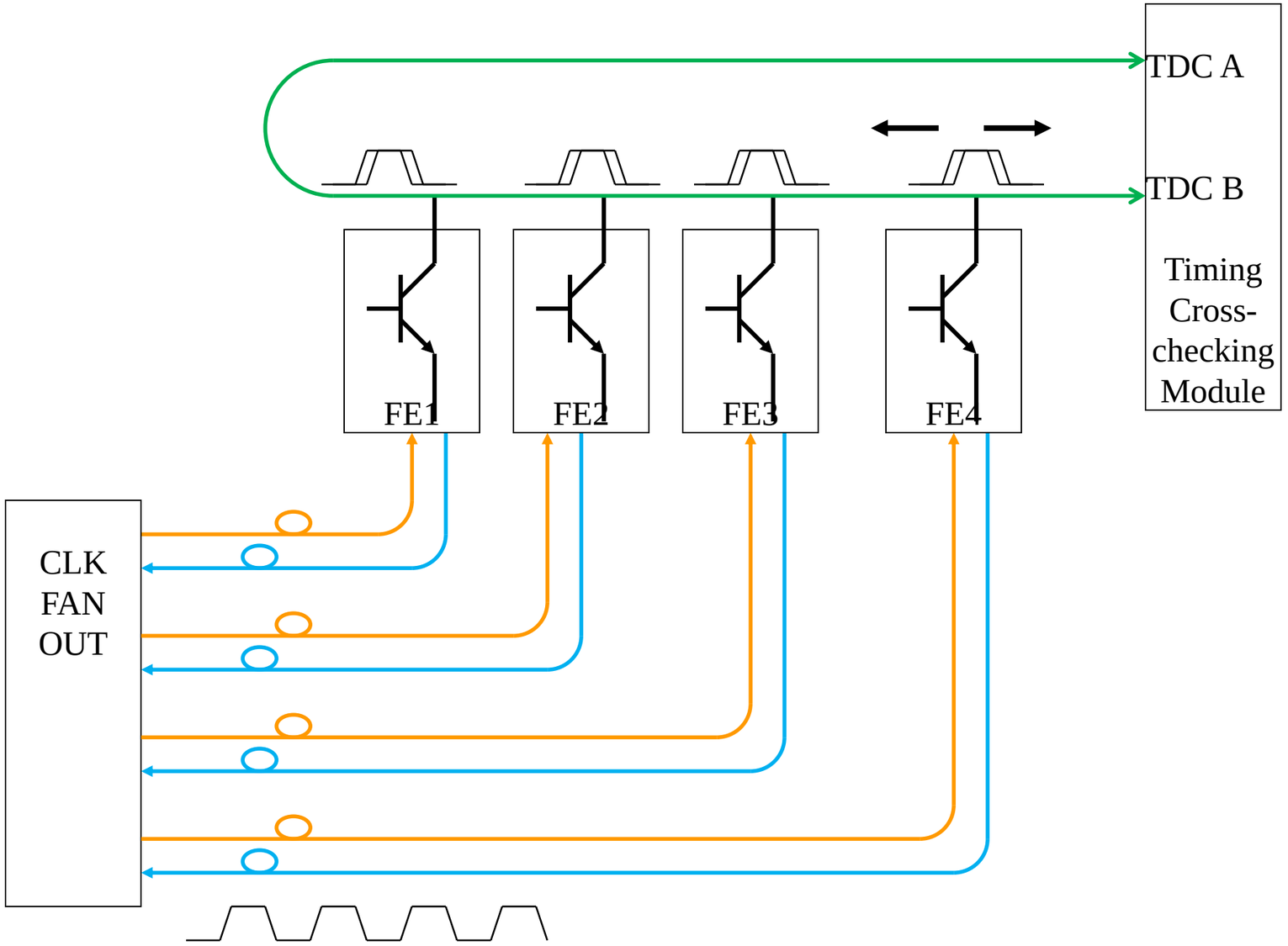




- Temperature variations of the cable delays are canceled mathematically
  - The values of the mean times may change with cable delays.
  - But mean times remain identical.

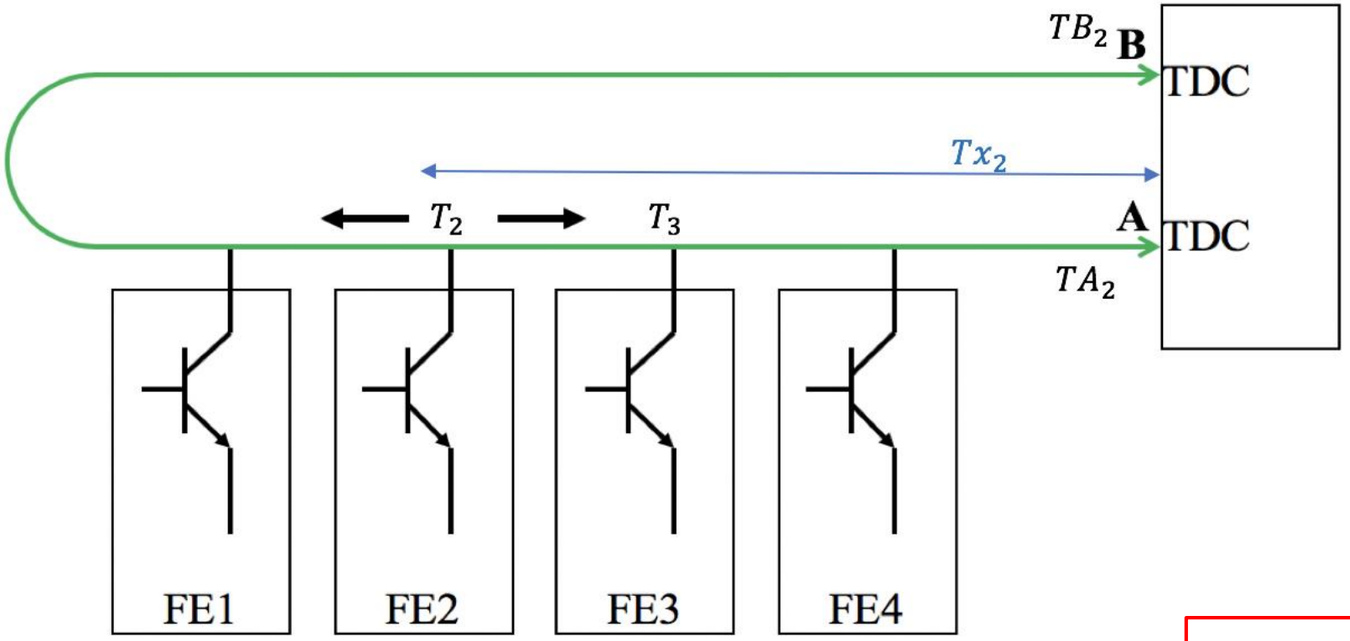
The New Scheme

Pulsing at the FE Modules



- Signals are sent from FE modules alternately synchronized with the system clock at each FE module.
- Using averages of the arrival times at TDC A and B, one can find the initial times of the pulses at different FE modules.
- Temperature variations of the cable delays are canceled mathematically.
- In this scheme, only two TDC channels are required at the Timing Cross-checking Module, not in FE modules.

Time Differences of FE Output Signals



$$TA_i = T_i + T(x_{i,A})$$

$$TB_i = T_i + T(x_{i,j}) + T(x_{j,B})$$

$$\frac{TA_i + TB_i}{2} = \frac{2T_i + T(x_{i,A}) + T(x_{i,j}) + T(x_{j,B})}{2}$$

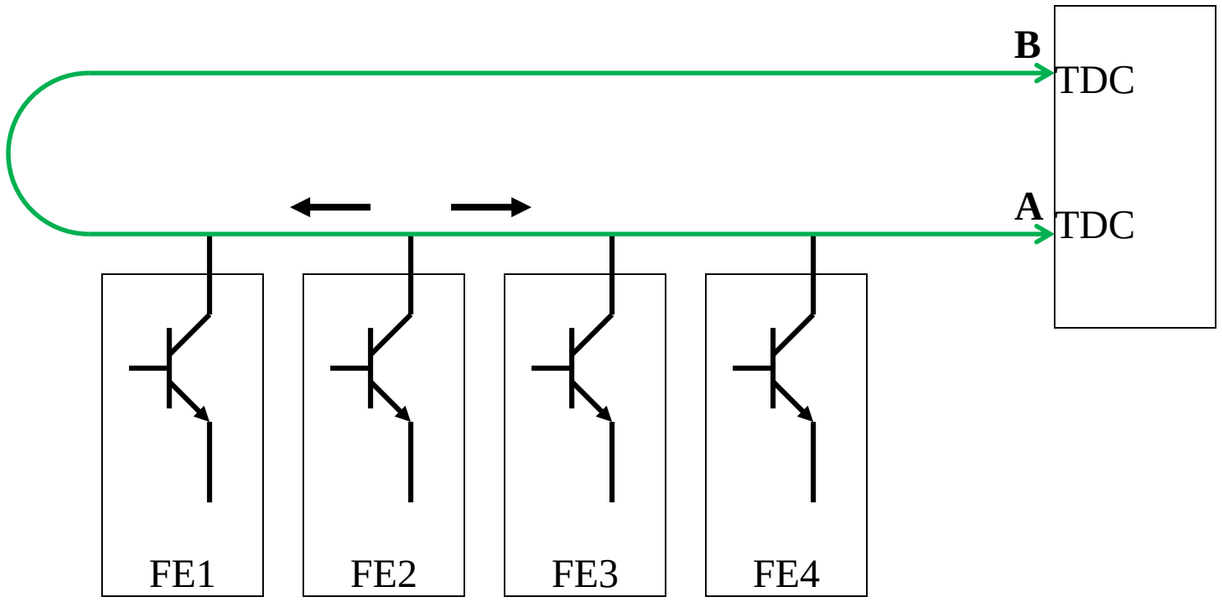
$$\frac{TA_j + TB_j}{2} = \frac{2T_j + T(x_{j,B}) + T(x_{j,i}) + T(x_{i,A})}{2}$$

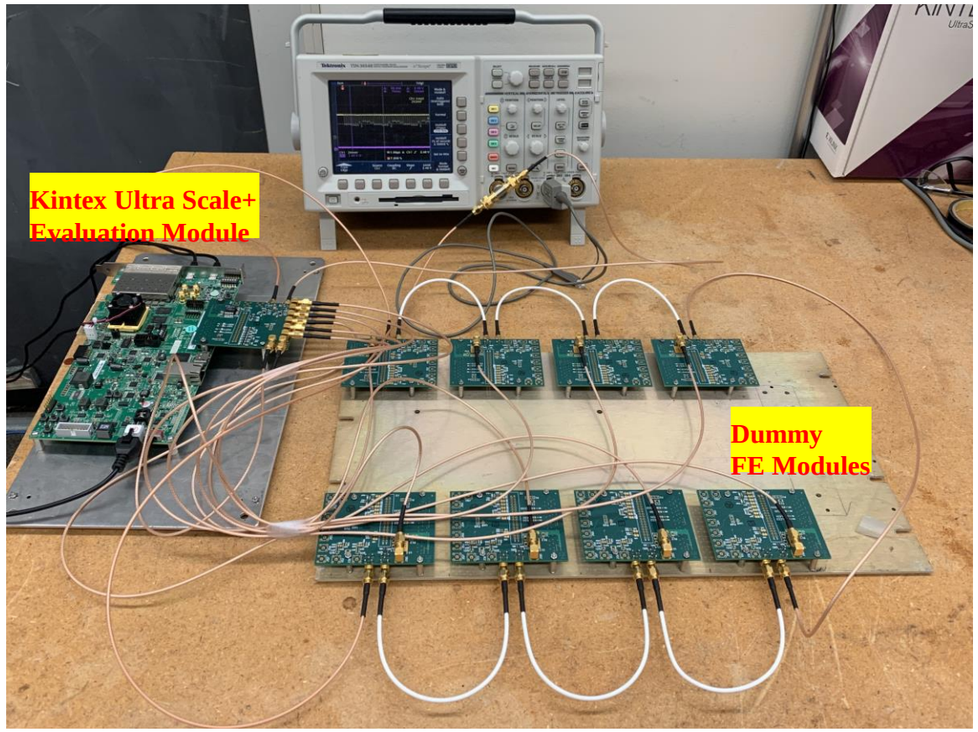
$$\delta T_{i,j} = \frac{TA_j + TB_j}{2} - \frac{TA_i + TB_i}{2} = T_j - T_i + \frac{Tx_{j,i} - Tx_{i,j}}{2}$$

- Temperature variations of the cable delays are canceled mathematically.
- The only requirement is that the signal travels both directions with the same speed in the cable.

Validation Tests

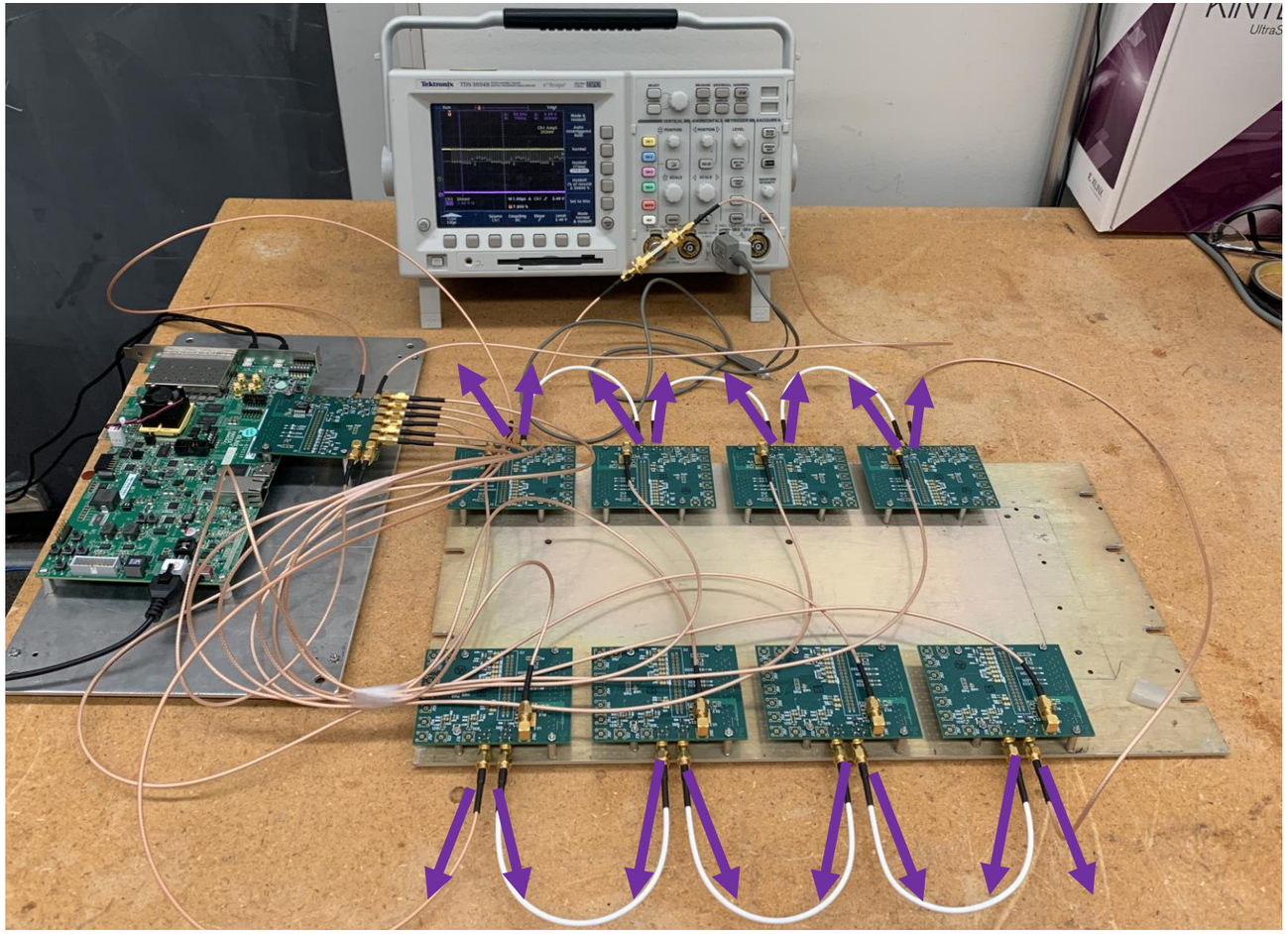
Cable Driven by Front End Modules

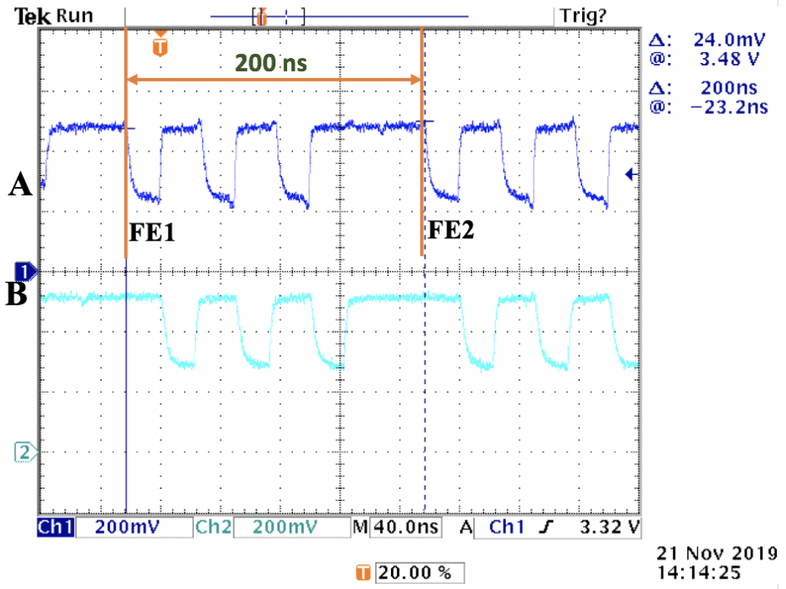


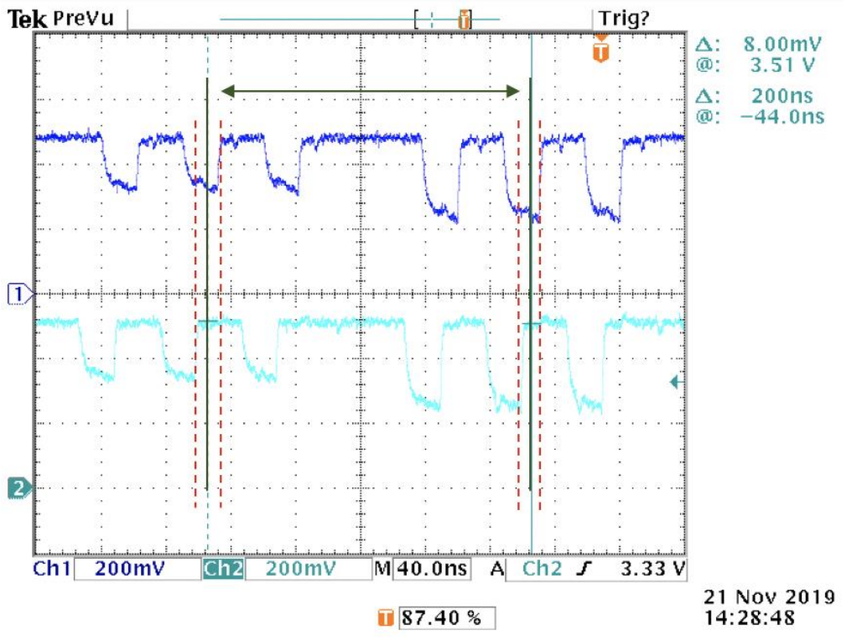


- The FE modules drive the cable alternately.
- The arrival times are measured by the TDC in the monitoring module.

Common Timing Bursts

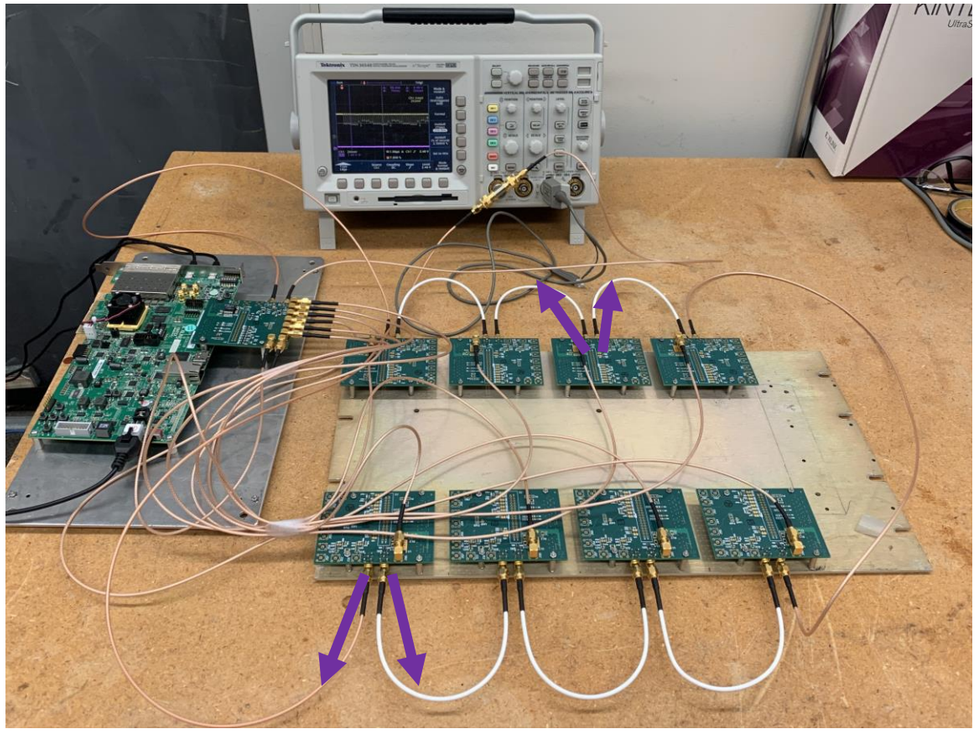


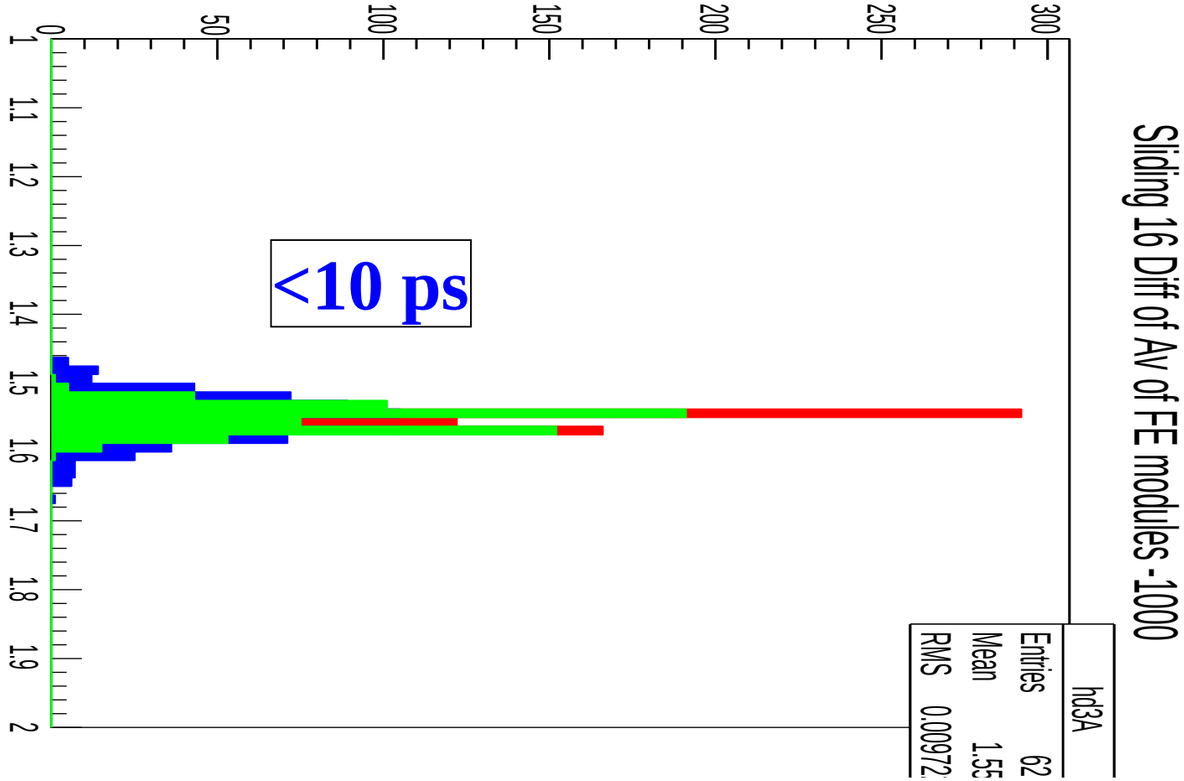




- Each module sends out a burst with three pulses.
- All edges of the bursts are used to improve measurement precision.

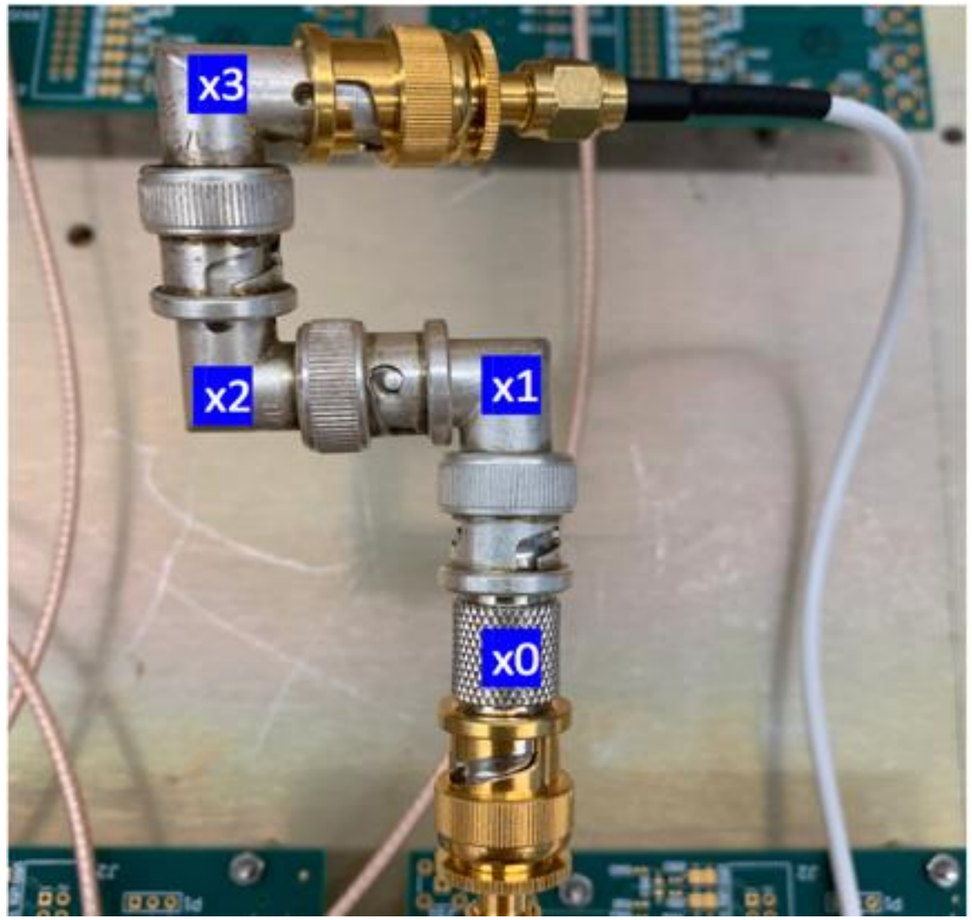
Time Differences Between Modules

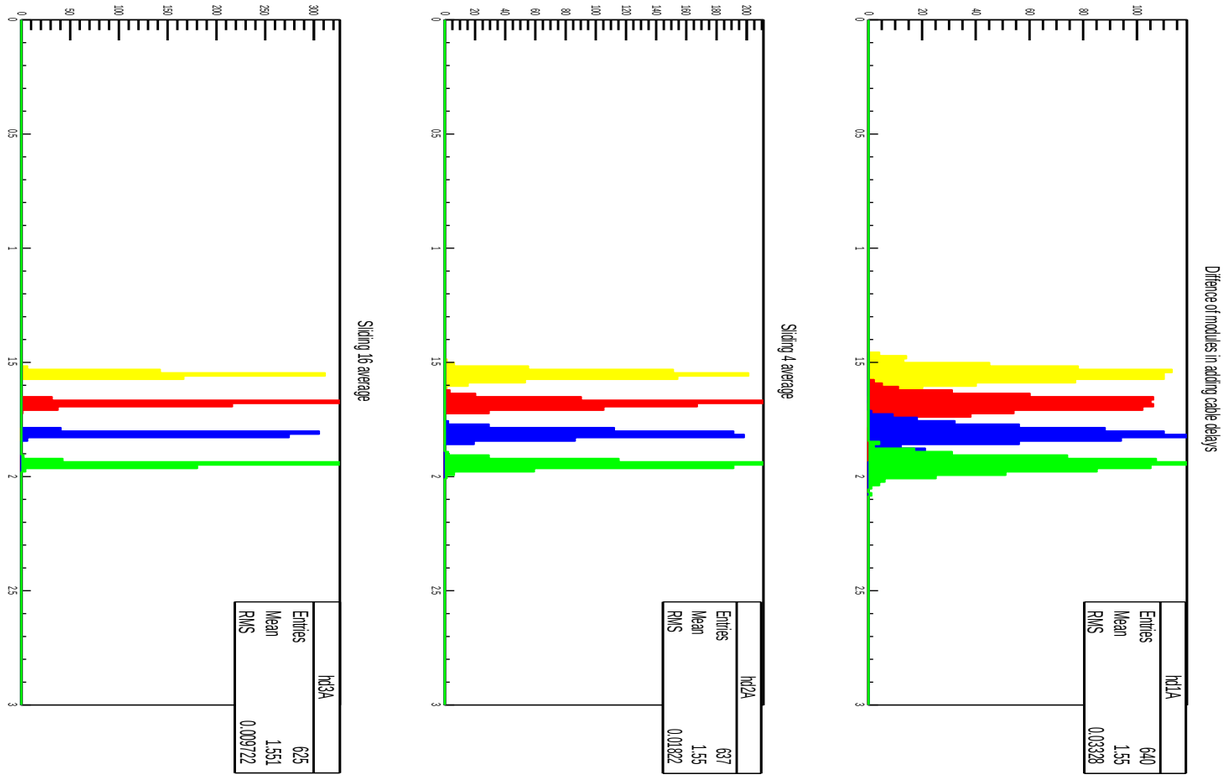




- The histogram shows the difference of the common burst times between two modules five segments apart.
- Timing precision can be further improved by averaging multiple measurements.

Clock Drift Monitoring





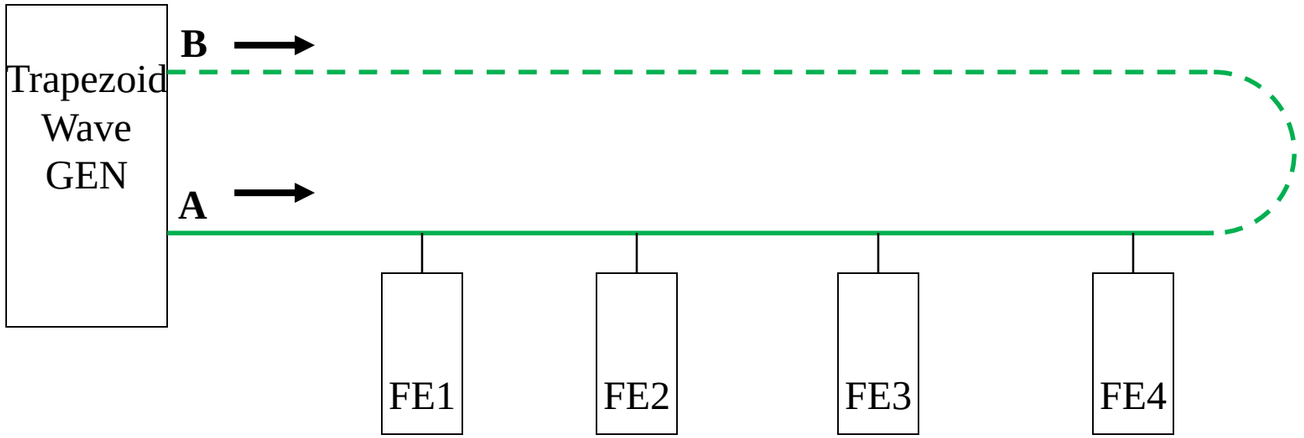
- Artificial clock drift at an FE module is emulated by adding connector unions.
- The connector union delay is 130-140 ps each.
- The clock drift can be monitored with good precision.

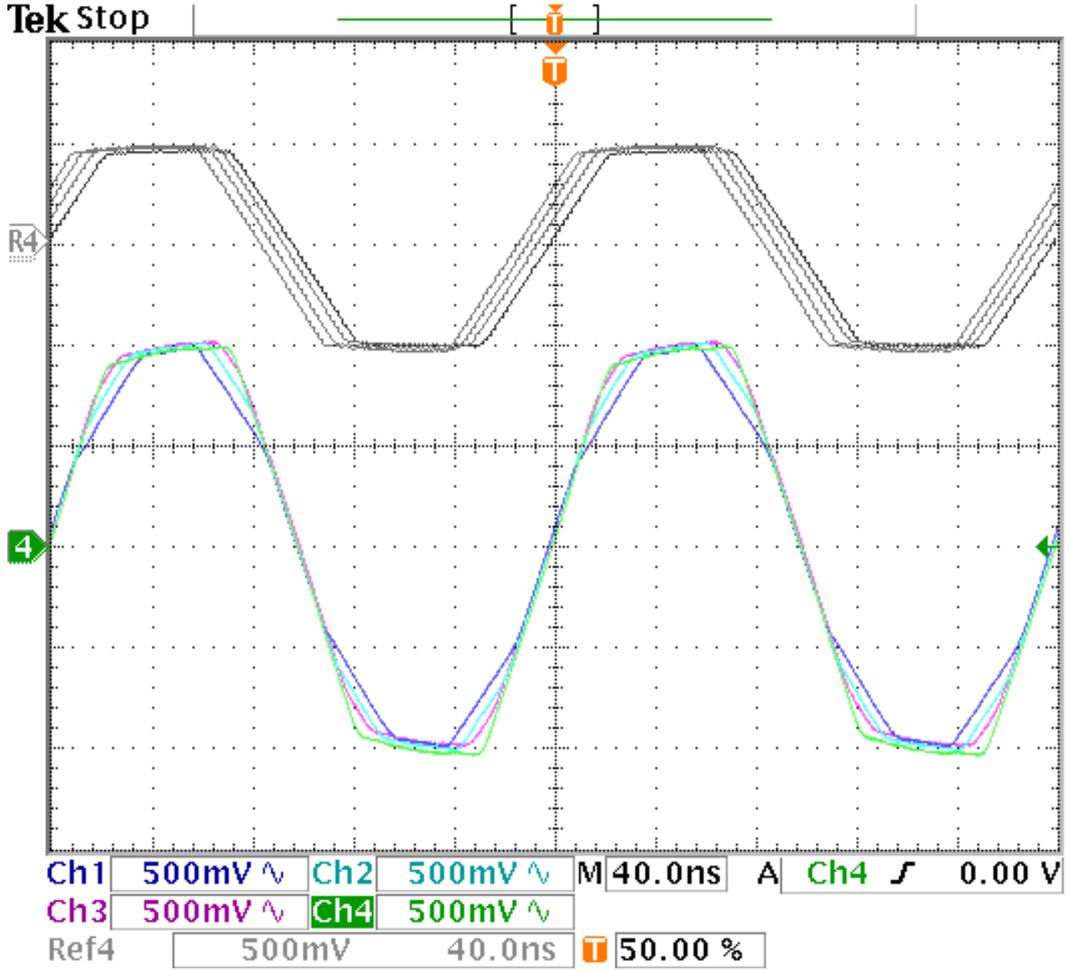
Comments

- This scheme provides a redundant checking/monitoring of the system clock on the front-end modules
- Each FE module only needs to send out pulses synchronized to its system clock.
- Clocks at the front-end module can be monitored with precision good to 10 ps.

The Analog Schemes (Previous Works)

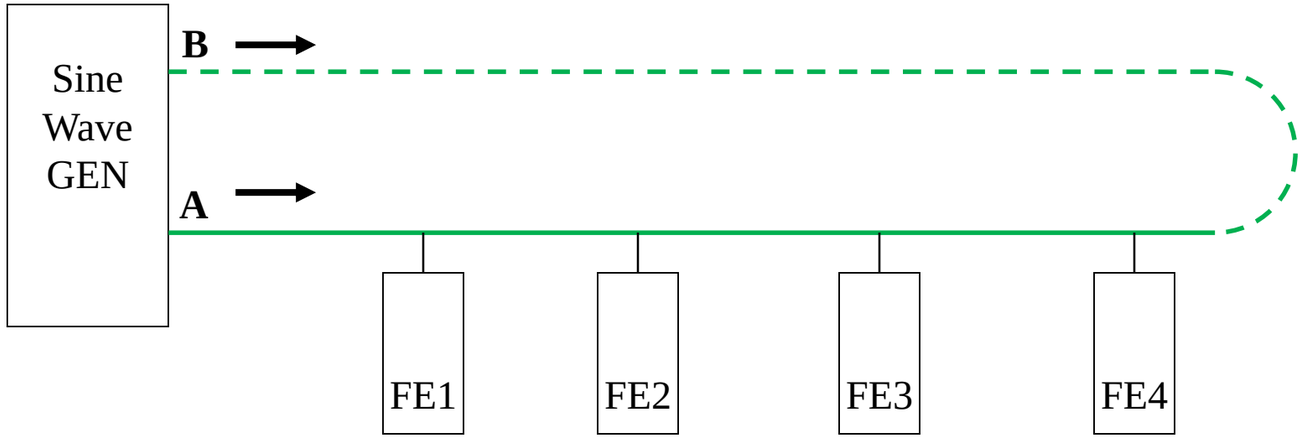
Analog Approach of Clock/Timing Distribution: Trapezoid Clocking

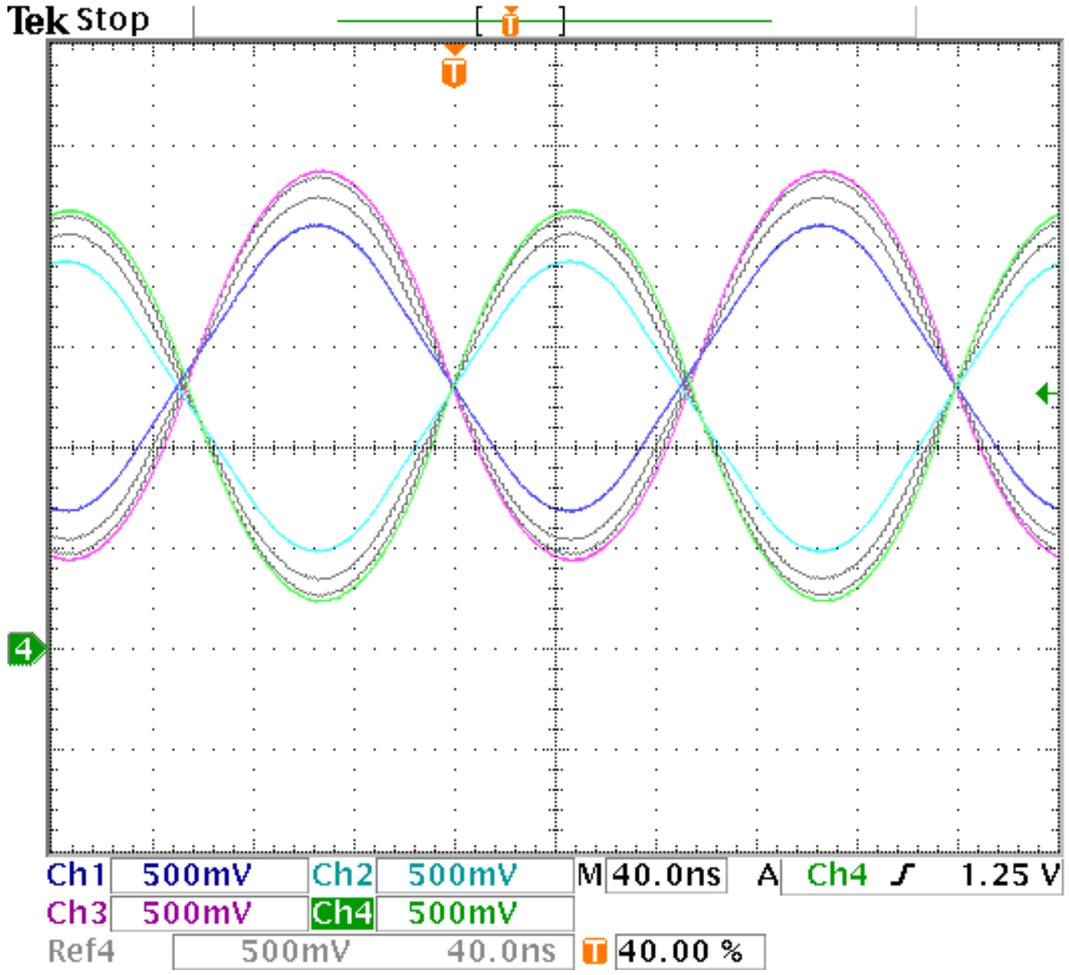




- Trapezoid waveforms are sent from both ends of the cable. (Or send from one end and let it to reflect from the open end)
- Summed voltage crosses zero simultaneously at all taps.

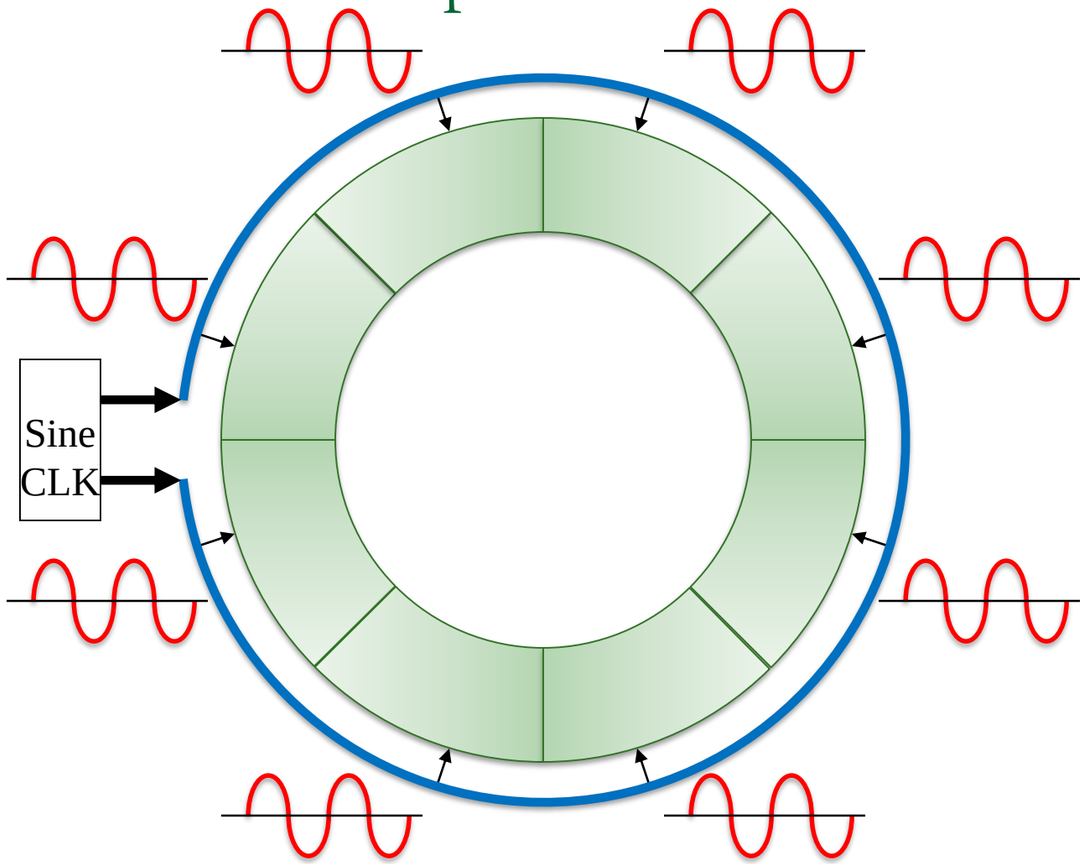
Analog Approach of Clock/Timing Distribution: Sine Wave Clocking

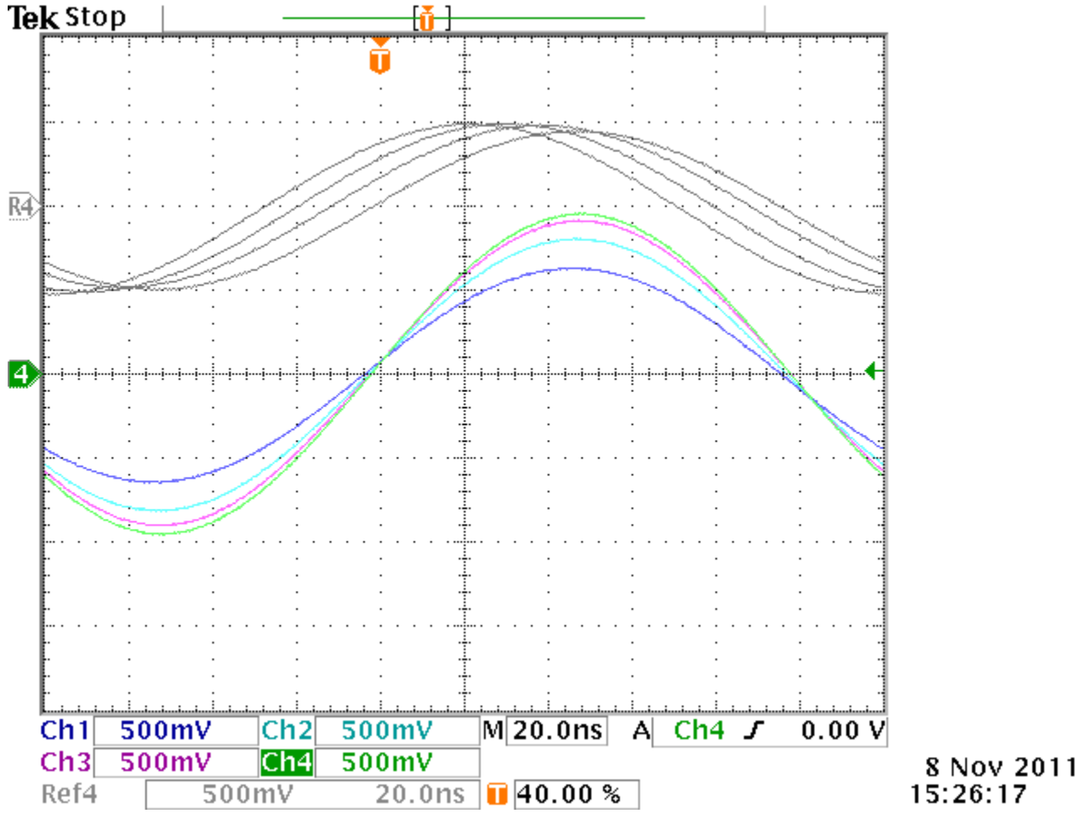




- Sine waveforms are sent from both ends of the cable. (Or send from one end and let it to reflect from the open end)
- Summed voltage crosses zero simultaneously at all taps.

A Possible Simple Clock Distribution Scheme





- When a sine signal is distributed in opposite directions in a cable, all high impedance taps on the cable pick up signals with same zero-crossing time.
- The signals can be used for redundant checking or as system clock to drive PLL directly.
- No delay-matched cables are needed.
- This is suitable for small systems such as TOF PET cameras.

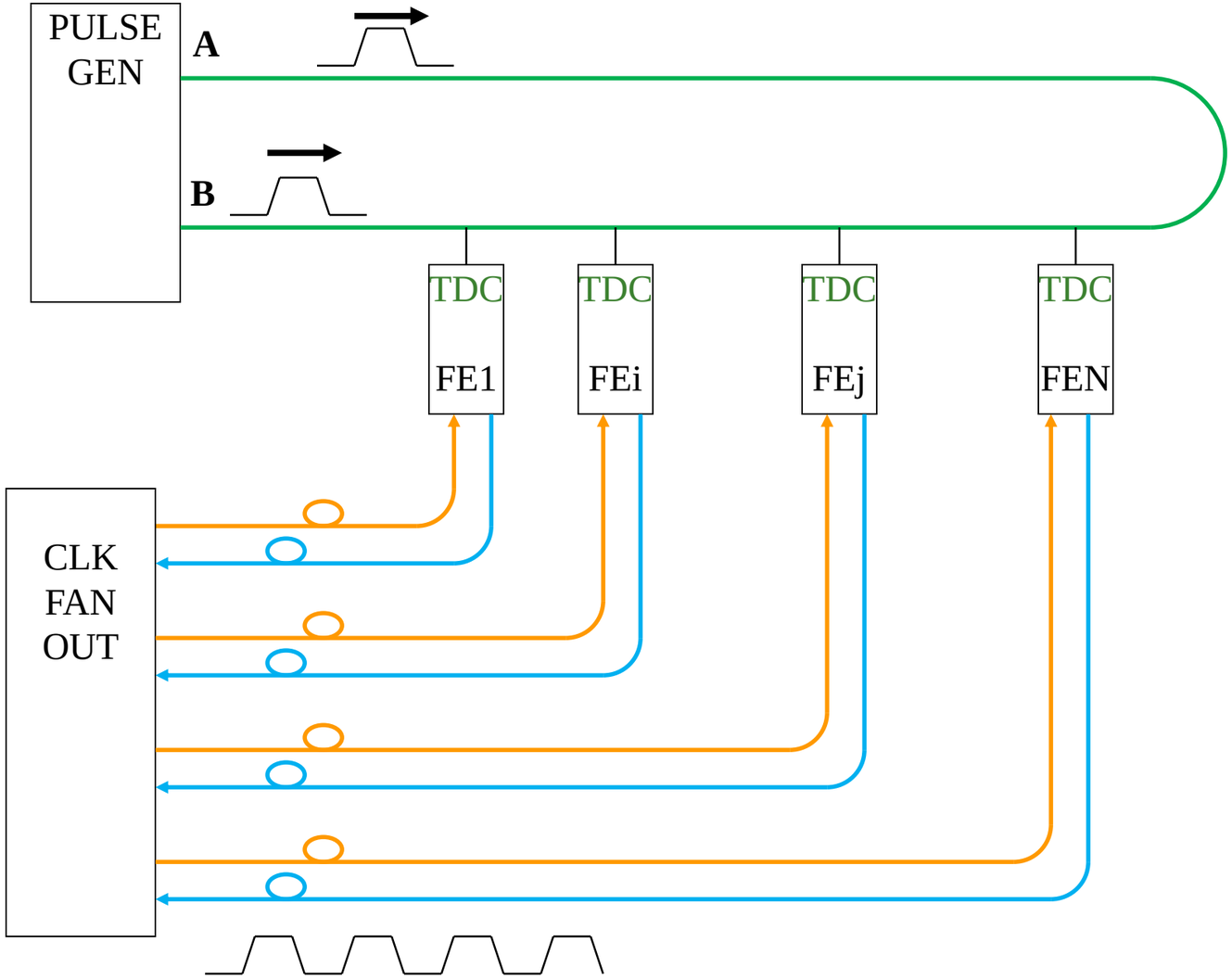
Summary

- The mean timing approach allows users to distribute to check common timing references at the FE modules connected to a cable without delay-matched cables.
- Digitals schemes:
  - TDC at FE modules (and pulsing from cable ends). (Reported 2019)
  - TDC at cable ends (and pulsing from FE modules). (This work)
- Analog schemes:
  - Trapezoid clocking 1: (using trapezoid signal)
  - Trapezoid clocking 2: (using sine signal)

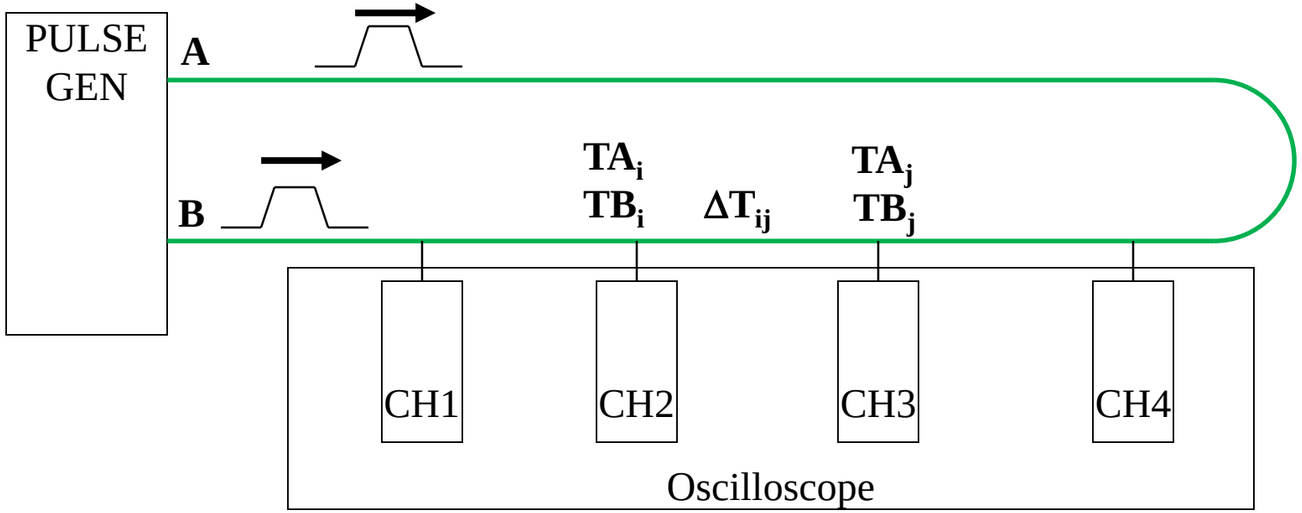
The End

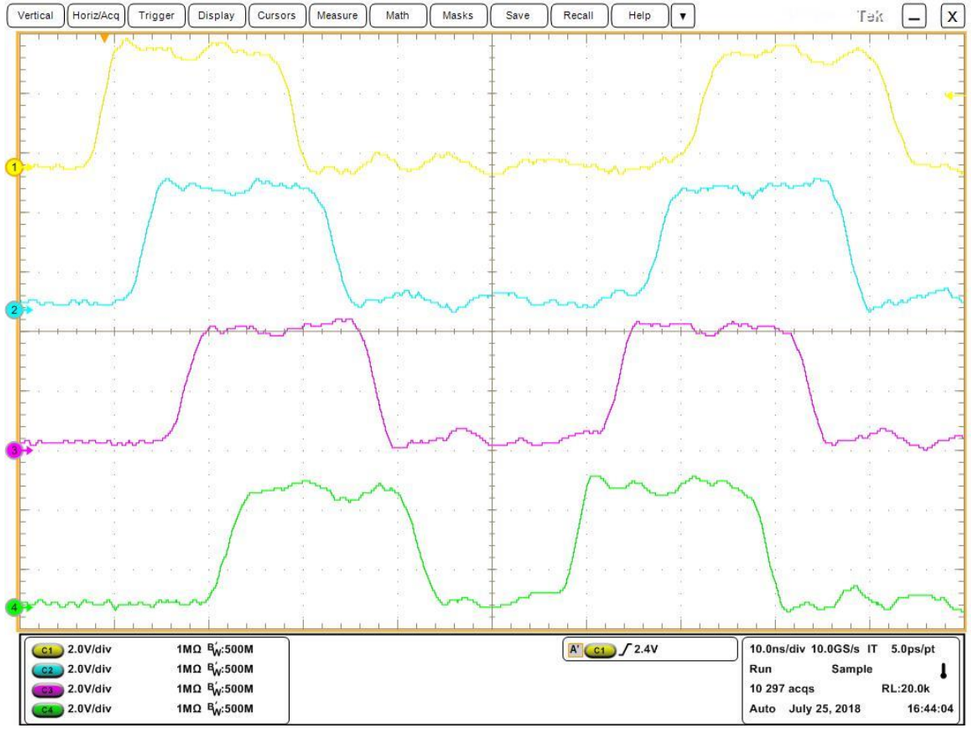
Thanks

Redundant Cross Checking



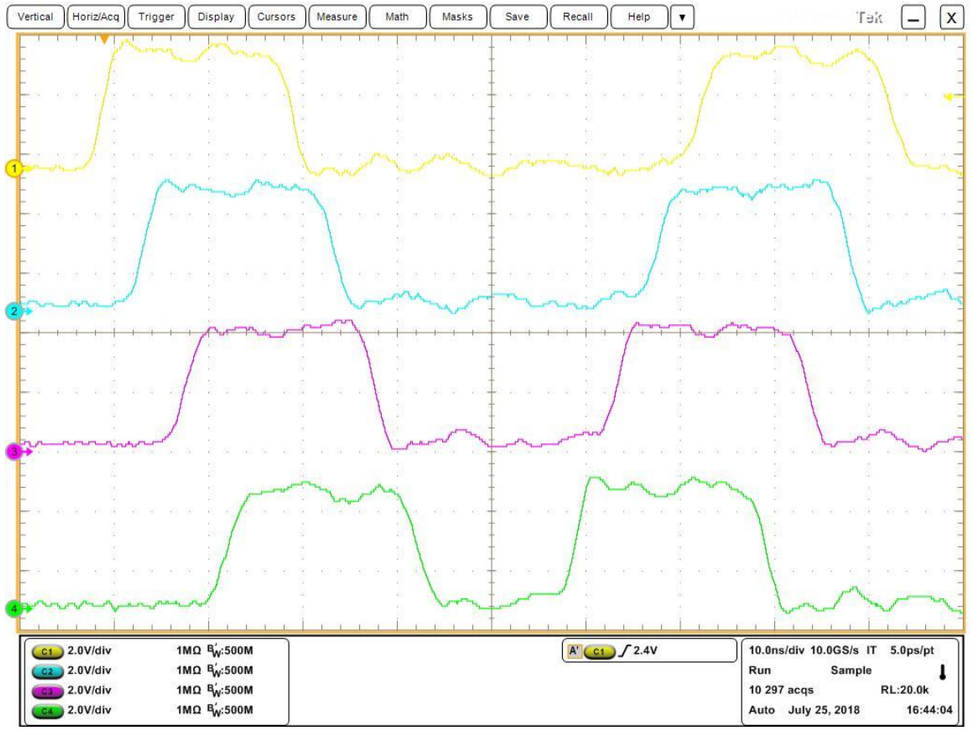
Validation Tests

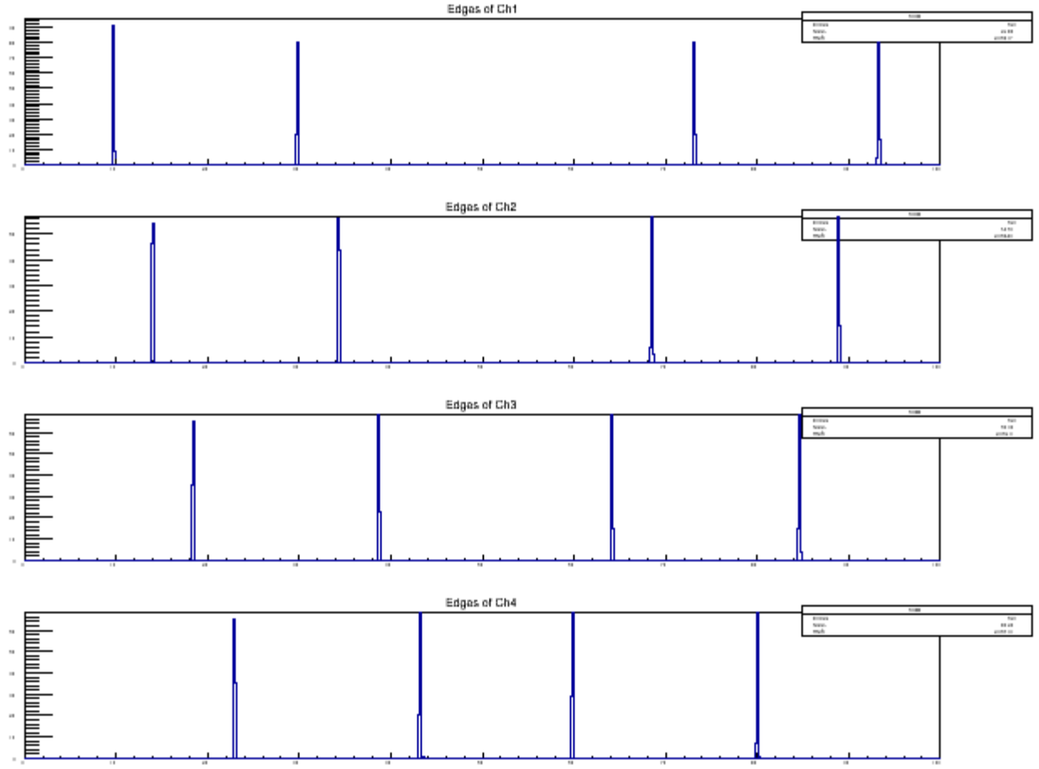




- The common bursts are captured by a digital oscilloscope.
- The 4 input channels in high impedance are daisy chained using BNC TEE connectors.
- The output results are stored in ASCII files.
- The samples at 10 Gs/s are used to emulate TDC channels with 100 ps bin width.

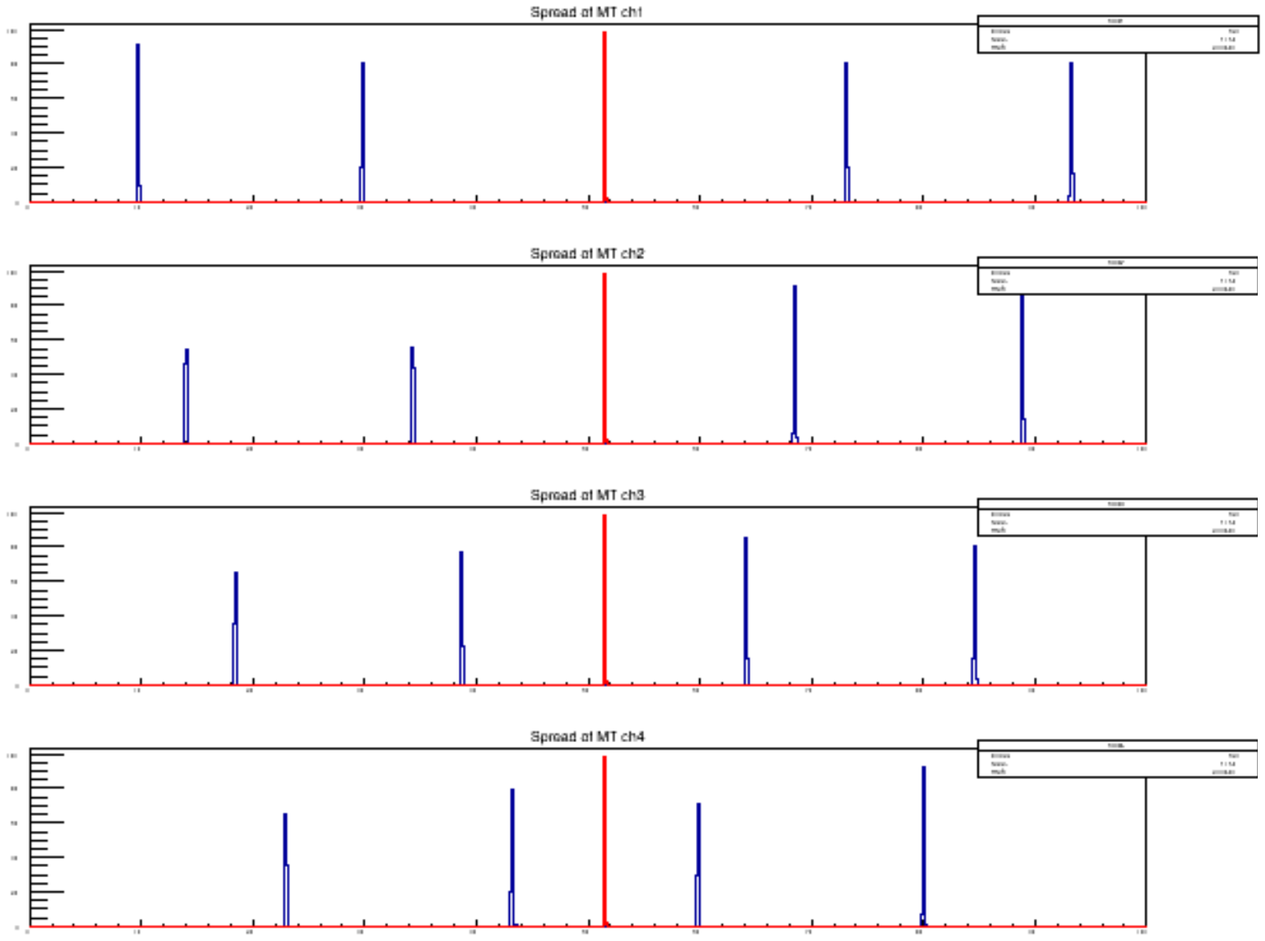
Arrival Times

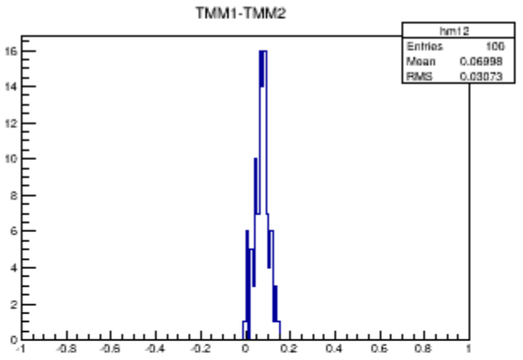


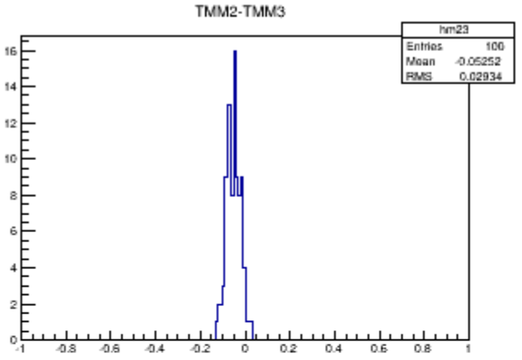


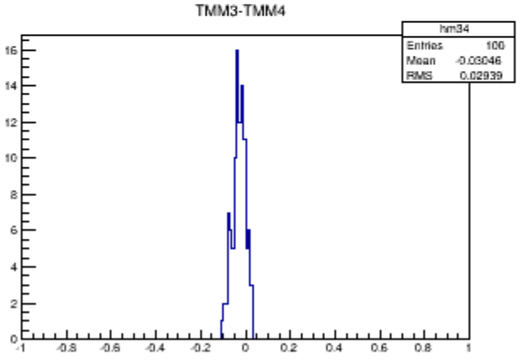
- Both rising and falling edges of the pulses are used.
- Times calculated with 100 ps granularity to emulate TDC (without analog information).
- With both edges, base line shift can be partially cancelled.

The Mean Times



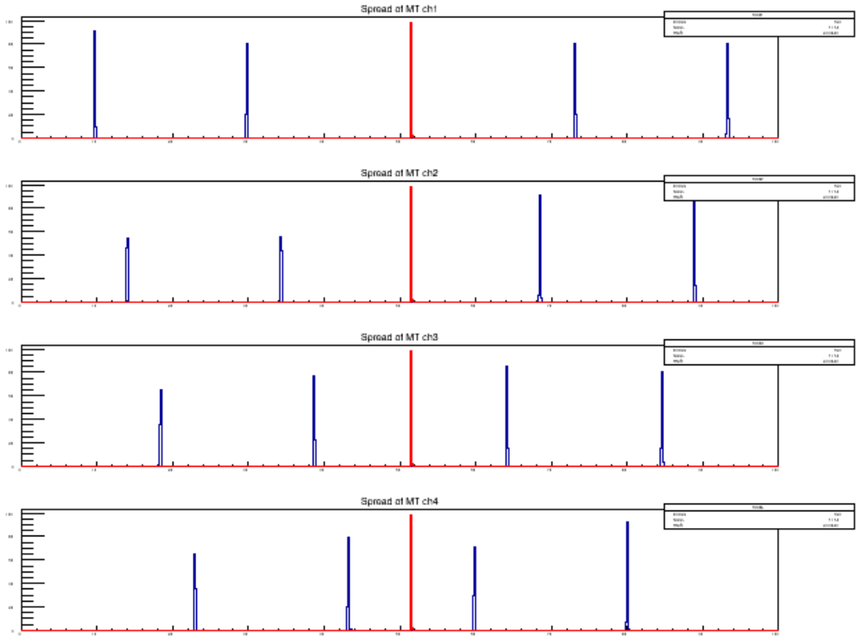


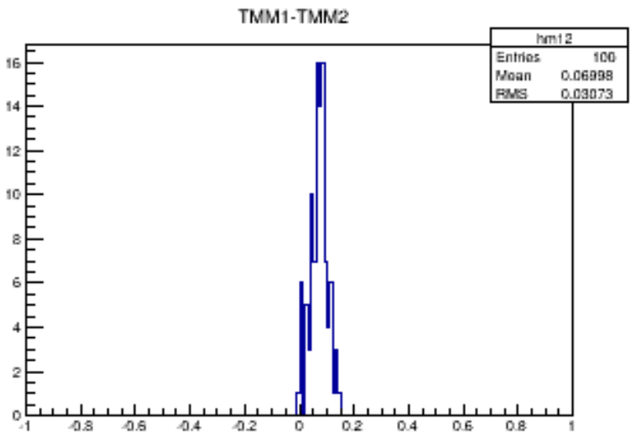


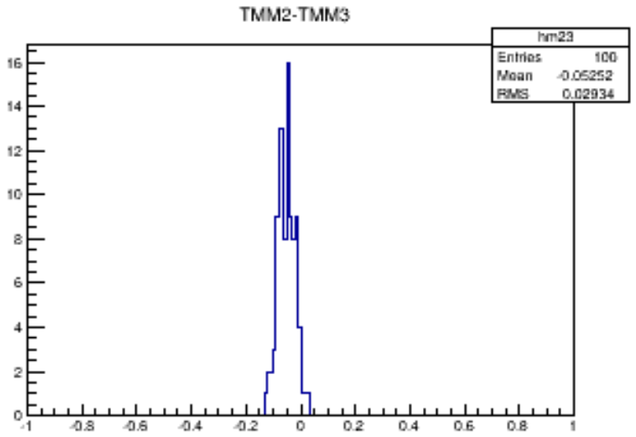


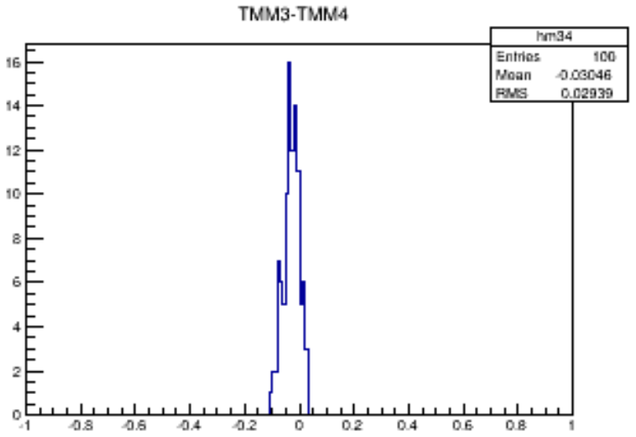
- Mean times using arrival times of 4 edges are calculated.
- The arrival times are different in different channels but the mean times are identical.

The Differences of Mean Times in Different channels





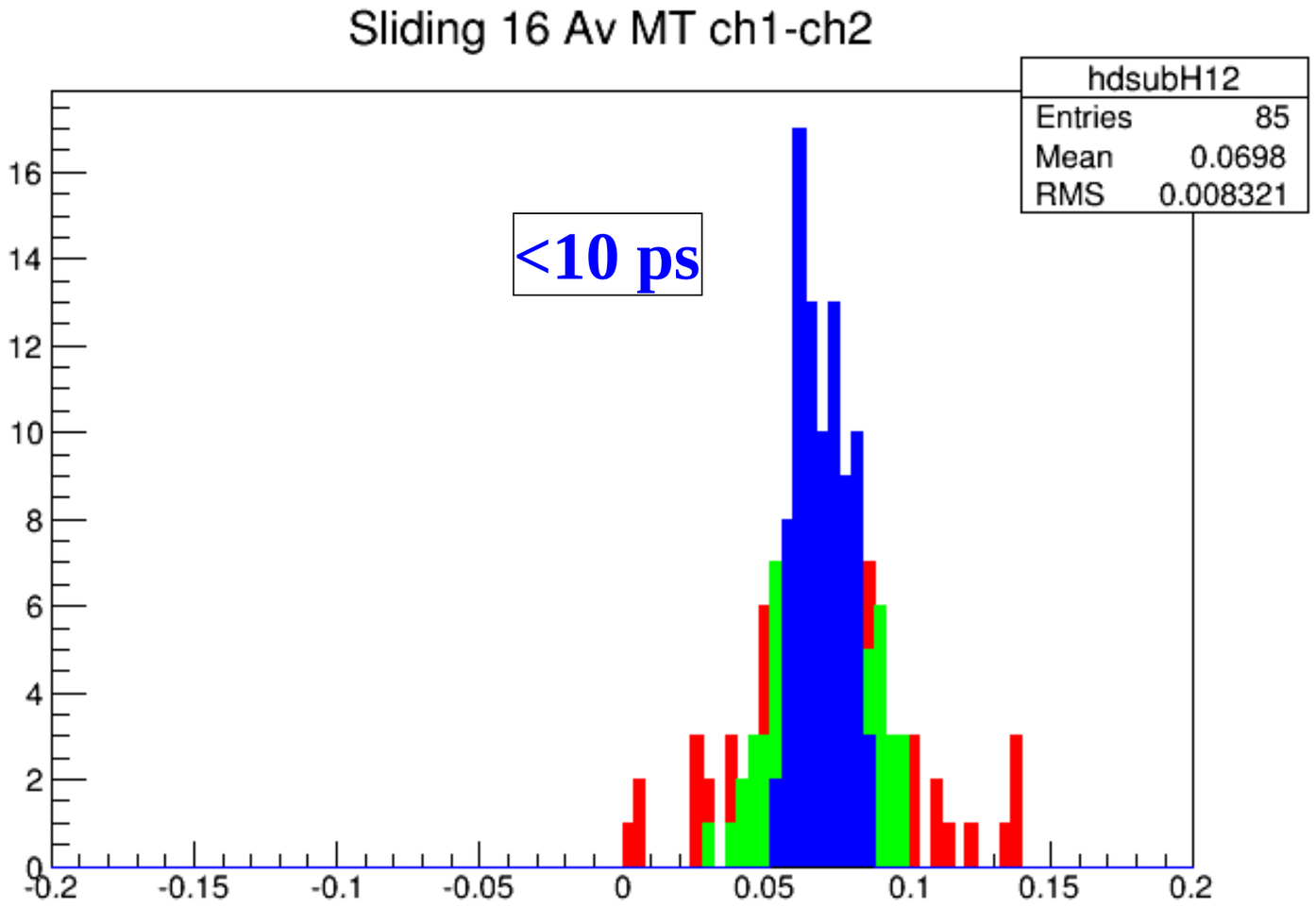




30 ps typ.

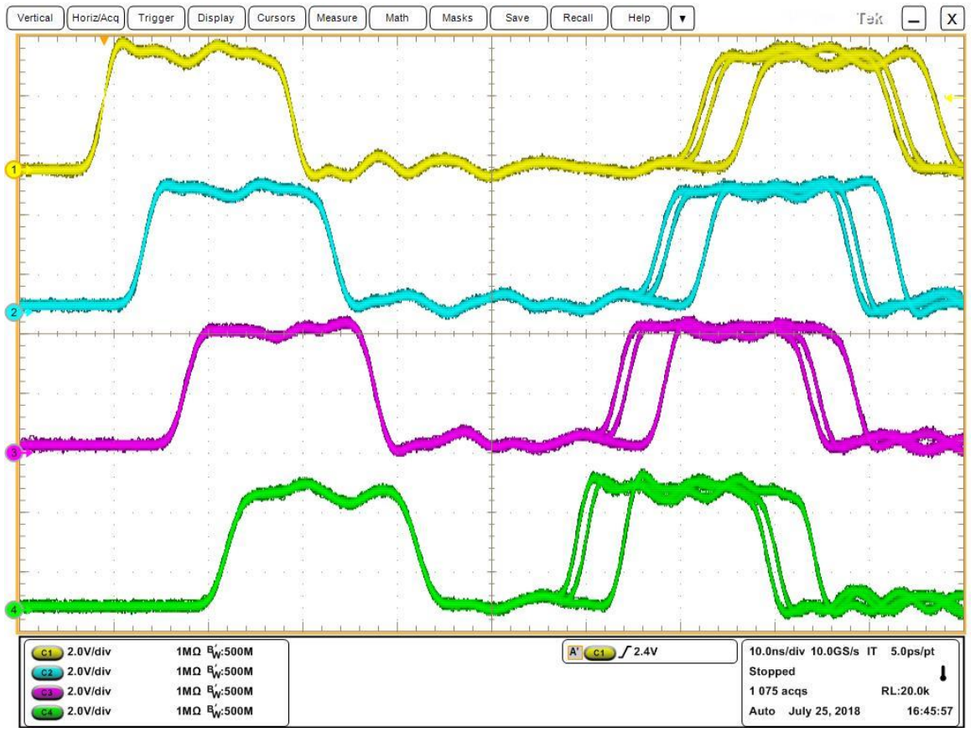
- The measurement precisions for single common burst of different channels are around 30 ps.

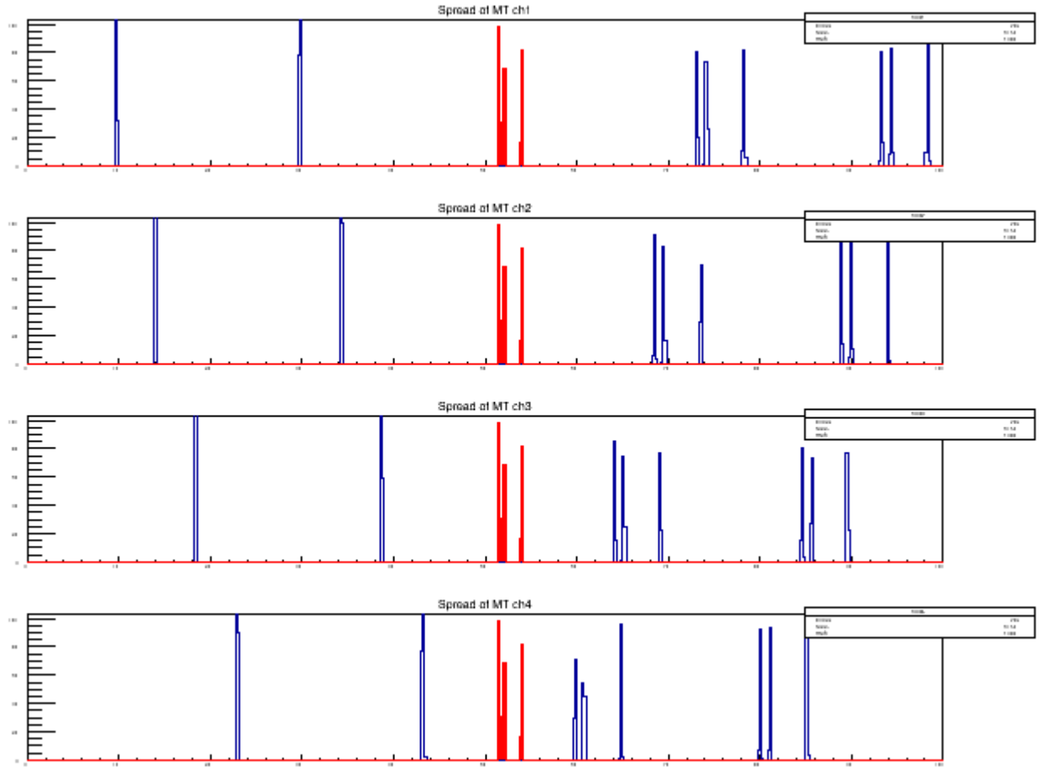
The Average of Multiple Measurements



- The single and sliding averages of 4 and16 mean times are plotted above.
- With repeating measurements, the monitoring precisions better than 10 ps can be achieved.

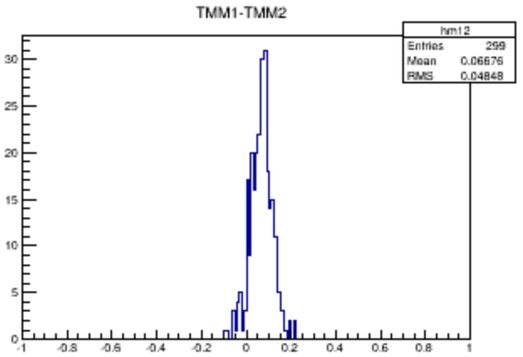
Cable Delay Effects

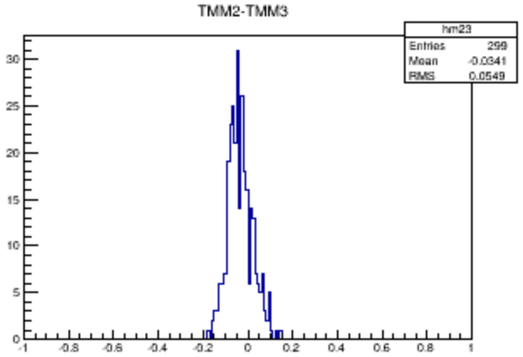


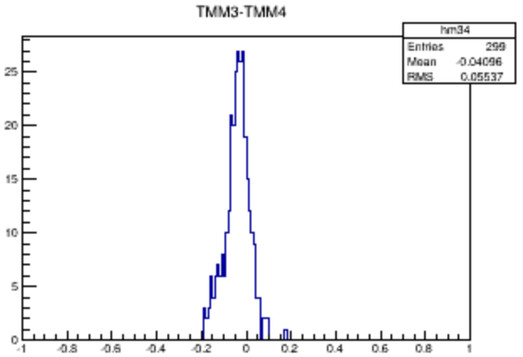


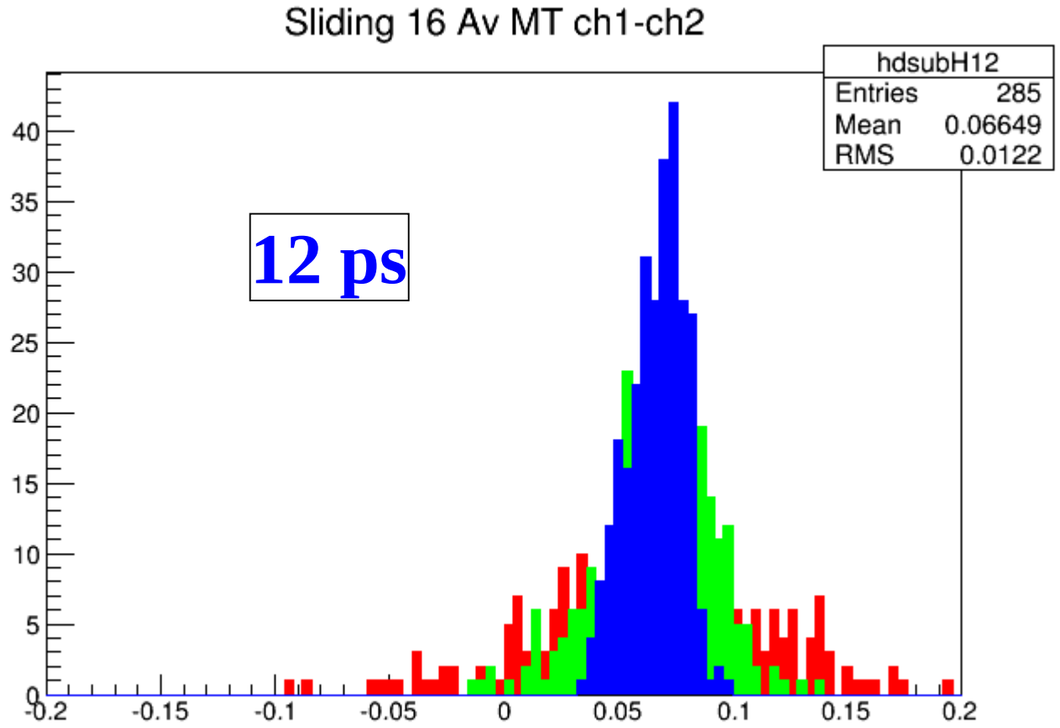
- Artificial delays are added in the signal generator pulses to emulate cable delay variations.
- Arrival times are changed accordingly.
- Mean times are also changed, but all channels have same amount of change.

Differences of Mean Times in Different Channels









- The mean times are still identical in different channels within good precisions.