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Data Acquisition and Signal Processing for the Gamma Ray Energy Tracking Array (GRETA)

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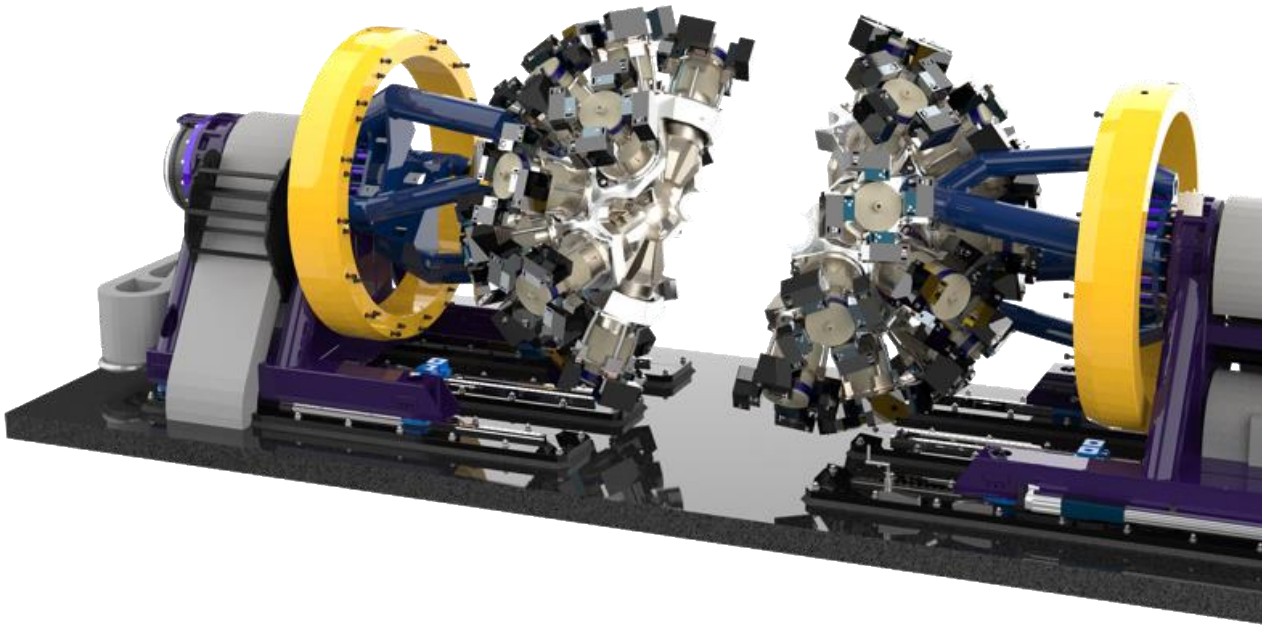
Real Time Conference 2020



Outline

01

Introduction to the GRETA Detector System

02

The GRETA Data Acquisition Hardware

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The GRETA Status and Performance

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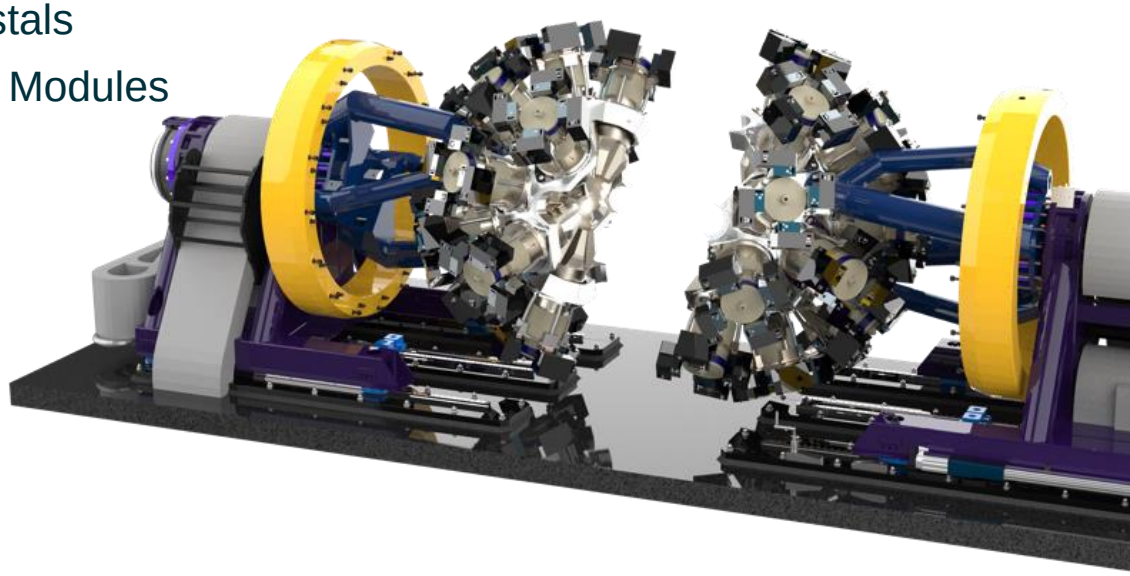
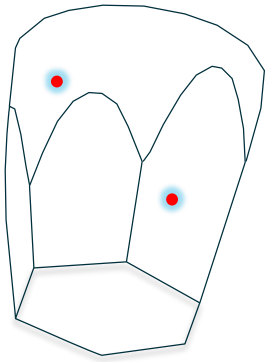
Summary

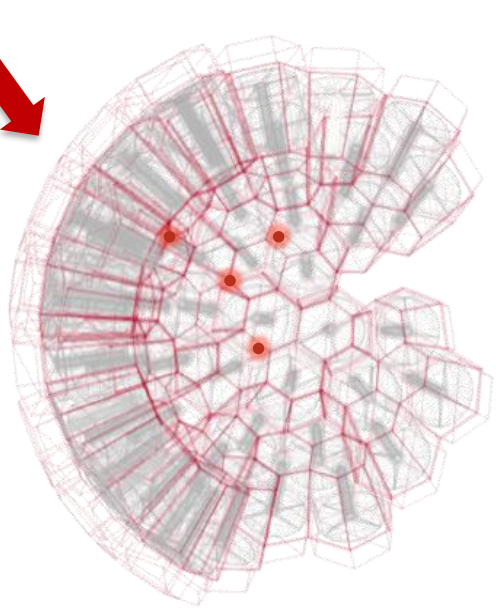
The GRETA Detector

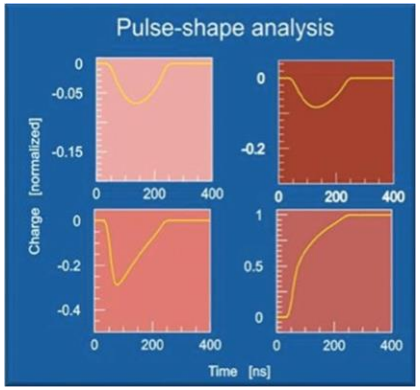
- Full 4π coverage of γ-ray tracking detector
  - Identify the position and energy of γ-ray interaction points within a compact “shell” of detectors
  - Gamma Ray spectroscopy
- Electronics, Computing and Mechanical Systems to support the 30 Detector Modules
- Movable Detector for use at different experimental sites
- Combines highly segmented, hyper-pure germanium crystals with real time digital signal processing techniques
  - 120 Segmented germanium crystals
  - Arranged into 30 Quad Detector Modules

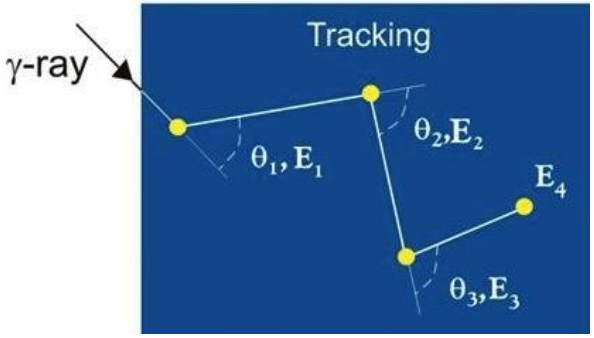


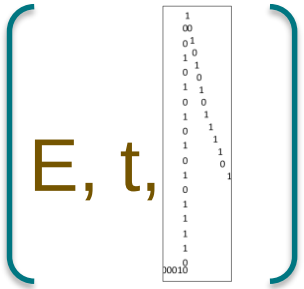
The GRETA Data

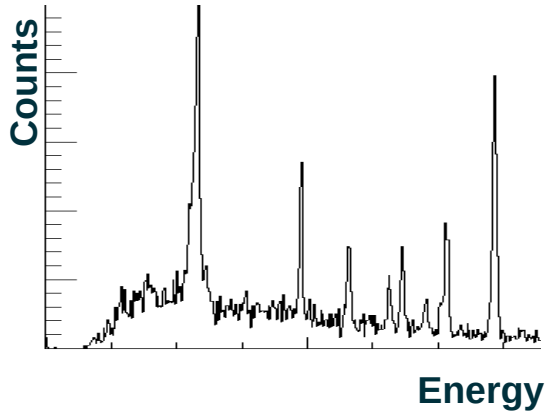




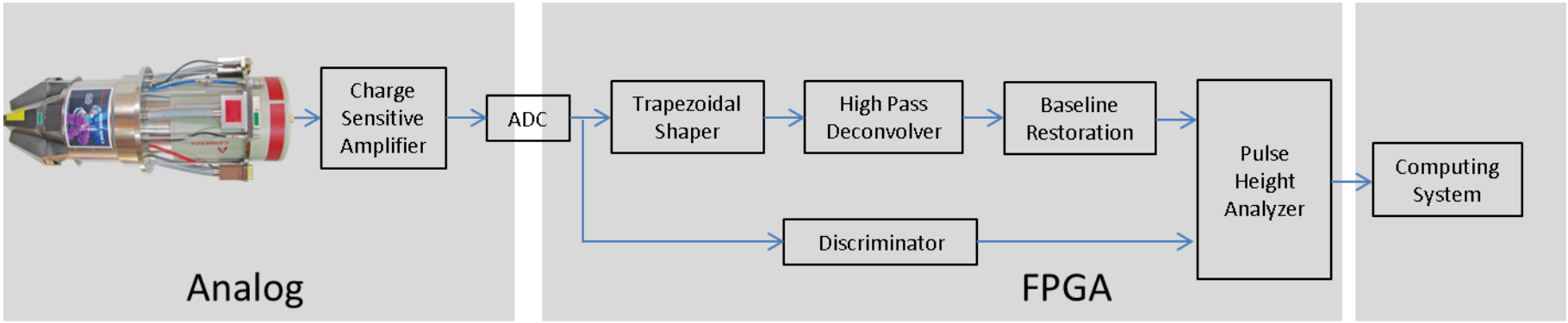








The High Level GRETA Data Acquisition Real Time Processing



- Analog
  - FET preamplifier
  - Charge sensitive with resistor bleeder

- FPGA
  - Shaping (Trapezoidal)
  - Pole-Zero Correction (High Pass Deconvolver)
  - Energy Finder
  - Data packer

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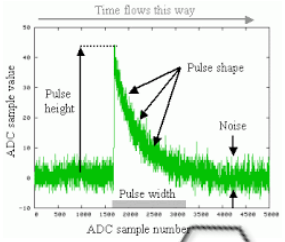
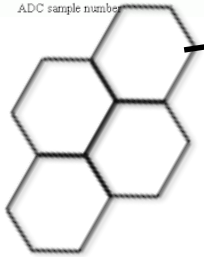
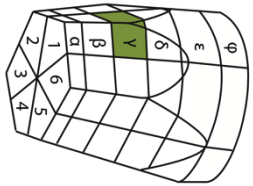
Summary

The GRETA Data Acquisition Hardware Blocks





Quad Detector



Detector Interface Box (DIB)

Digitizer Module (DM)

~100Gb/s

DM
DM
DM

Signal Filter Board (SFB)

25GbE

Network Switch

Computing Systems

Forward Buffers

10GbE

Trigger Routers

Timing Module

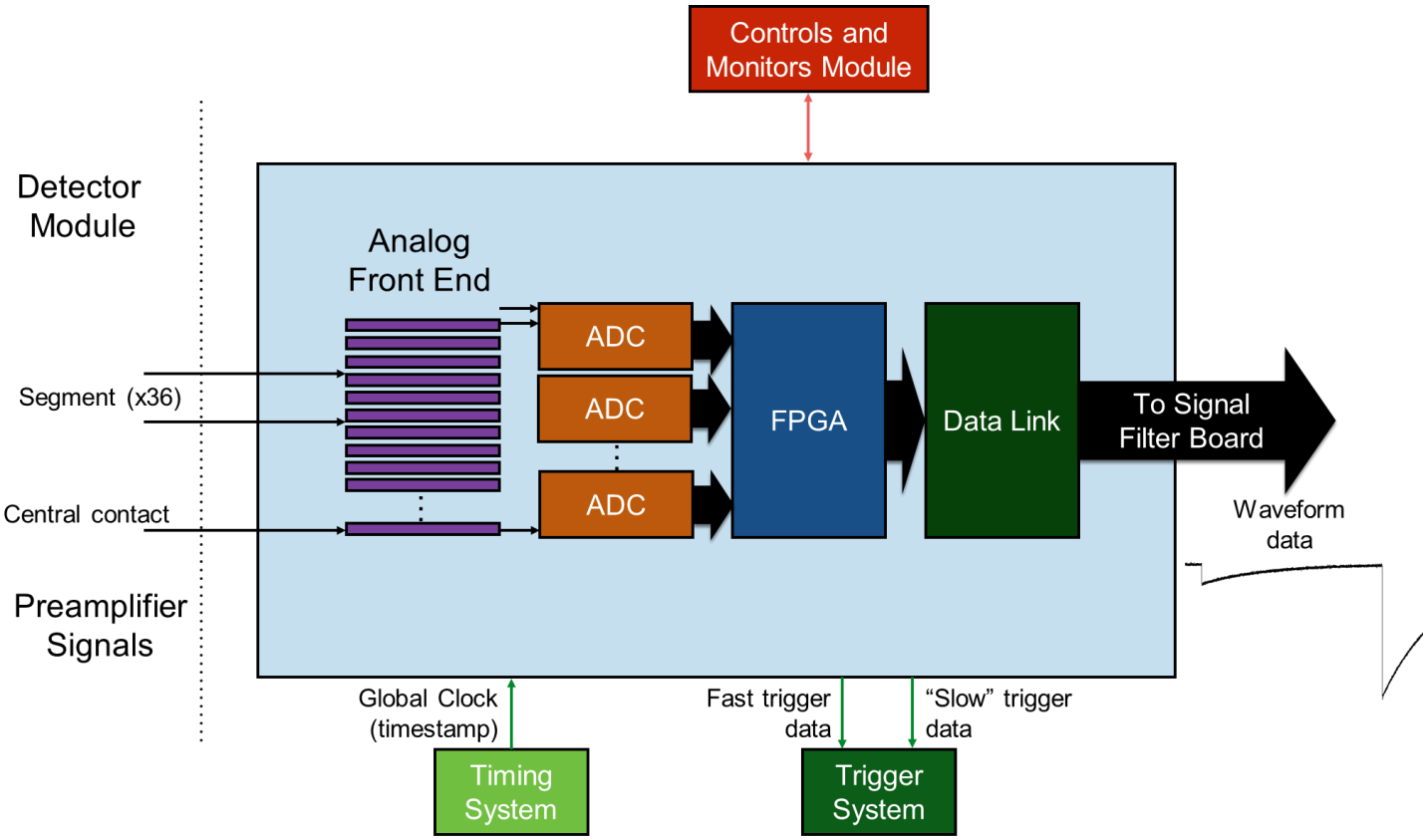
Master Trigger

GbE

Slow Control and Monitoring Module

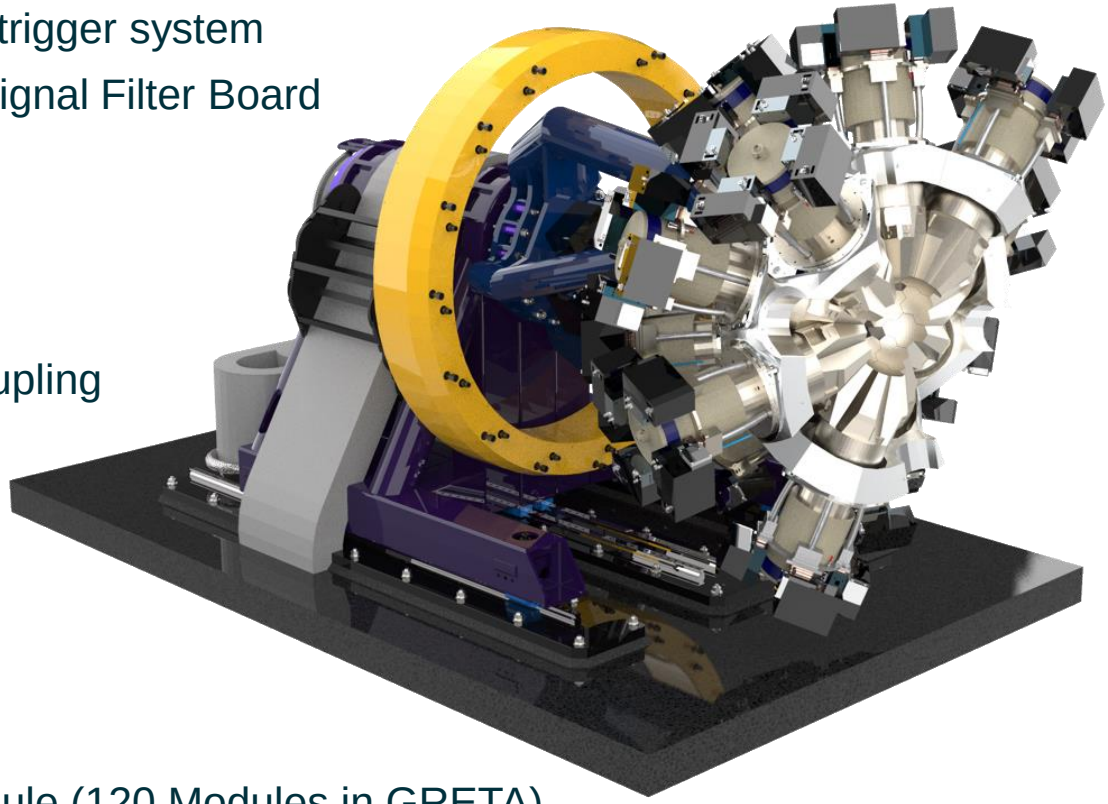
External Detectors / Accelerator Clocks

The Digitizer Module



The Digitizer Module

- Function
  - Ensure best digitization of the detector signals
  - Timestamp the digital data
  - Provide fast trigger data to the trigger system
  - Transmit digitized data to the Signal Filter Board
    - 10x ~10Gb/s

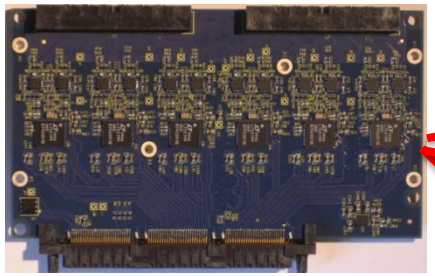


- Mounted on the Detector
  - Ensures least signal loss or coupling
  - One per germanium crystal

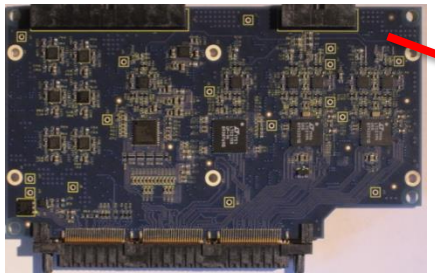
- ADC is key to the performance
  - 100MSample/s
  - 16bit
  - 40 ADC channels/Digitizer Module (120 Modules in GRETA)

The Digitizer Module ADC Cards

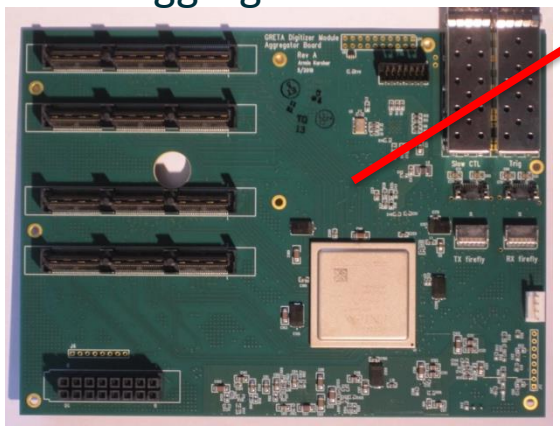
Segment ADC

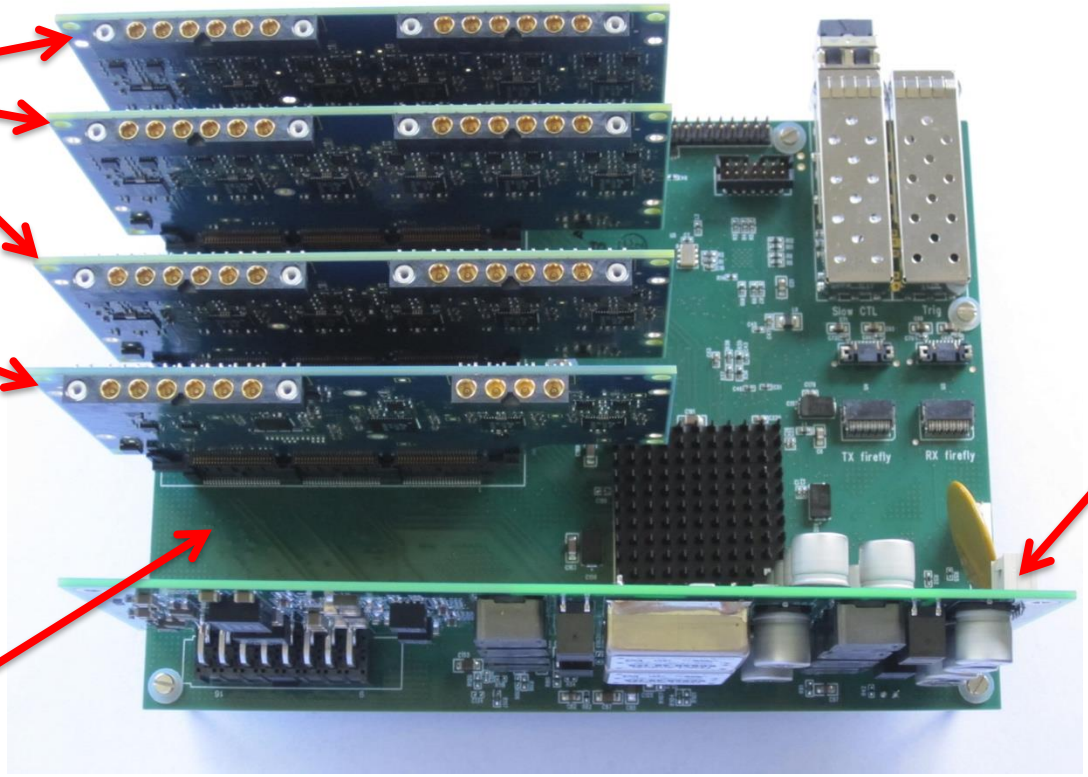


Core Contact ADC



Aggregator

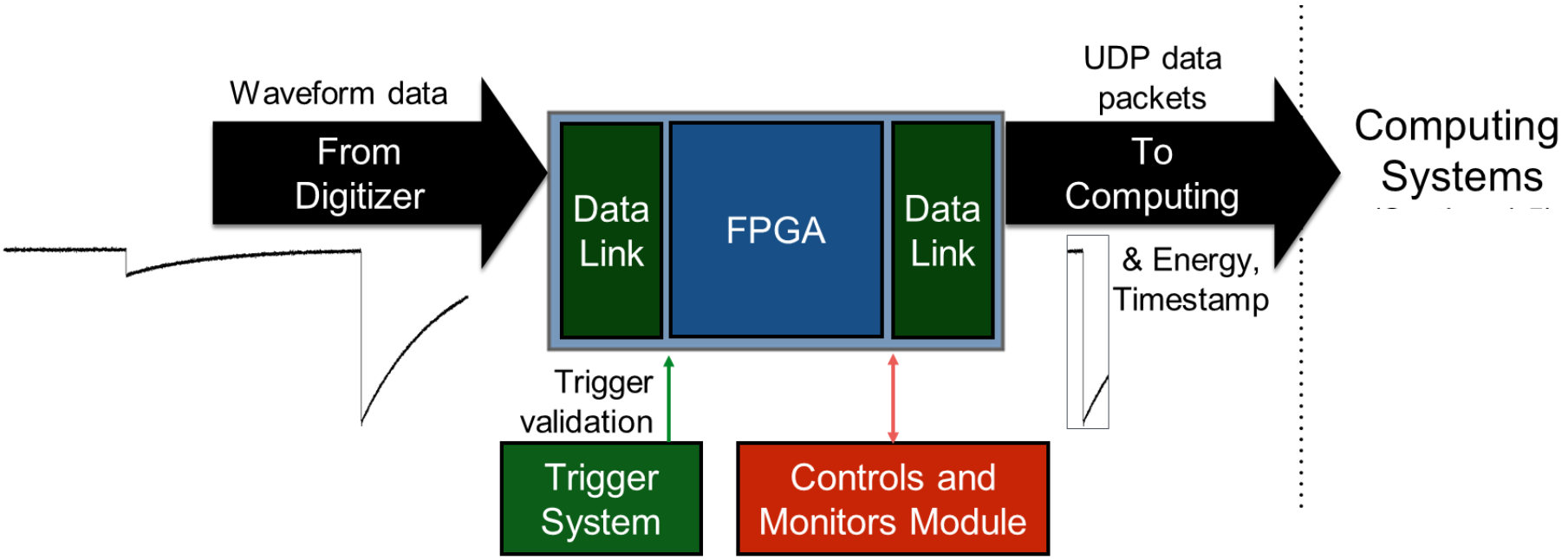




Digitizer Module Assembly - Internal Boards

Power Board

The Signal Filter Board



The Signal Filter Board Hardware

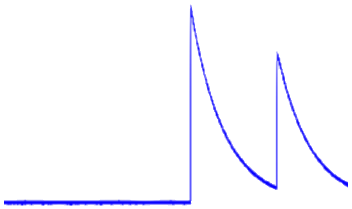
- The real time digital signal processing of the Electronics DAQ chain
- Commercial of the shelf hardware
  - Easy upgrade
- Function
  - Receive ADC Data from 4 Crystals / Digitizer Modules
    - 4 * (10 * ~10GB/s)
  - Highly parallel real time signal processing
    - Extract 

 from all ADC channels for γ-rays
  - Package γ-ray data for triggered events
  - Transmit data to computing
    - 25Gb Ethernet

The Signal Filter Board Processing

- Real-time digital processing of detector ADC data
  - Highly Parallel
    - 4 Digitizer Modules * 40 ADC Channels

- The GRETA Filter Algorithms
  - LED Leading Edge Discriminator
  - Trapezoidal Filter
  - Pole-Zero Cancelation
  - Baseline Restoration
  - Energy Determination



Leading Edge Discrimination

$y(n)=x(n) - x(n-k)$ (differentiation)

$y(n)=(x(n) + x(n-2)) + x(n-1)<<1$ ($\times$4, Gaussian filtering)

Threshold comparison $\rightarrow$ LE discriminator time

Constant Fraction Discrimination

$y(n)=x(n) - x(n-k)$ (differentiation)

$y(n)=(x(n) + x(n-2)) + x(n-1)<<1$ ($\times$2, Gaussian filtering)

$y(n)=x(n-k)<<ab - x(n)$ (constant fraction)

Zero crossing comparison $\rightarrow$ CFD time

Trapezoidal filter and energy determination

$y(n)=y(n-1) + ((x(n) + x(n-2m-k)) - (x(n-m) + x(n-m-k))$

Maximum tracking $\rightarrow$ energy

Pole-Zero cancellation

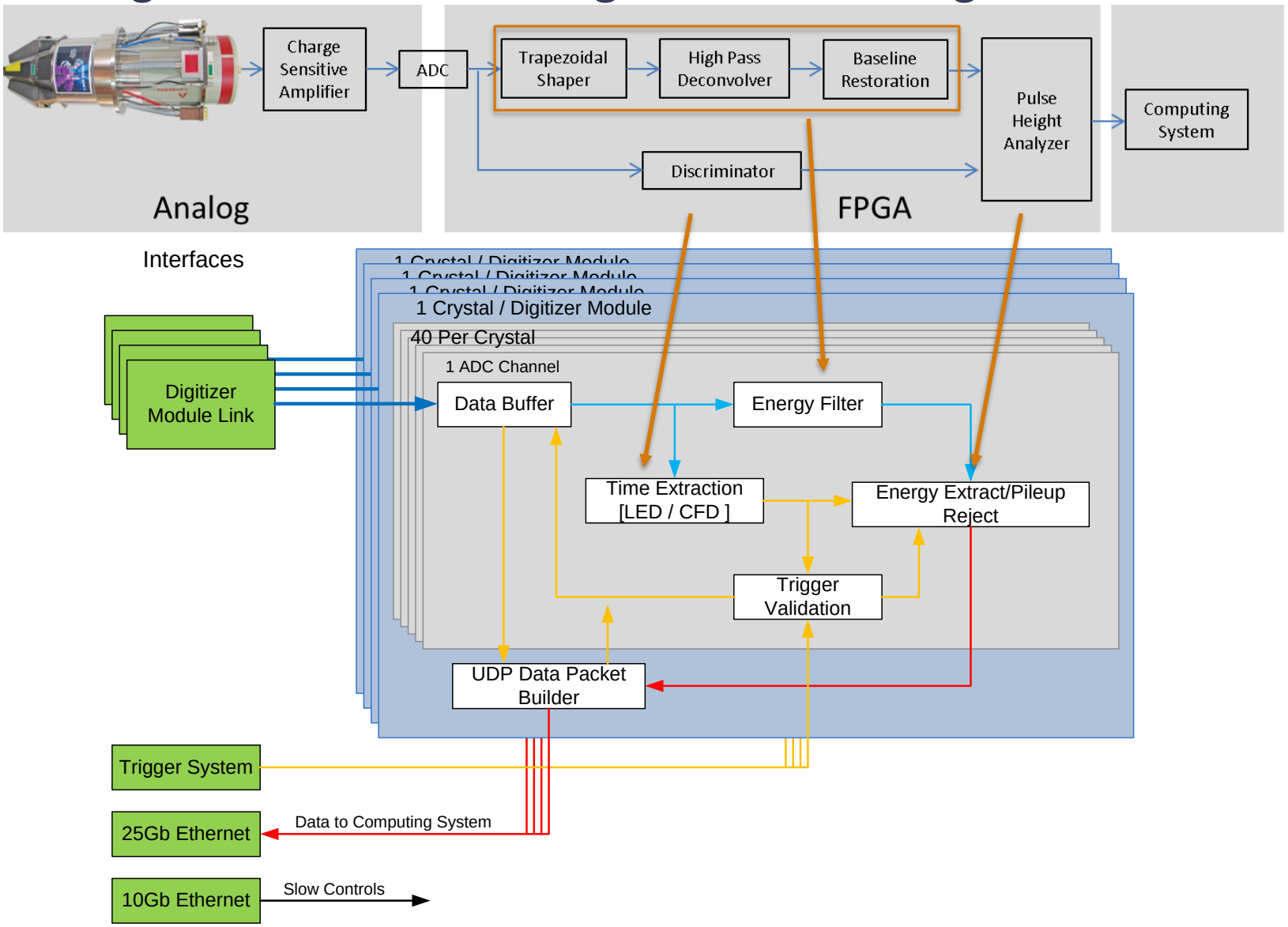
$I(n)=I(n-1) + x(n)$

$y(n)=x(n) + I(n)/t$ (where t is the pre-amp time constant)

Baseline Restoration

y(n)=BLR*y(n-1) + x(n) ($\times$2)

The Signal Filter Board Signal Processing



The Signal Filter Board to Computing Interface

- Ethernet interface
  - 25Gb Ethernet 25GBASE-SR
  - Jumbo frames
  - UDP data protocol
    - 64kB UDP packets

- No data retransmission
  - Data format can detect lost packets to account for in the analysis

- Streaming of data to computing
  - Flow control through the trigger system

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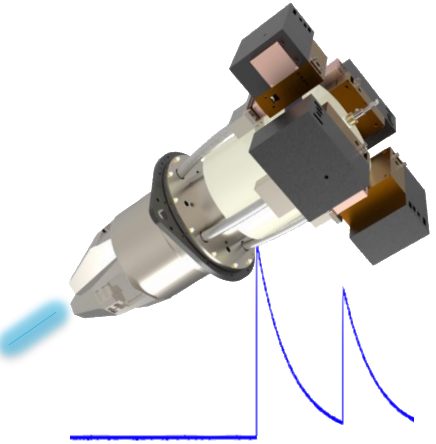
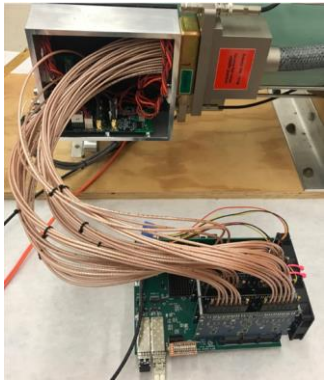
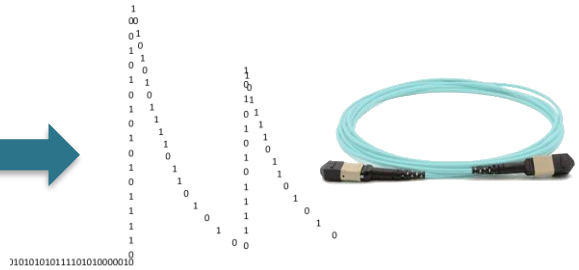
The GRETA Status

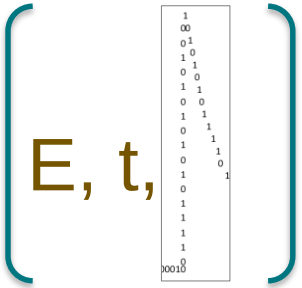
- Design of the real time data acquisition hardware is complete
- Signal processing implemented to demonstrate functionality and performance
- Prototypes demonstrated the performance
  - Energy resolution







- Continuous 100MHz digitization of **40** preamplifier signals **per crystal**

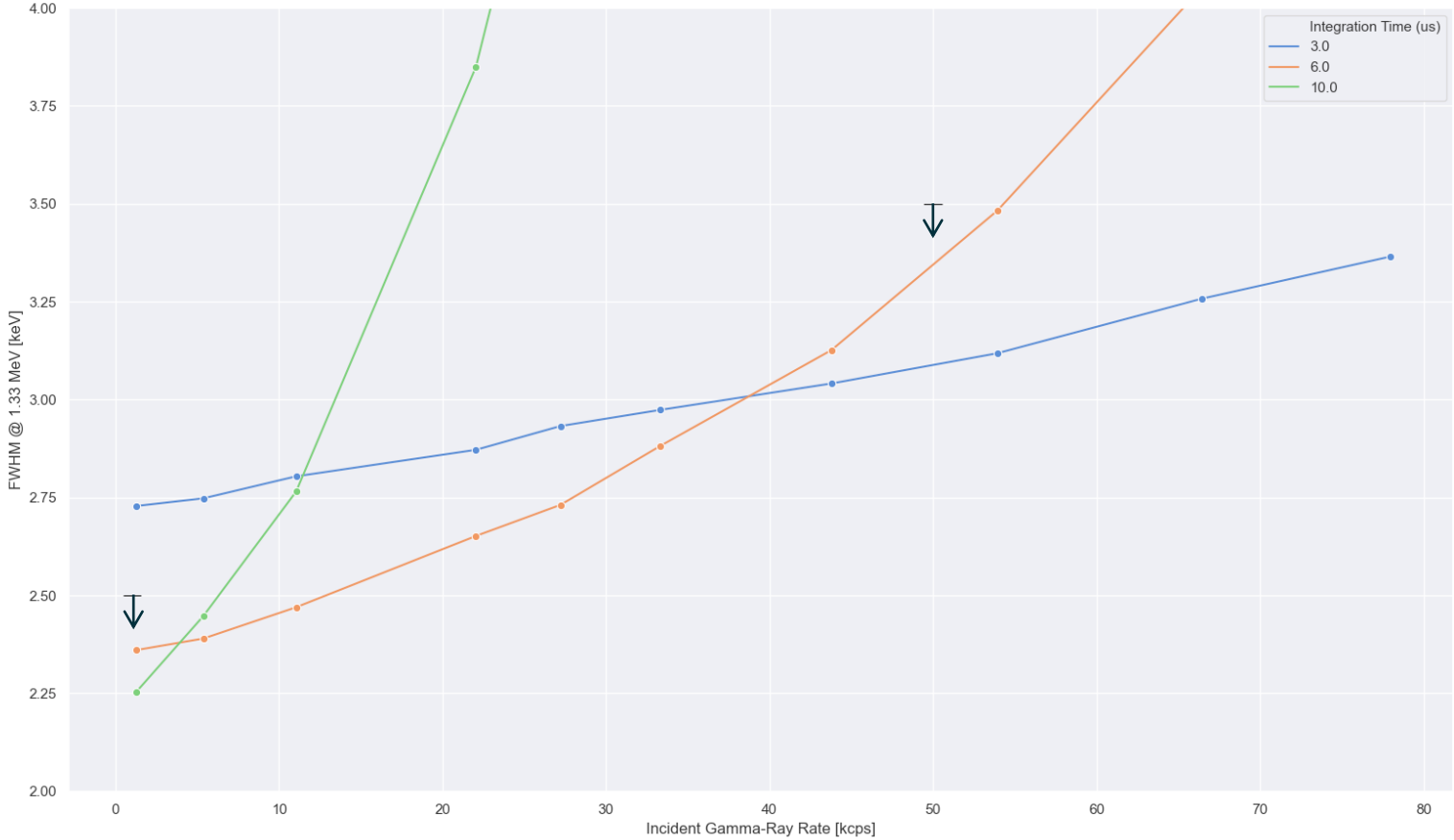


x 40

- FPGA-based energy filters

The GRETA DAQ Electronics Performance

- Required Range: 0-10 MeV
- Resolution at 1kHz incident rate: <= 1.4 keV at 60 keV, <= 2.5 keV at 1.33 MeV
- Resolution at 50kHz incident rate: <= 3.5 keV at 1.33 MeV



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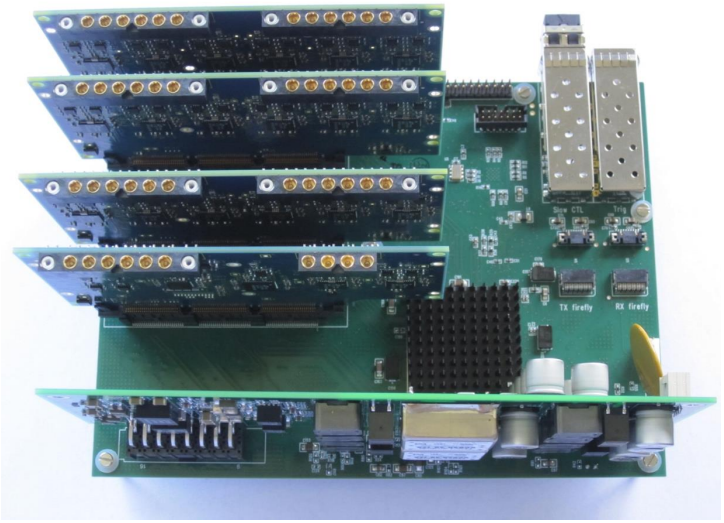
The Summary

- Design of the real time data acquisition hardware is complete
- Signal processing implemented to demonstrate functionality and performance
- Prototypes meet requirements
- Started production phase
  - Build and test full complement of Data Acquisition Hardware
  - Finish full firmware functionality



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Thank You