## **Novel Digital Camera with the PCIe Interface**

#### Introduction

Diagnostic systems of the ITER tokamak require use of more than 200 digital cameras working in the visible, infrared, and gamma radiation range. Tokamak vision systems should allow for image acquisition and processing with the resolution to 8 million pixels of 1 registered within the range of



50 to 50000 frames per second. For example, a digital 8-bit camera with a resolution of 1 megapixel working with a frame rate of 1000 frames per second generates a stream of data not less than 8 Gb/s. In this situation, the tokamak image acquisition system, which provides a stream of data from 10 cameras, requires a data throughput of at least 80 Gb/s.



The standard approach (found in CoaXPress, Camera Link, CLHS, ...)

- the camera interfaces the host through frame grabber
- the data is buffered three times
- COTS frame-grabbers can only transfer the data to the host RAM
- throughput is limited by the frame grabber interfaces
- precision timestamping is often not possible

## **D. Makowski, A. Mielczarek**, Lodz University of Technology, Poland

### **Throughput & Latency**



The new approach

- no unnecessary data buffering much lower latency
- data transfers directly to GPU are possible
- scalable throughput, limited mostly by sensor performance
- much easier camera control, using native register interface
- possibility of standardization of the firmware upgrade of the camera
- timestamping is still hard it has to be done on the camera

# **Proof of Concept System** Vivado IP Integrator Block Design REFCLK FPGA\_RESET\_N PCIe Link

The design of scalable, complex control and data acquisition systems for fusion devices requires application of various real-time data processing devices, such as FPGA (Field Programmable Gate Array) circuits, GPU (Graphics Processing Unit) and CPU (Central Processing Unit). The hardware platform should assure low overhead and high performance of the data transmission. It is profitable to store the data and process it in the same memory space. The data should be directly transmitted from the sensor to data processing unit. The Authors proposed a new scalable hardware solution suitable for distributed DAQ systems where the PCI Express endpoint is integrated with the sensor such as camera or digitiser. The architecture allows to transfer data directly from the sensor to data processing unit, and therefore avoid multiple copying. Such a solution has various advantages including low overhead, high performance and scalability. The solution also effortlessly provides optical isolation, required for application in most plasma devices. The developed architecture and initial measurements for imaging system will be presented and discussed in paper, published at later time.



Memory

CPU 1

CPU N

GPU







Hardware Platform



### Conclusions

Lodz University of Technology **Department of Microelectronics** and Computer Science