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## An 8.8-ps RMS Precision Time-to-Digital Converter Implemented in a Cyclone 10 LP FPGA with Automatic Temperature Correction

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This paper presents a non-uniform multiphase (NUMP) time-to-digital converter (TDC) implemented in field-programmable gate array (FPGA) with automatic temperature compensation in real time. NUMP-TDC is a novel low-cost, high-performance TDC that has achieved an excellent (2.3-ps, root mean square) timing precision in Altera Cyclone V FPGA. However, the time delays of the delay chains in some FPGAs (for example, Altera Cyclone 10 LP) change significantly with the changes of the temperatures. Thus, the timing performances of the NUMP-TDCs implemented in those FPGAs are significantly affected by the temperature fluctuations. In this study, we developed a simple method to monitor the changes of the time delays using two registers deployed at the two ends of the delay chains, and to compensate the changes of the time delays using a look-up table (LUT). When the changes of the time delays exceed a given threshold, the LUT for delay correction is updated and the bin-by-bin correction is launched. Using this correction approach, a precision of 8.8-ps RMS over a wide temperature range (5°C to 80°C) has been achieved in a NUMP-TDC implemented in a Cyclone 10 LP FPGA.

### Minioral

Yes

### IEEE Member

No

### Are you a student?

Yes

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