

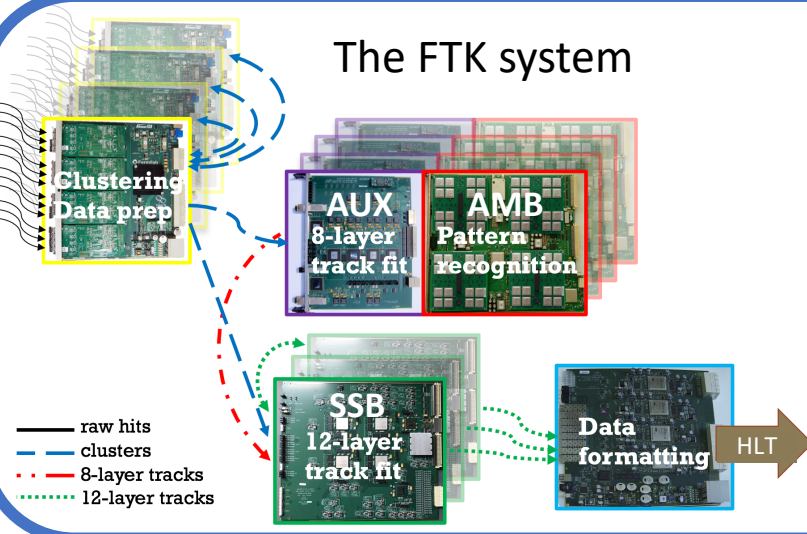
Cooling and timing tests of the ATLAS Fast Tracker VME boards

Simone Sottocornola on behalf of the FTK VME team*

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The FTK system



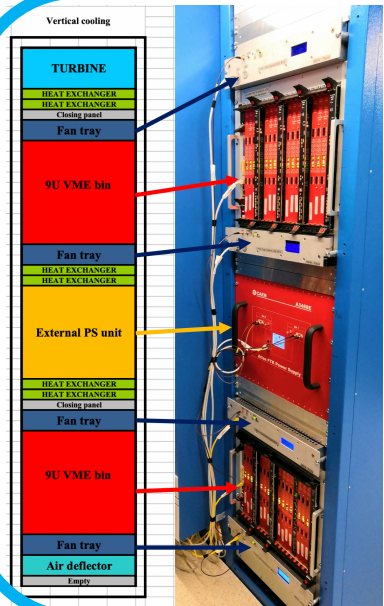
The Fast Tracker (FTK) is a **data driven** and **massively parallel track reconstruction** system.

- Designed to reconstruct tracks with $100 \mu\text{s}$ latency at **100 kHz input rate**.
- HW processor based on pattern recognition:
 - **2k FPGAs** for data clustering, formatting and fitting.
 - **8k Associative Memory chips** (AM - ASICs) for pattern matching.
- More than 450 boards, dataflow on serial links ($\sim 10\text{k}$ links), complex synchronization.
- Based on ATCA and VME standards.

FTK boards **dataflow is monitored using spybuffers**.

AM chips perform **pattern matching** on the whole event in the detector readout time. The **study of AM board timing is crucial** for ensuring the required latency.

- Clusters (**Hits**), sent from the AUX board, are received in parallel on 8 serial inputs (**HIT Time**).
- Hits are compared to each pattern inside the AM chips, on a single clock cycle.
- The tracks candidates (**Roads**) found by the AM chips are readout in parallel on 16 serial links, and then sent back to the AUX card (**Road Time**).
- While an event is received by the AM chips the previous event is readout from them in parallel.

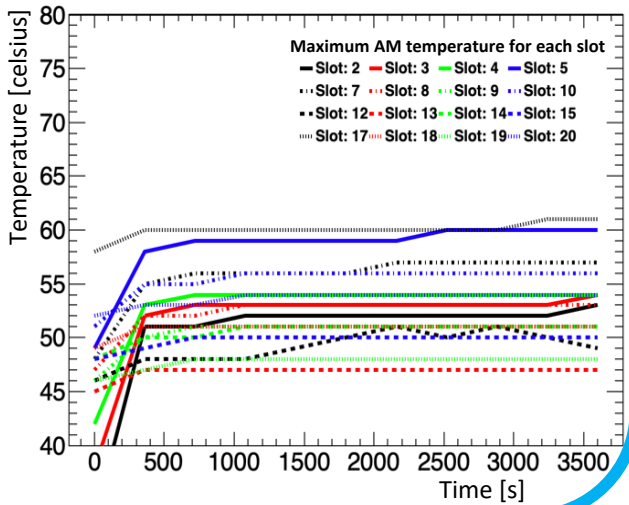


The FTK design implies a **very high density computing power**, thus the FTK VME crates are equipped with **custom cooling and power distribution**.

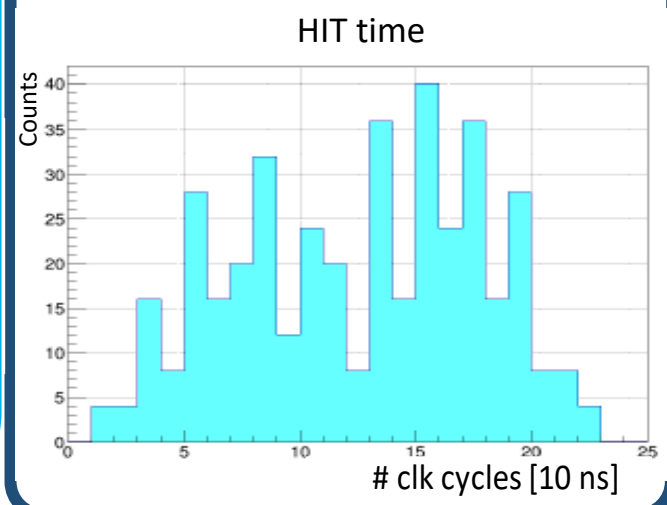
Characterization of the power consumption and cooling system performance is mandatory.

- 16 kW/rack power in data-taking conditions.
- 80°C boards PCB safe temperature limit.
- **Largest source of heat is the number of bit flips (BF) per clock cycle in AM chips** (data dependent):
 - Simulated expected BF values during run.
 - Performed cooling tests in many conditions.

Optimizations allowed sufficient cooling power to cover the worst case scenario.



The timing measurements **confirmed consistency with 100 kHz processing**.





A few details

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FTK VME cooling

FTK characterized by **very high density power** consumption.

- Single VME rack contains more than **2000 AM chips and 350 FPGAs**.
- Tests are mandatory to guarantee sufficient cooling power.

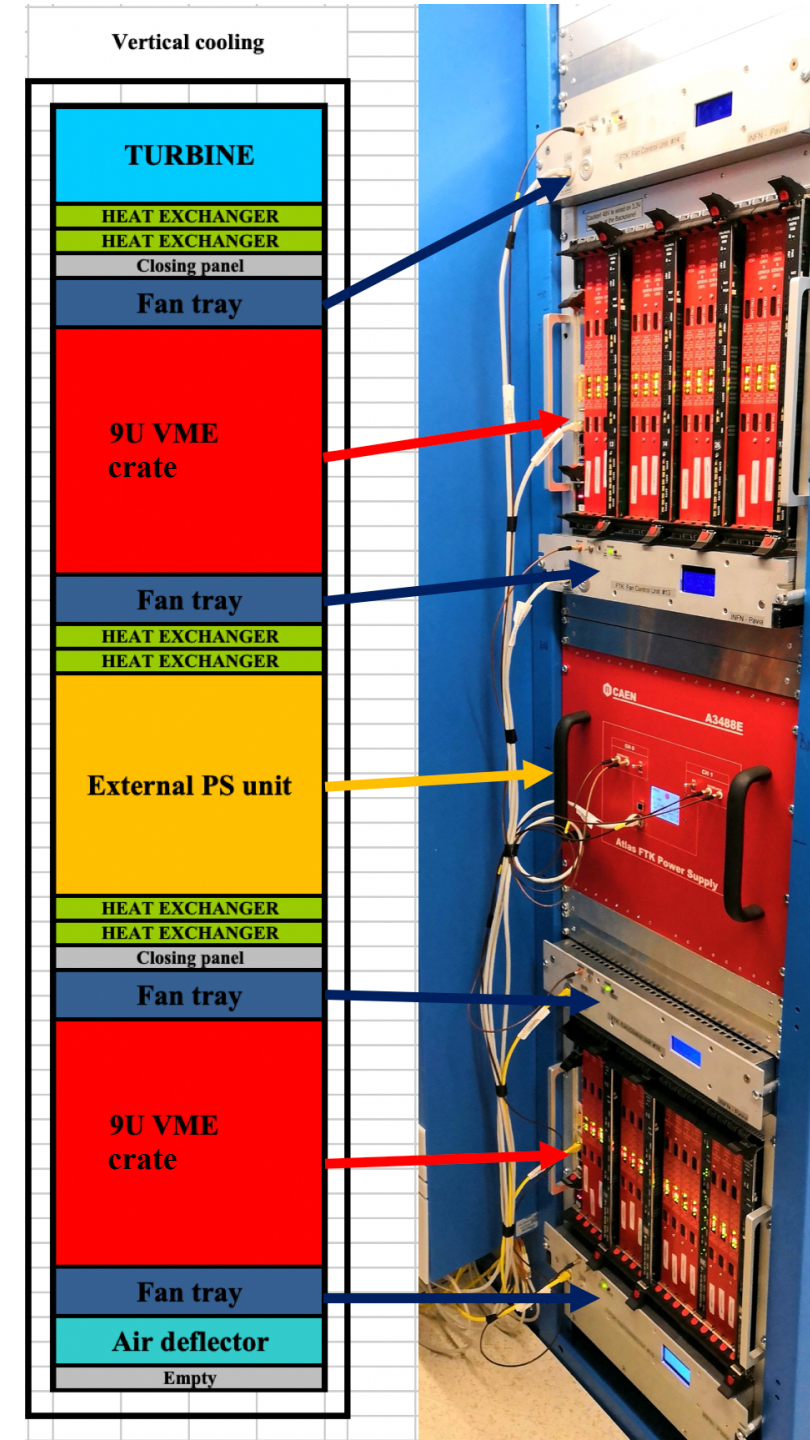
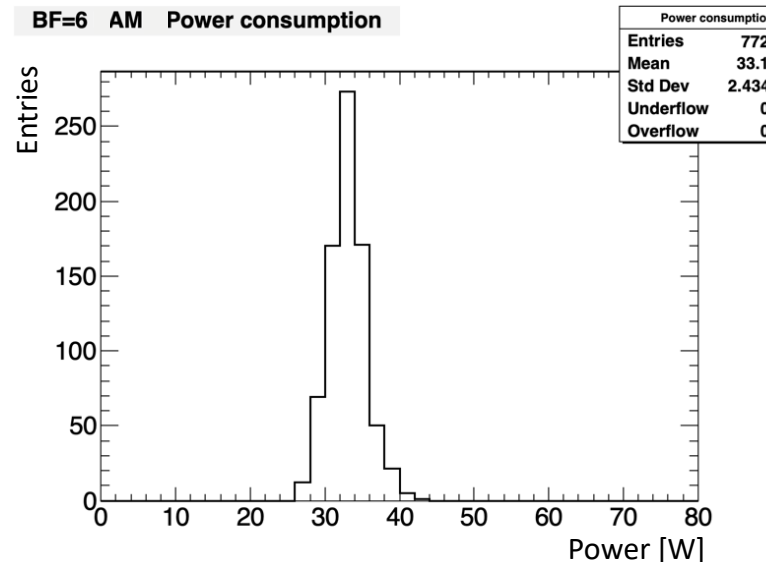
Two different power consumption cases for FTK VME boards:

- For FPGA based boards, power consumption is fixed (**FW dependent**).
- For AM chip based boards, consumption varies with number of bit flips per clock cycle (**data dependent**).

Number of bit flips for given data taking condition extracted from simulation.

- **Real board's power measured** by running on generated test data.

FTK VME component	Power consumption
AUX (FPGAs)	~ 70 W
AM Board	230-250 W
SSB (FPGAs)	~ 160 W
Rack	~16 kW



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FTK VME cooling

Custom cooling system required to keep components running in safe working conditions and to increase components' lifetime.

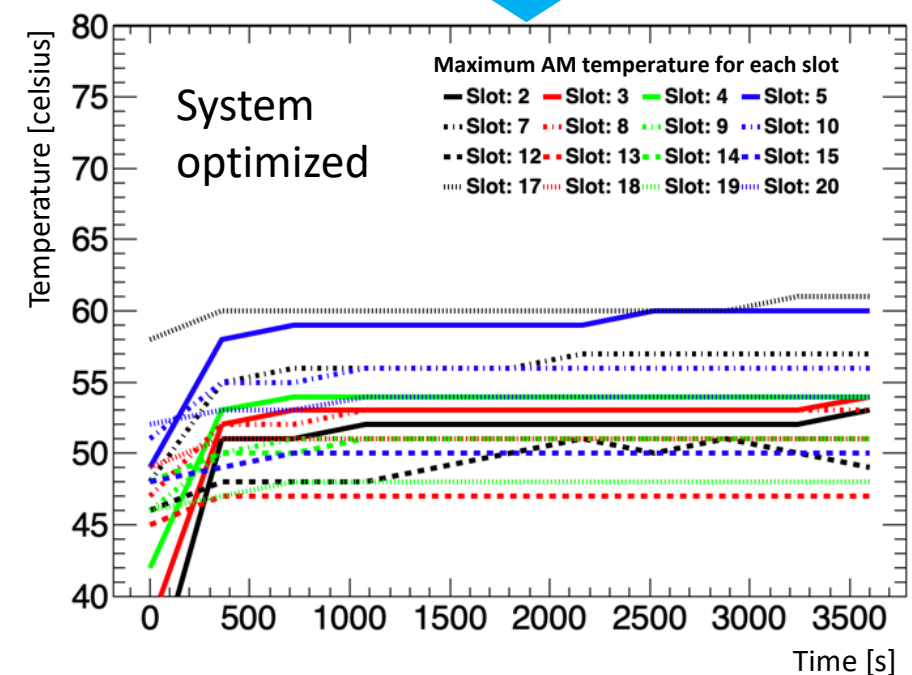
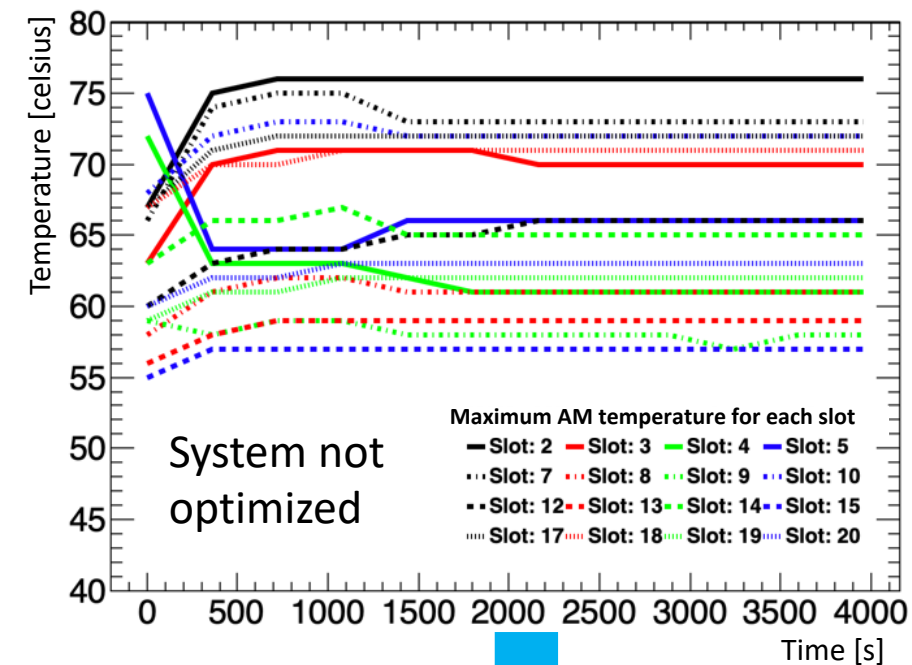
- **Threshold of 80 °C** on boards PCB selected as safe temperature limit. To ensure electronic safety, firmware and software protections set up:
- **FW interlocks** blocking board processing when onboard sensor threshold reached.
- **SW protections** cutting rack power if rack air temperature above 38 °C or single board sensor exceeds temperature threshold.

To ensure operation of the FTK system, cooling tests have been performed.

- Temperatures monitored on onboard sensors and on rack air.

After optimizations, **cooling proven to be sufficient for the worst expected operation conditions:**

- Optimized AM board power consumption.
- Optimized speed of fans and board intra-crate positions.
- Optimized cooling water flux and temperature.
- Optimized all temperature thresholds.



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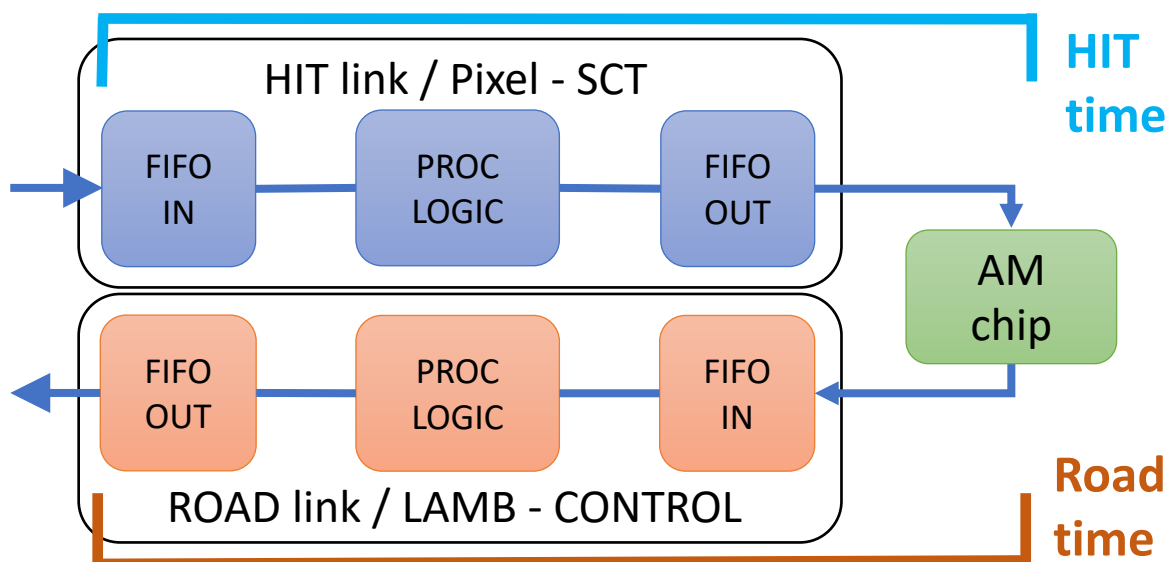
VME boards

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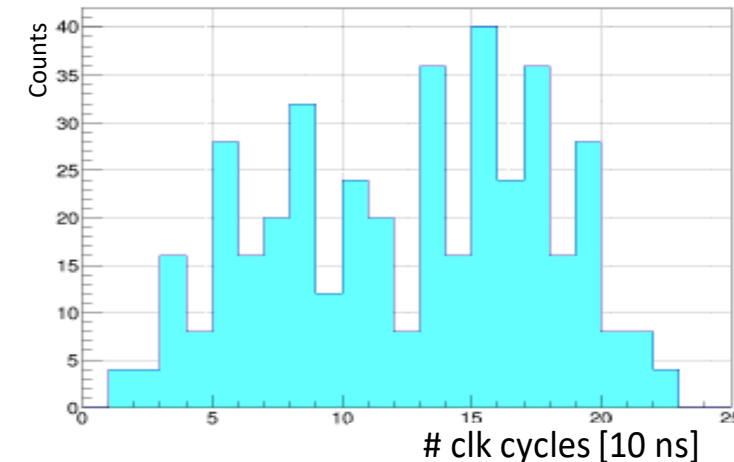
AM board timing

- AM board output link times characterized by two contributions:
 - IDLE word cycles required for end of event identification: 500 clock cycles.
 - This time affects also events with zero roads, measured at AM chip output.
 - Time required to **propagate first 9 roads** through daisy chain and Road output logic: **~150 clock cycles**.
 - This contribution depends on the number of roads fired.
- The 500 clock cycles **IDLE word** was originally set as a conservative value.
 - Now **optimized to 50 clock cycles**, drastically reducing output time.

The **input and output time** of the AM board is **proven to be consistent with the 100 kHz** design processing rate.



HIT time



Road time VS number of matched roads

