ATLAS hardware-based Endcap Muon Trigger for future upgrades

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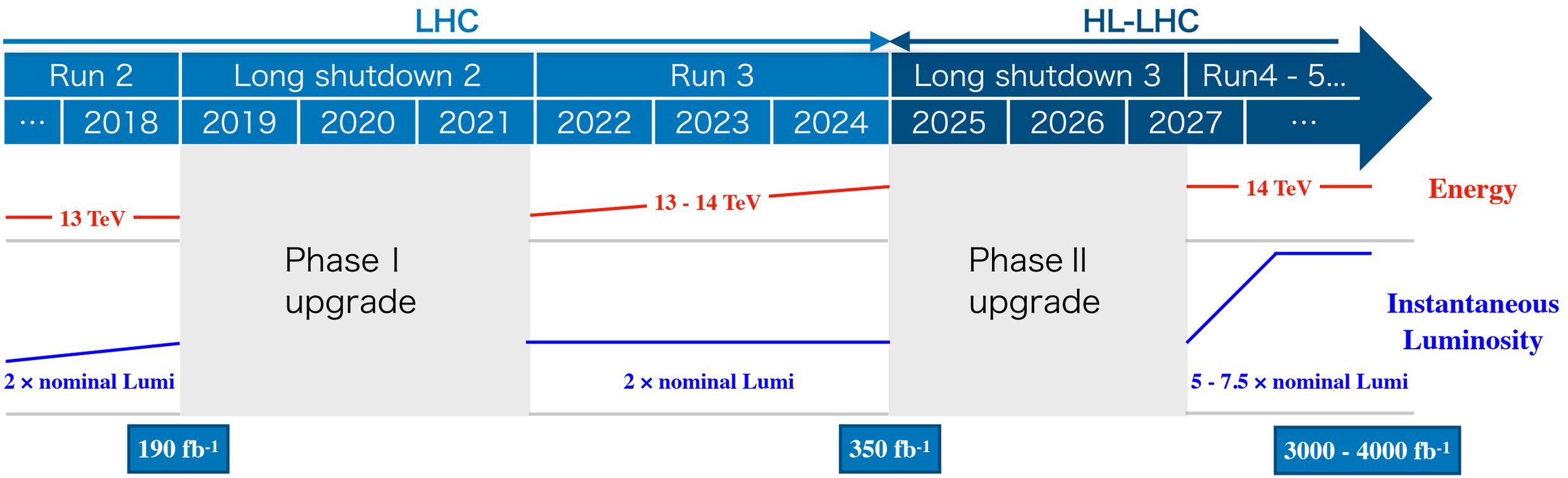
Yuya Mino (Kyoto University)
on behalf of the ATLAS Collaboration

Introduction

- Future upgrades are planned for new physics searches and standard model precision studies with higher energy and luminosity.
  - **Run 3** : Increase center-of-mass energy to 14 TeV with an instantaneous luminosity to 2 × 10^{34} $cm^{-2}s^{-1}$ (**Higher energy**)
  - **HL-LHC** : Planned to start the operation in 2027 with an instantaneous luminosity of 5.0 - 7.5 × 10^{34} $cm^{-2}s^{-1}$ (**Higher luminosity**)

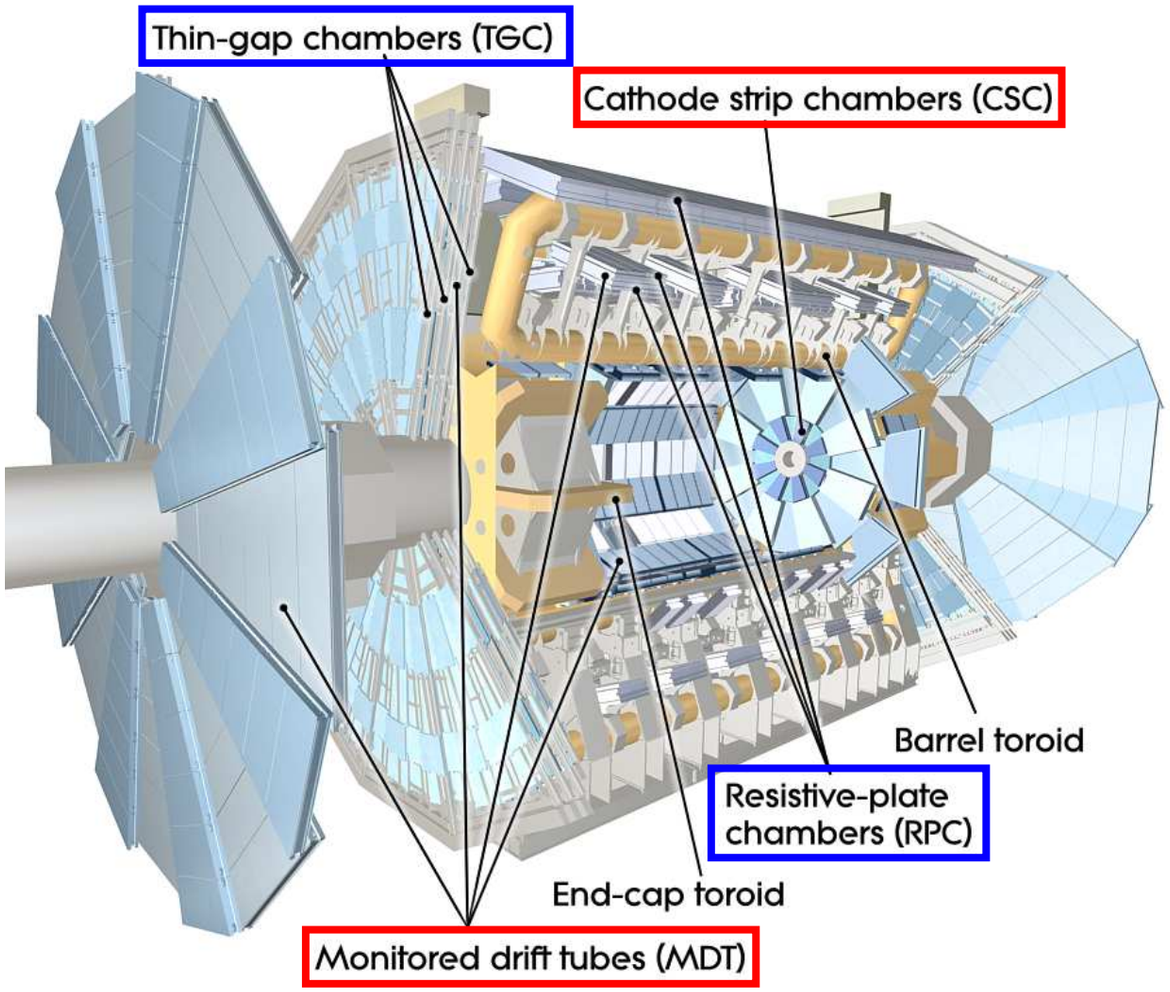


- Continuous upgrades of the hardware-based (Level-1/0*) endcap muon trigger is required to cope with the high event rate.

* First trigger level is renamed Level-1→ Level-0 after Run3

Muon system in Run 2

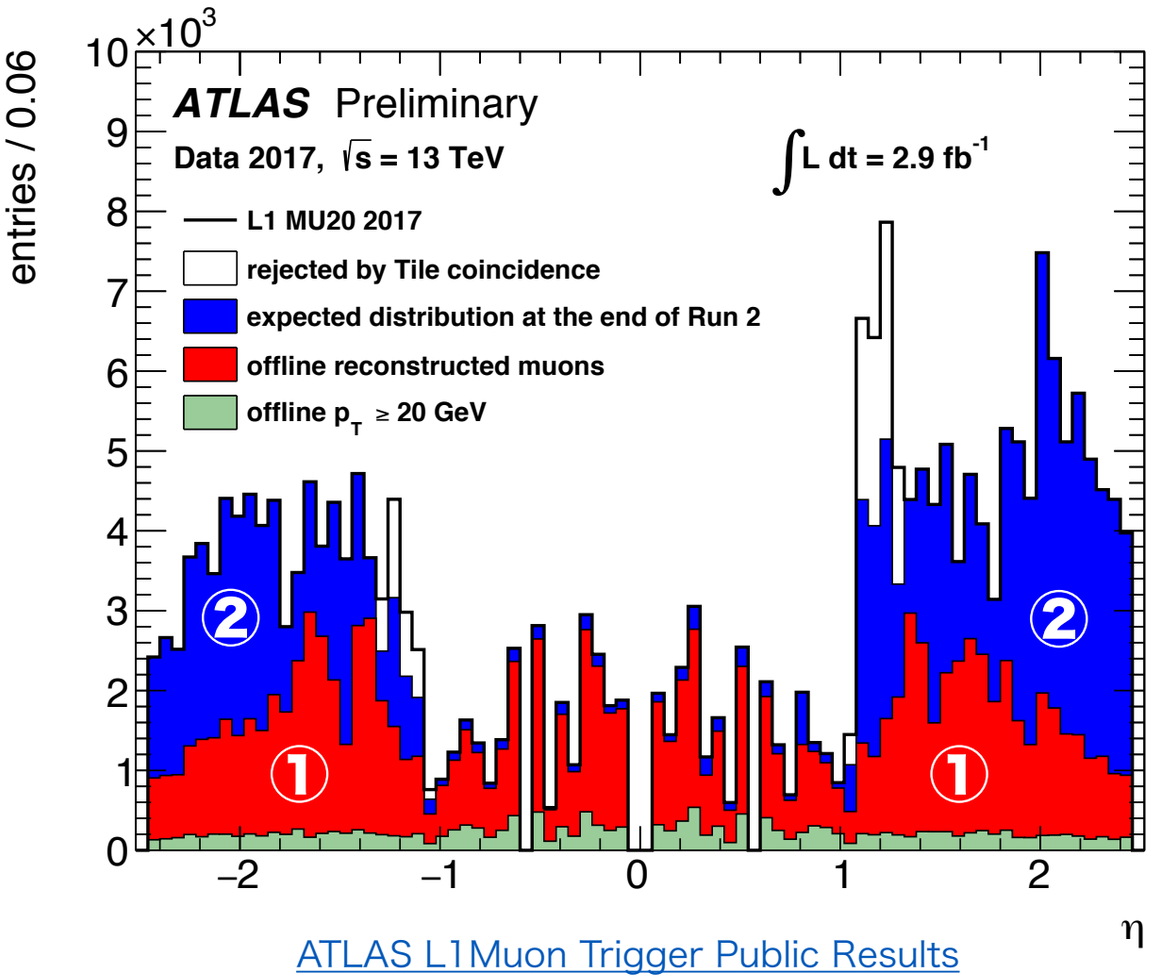
- Muon detector system consists of 4 types of detectors for **triggering** and **precision tracking**.



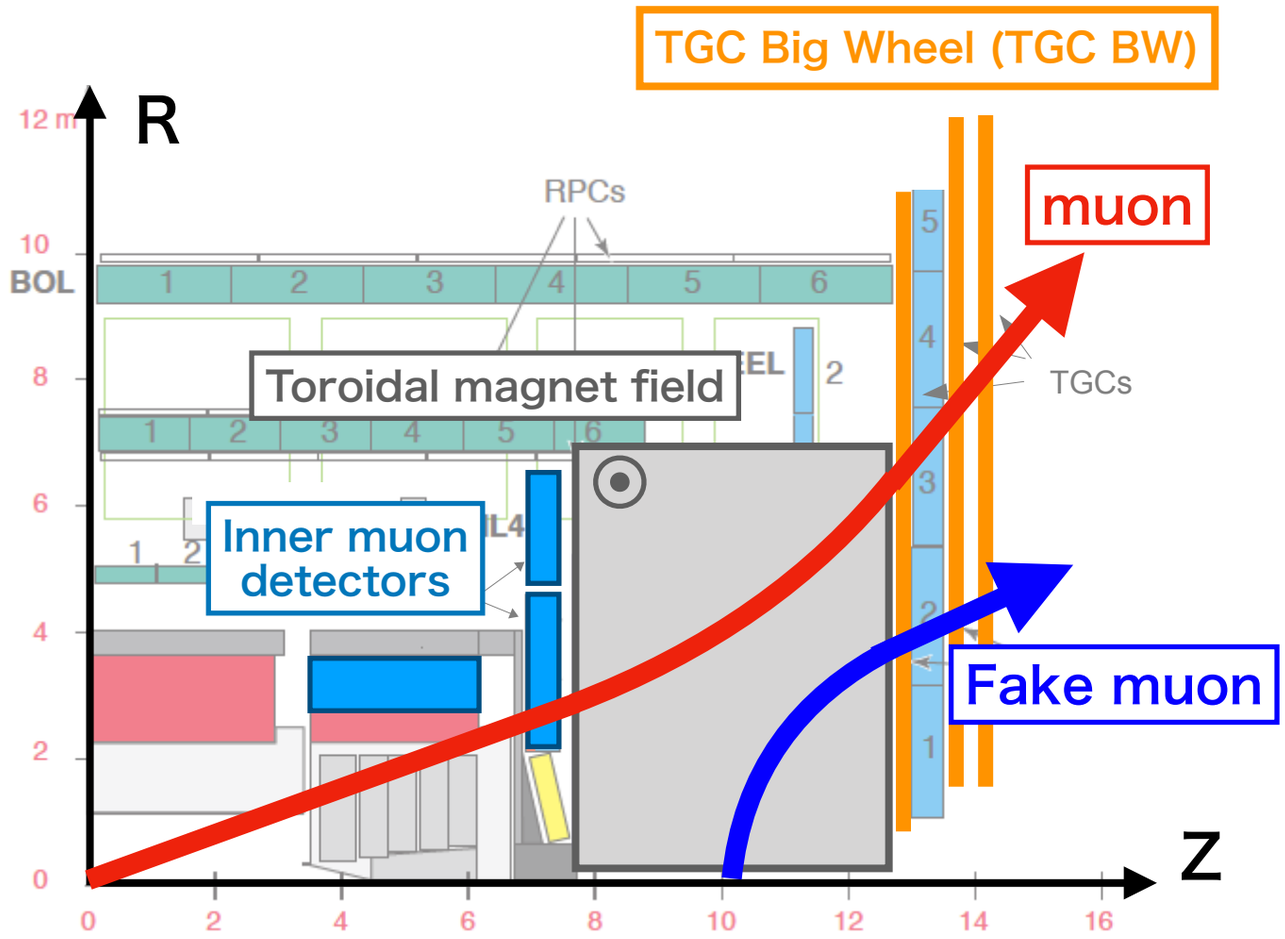
- **Thin Gap Chamber (TGC)**
  - Multi-wire proportional chamber
  - Covers the endcap region ($1.05 < |\eta| < 2.7$)
- **Resistive Plate Chamber (RPC)**
  - Covers the barrel region ($|\eta| < 1.05$)
- **Monitored Drift Tube (MDT)**
  - Placed inside ($|\eta| < 2.0$) and outside ($|\eta| < 2.7$) the magnetic field
- **Cathode Strip Chamber (CSC)**
  - Placed only inside the magnetic field ($2.0 < |\eta| < 2.7$)
  - Used to cope with high event rate

Level-1 muon trigger in Run 2

- p_T threshold is set for Level-1 muon trigger to select events with high-p_T muons from interesting physics processes.
- Level-1 muon trigger rate in Run 2 is dominated by
  ① Triggers by **low p_T muons** below the p_T threshold.
  ② Triggers by charged particles emerging from the endcap toroid magnets. (**Fake muons**)
  ➡ New coincidence logic developed in Run 3 and HL-LHC to reduce ① & ②.

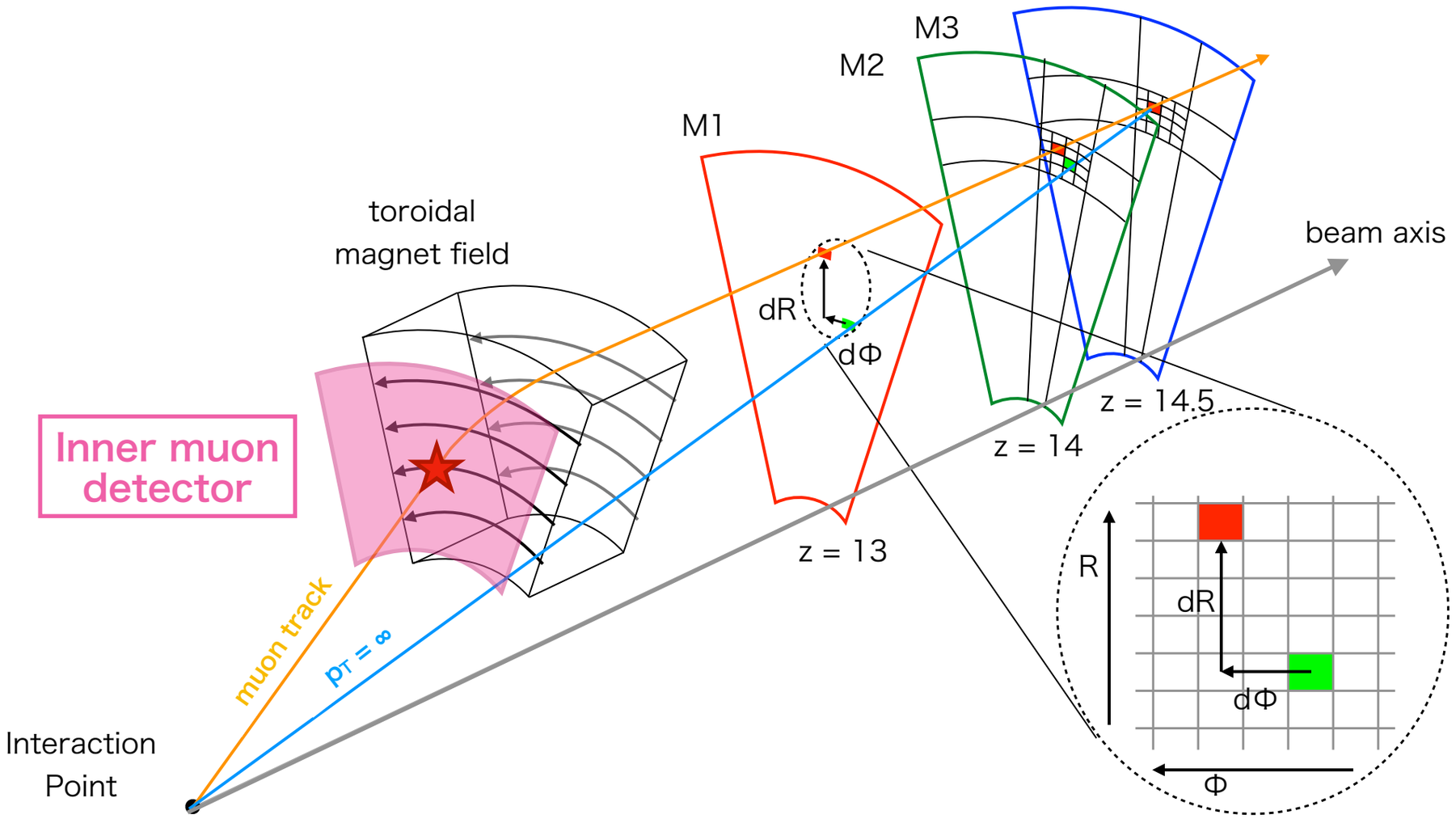


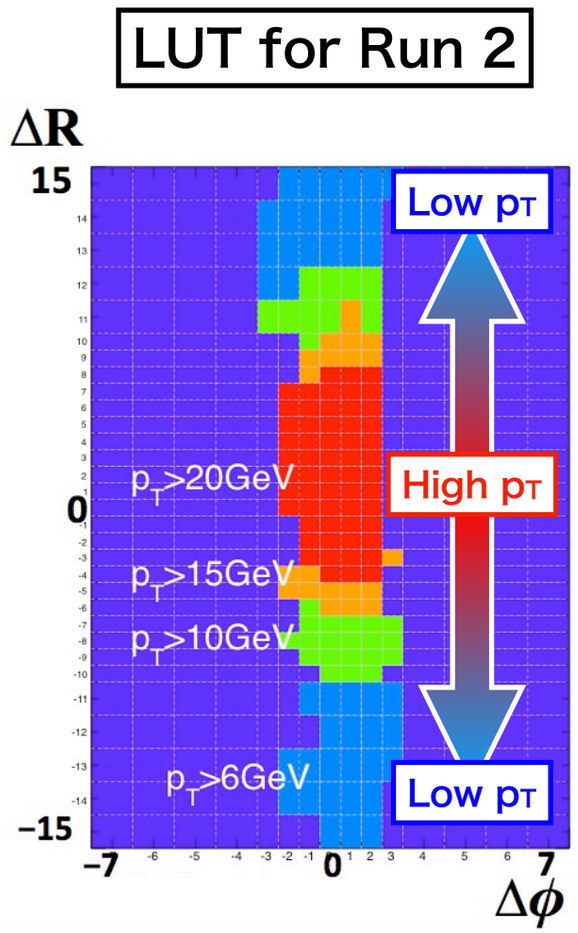
ATLAS L1Muon Trigger Public Results



Hardware-based online triggering

- Basic concept of endcap muon hardware trigger :
  - Position difference (dR, dϕ) in the TGC BW calculated on the front-end boards.
  - dR, dϕ information is handed over to a **Look-Up-Table (LUT)** implemented on trigger processor board to calculate p_T of the muon candidates. **(TGC BW coincidence)**
  - Require hits in the inner muon detector to reduce fake muons. **(Inner coincidence)**

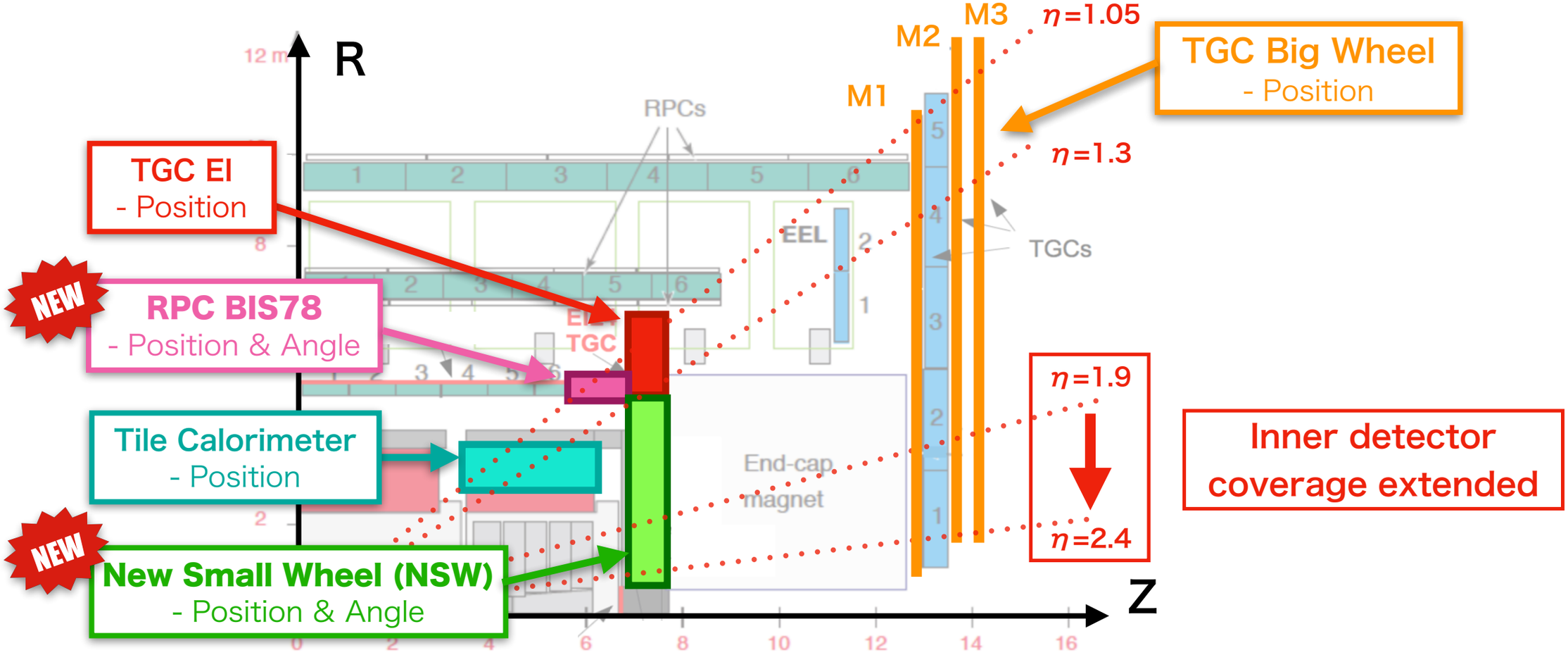




Run 3

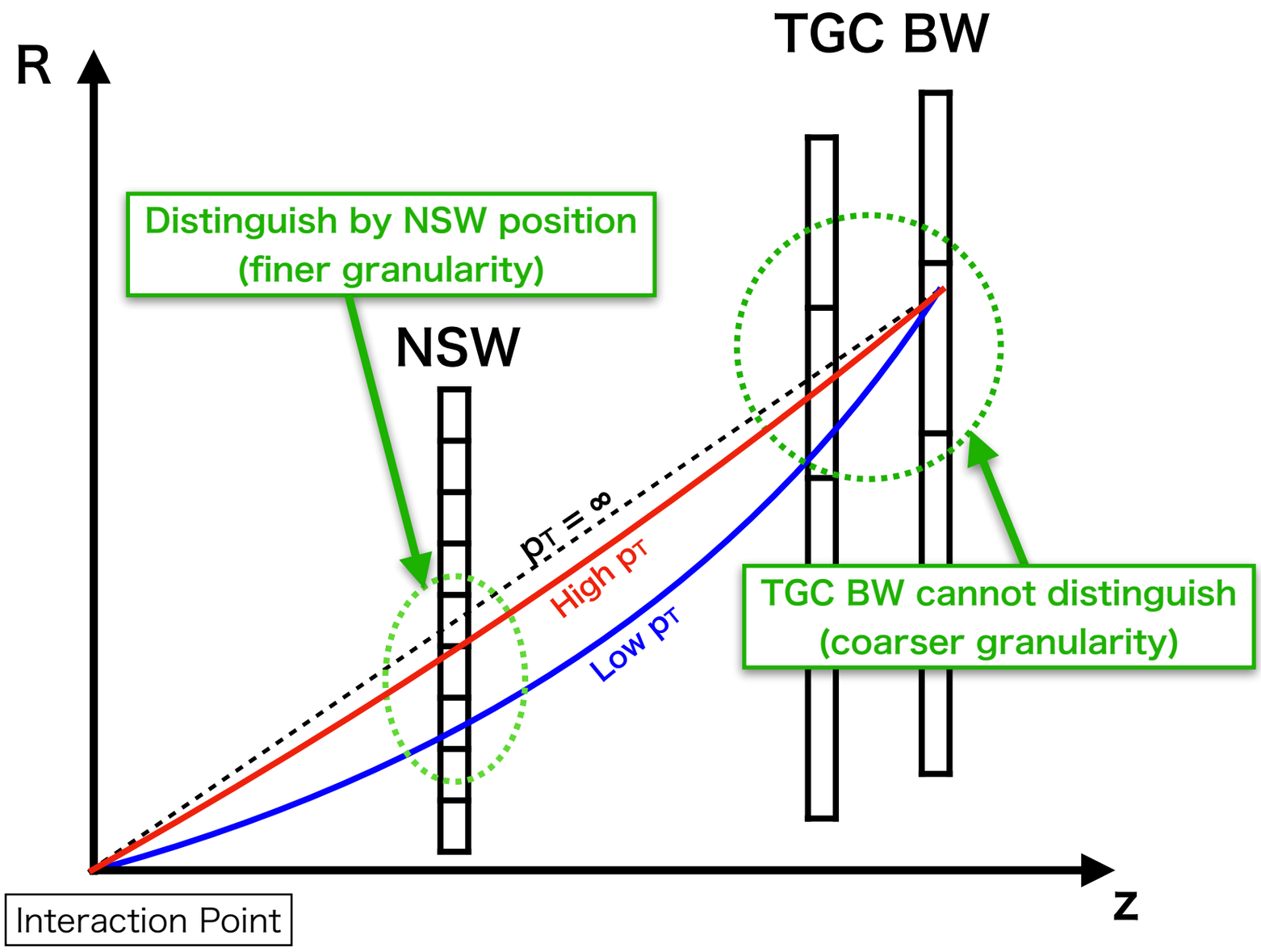
Level-1 endcap muon trigger in Run 3

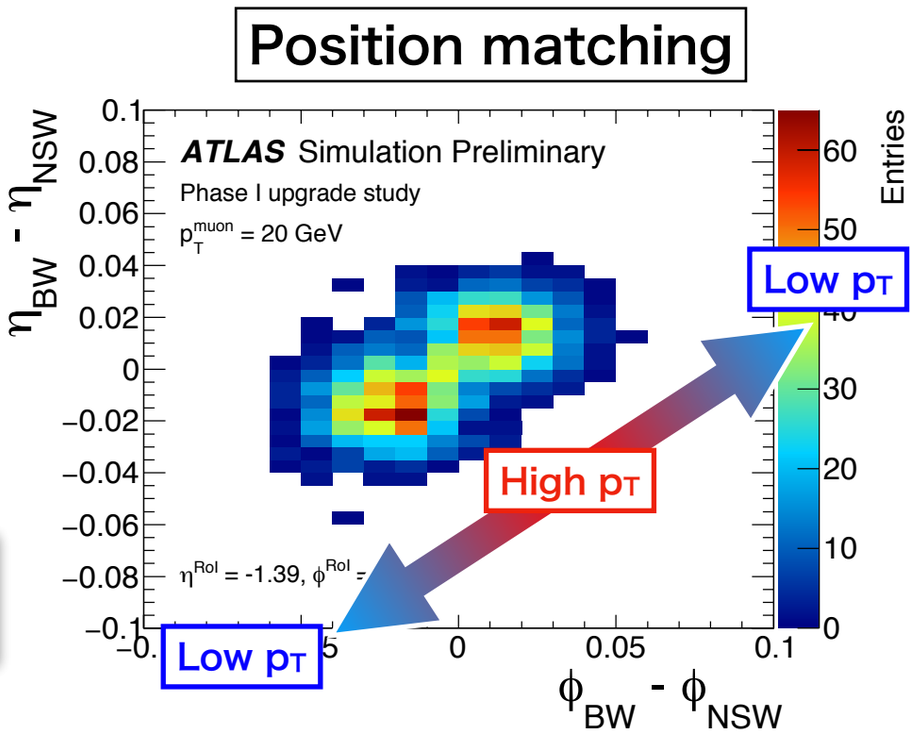
- New detectors will be installed to measure muons with higher resolution and reduce fake muons.
  - ① **New Small Wheel (NSW)**
    - Consists of 8 layers each of small-strip TGC and Micromegas. (Total 16 layers)
  - ② **Resistive Plate Chamber BIS78 (RPC BIS78)**
    - Consist of 3 layers of RPC
  - Finer position and angle information combined with TGC BW position to reduce fake muons and re-calculate p_T. (①, ②)
  - Coverage of the inner muon detector extended from $|\eta|$ = 1.9 to 2.4 . (①)



Coincidence logic with new inner muon detectors in Run 3

- Position and angle matching between TGC BW and new inner muon detectors are implemented to measure p_T with higher precision.





ATLAS L1Muon Trigger Public Results

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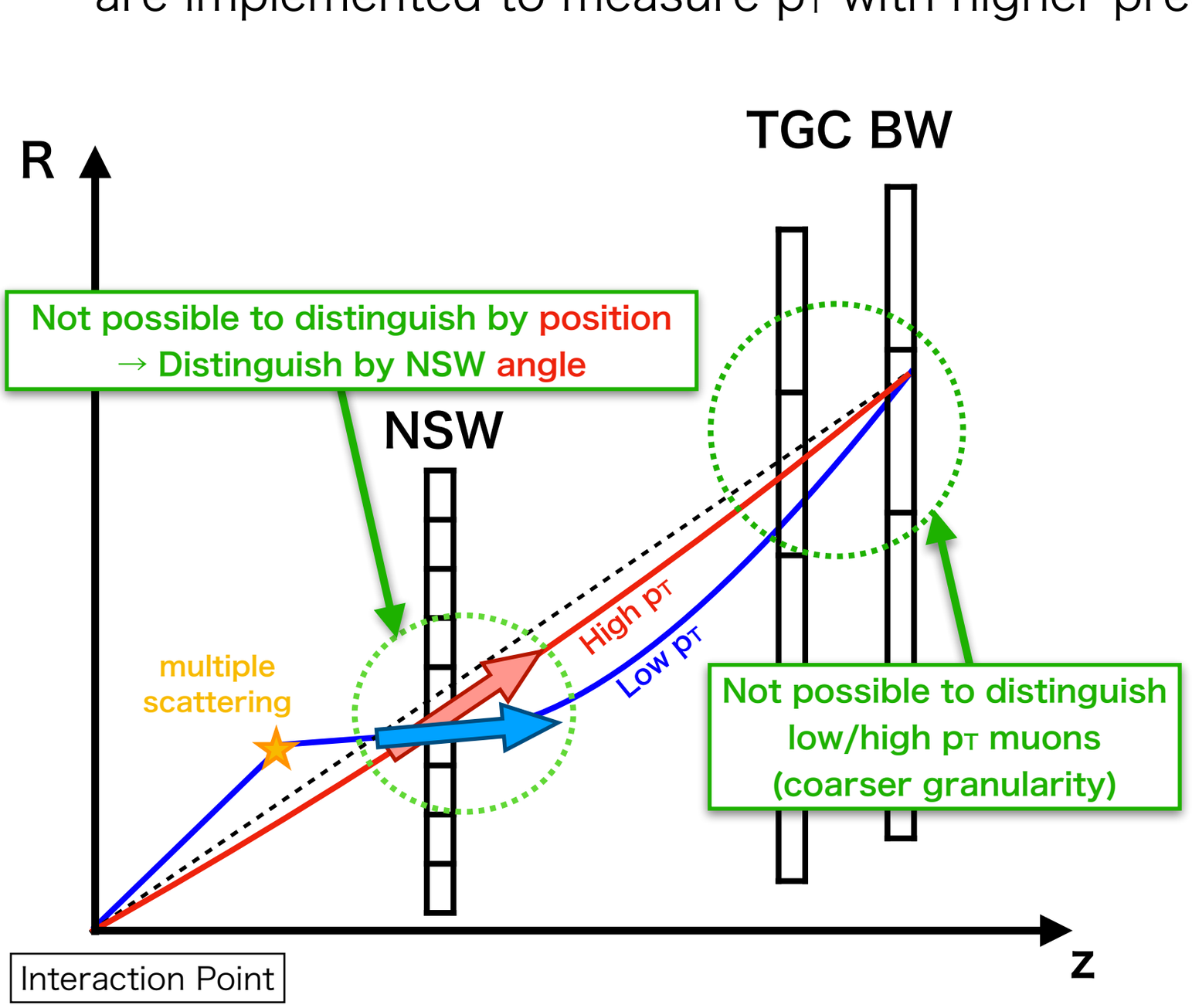
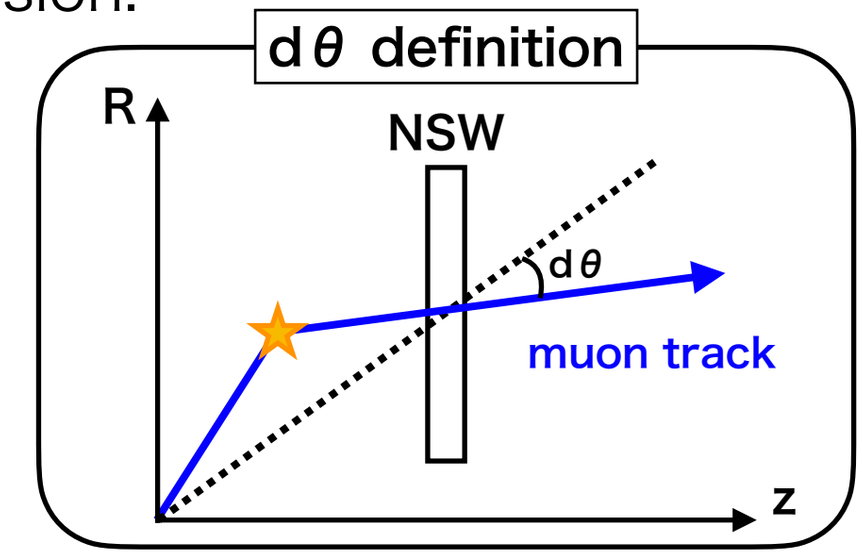
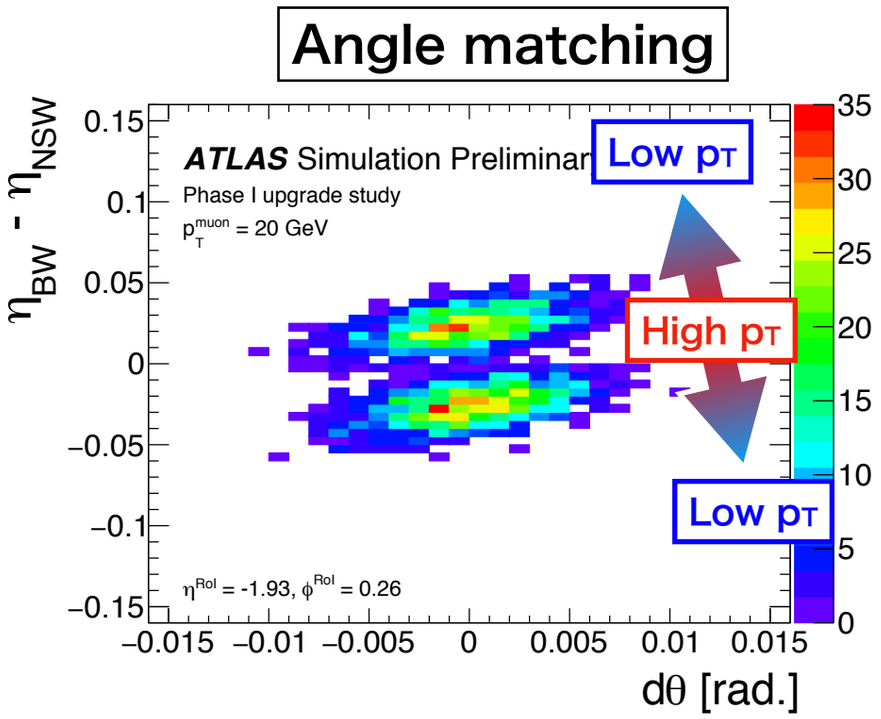






ATLAS L1Muon Trigger Public Results

Hardware design of Sector Logic in Run 3

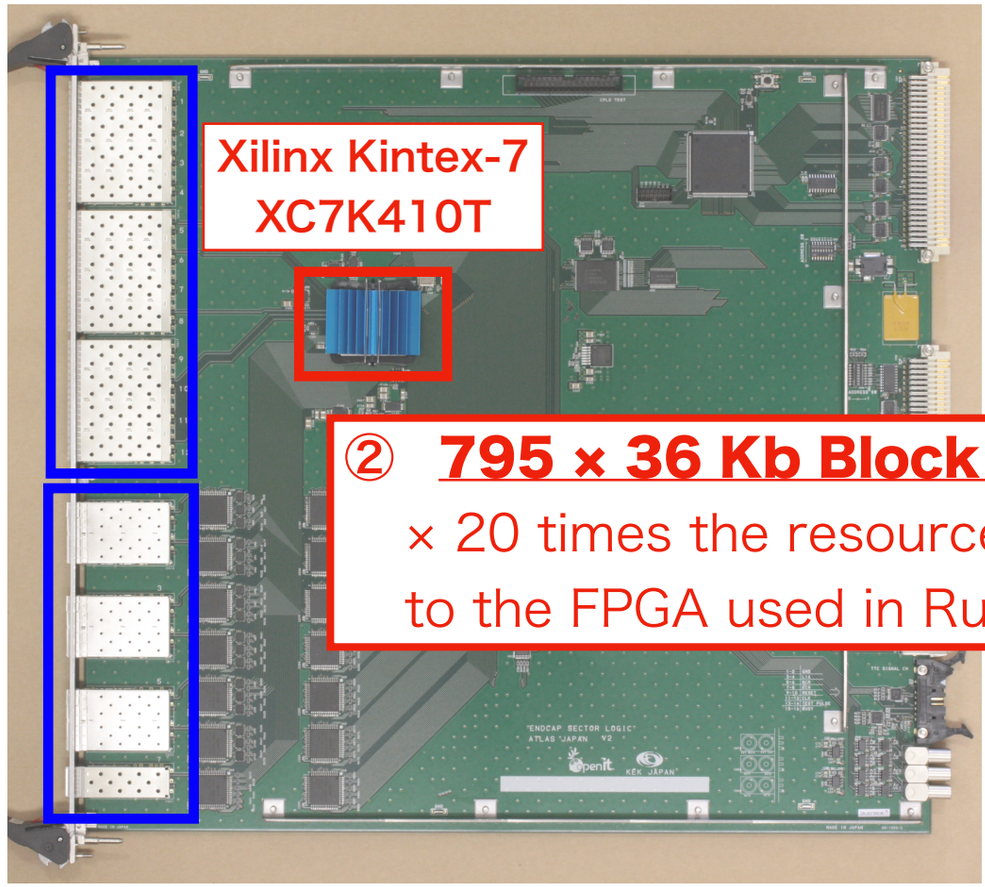
- Endcap trigger processor board (Sector Logic) is required to have
  ① Enough I/O ports to handle data from various detectors.
  ② Large amount of resources to implement new coincidence logic.
  ▶ New Sector Logic (SL) board has been developed.

① Optical interfaces are placed to use **GTX*/G-Link** connection

GTX
For TGC EI, NSW ,BIS78
8 lanes × 6.4 Gbps = **51.2 Gbps**

G-Link
For TGC BW, Tile
13 lanes × 0.8 Gbps = **10.4 Gbps**

NewSL board

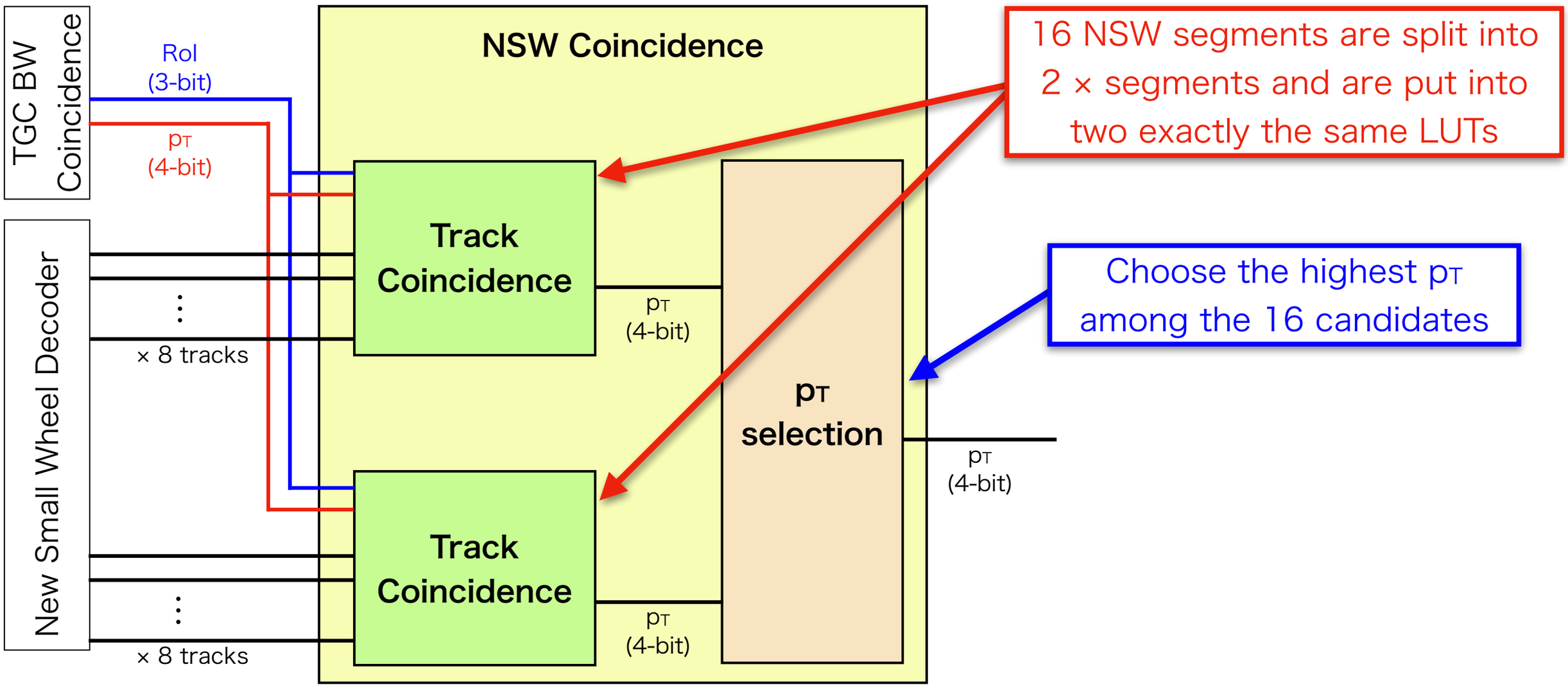


*** GTX: multi-gigabit transceivers for Xilinx Kintex-7 FPGAs**

- Installation is completed and the commissioning is ongoing.

Firmware implementation for NSW coincidence logic

- Each muon candidate from TGC BW is compared with 16 track candidates from NSW.
- Limitation on the latency is set to 2 LHC clocks (40 MHz) in Run 3.
  ①Coincidence is calculated in parallel using two identical LUTs with 320 MHz clock.
  → 2 × 8 = 16 candidates can be processed in 1 LHC clock.
  ②The best candidate is chosen in the p_T selection.



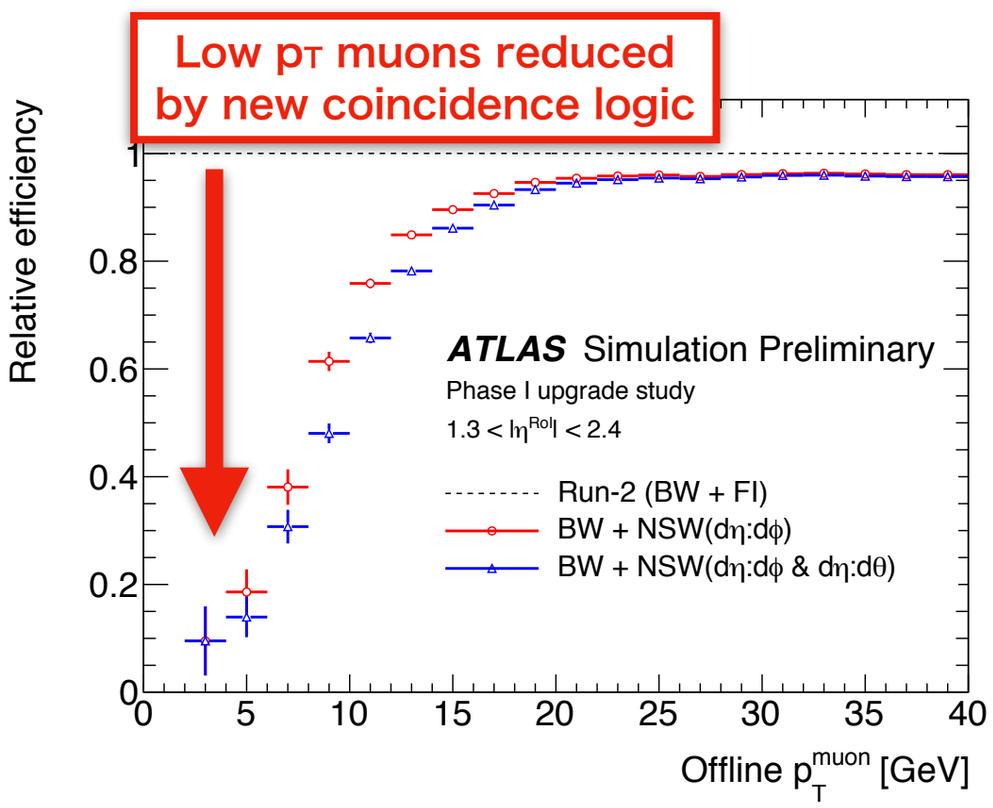
Performance of Level-1 endcap muon trigger in Run 3

Efficiency

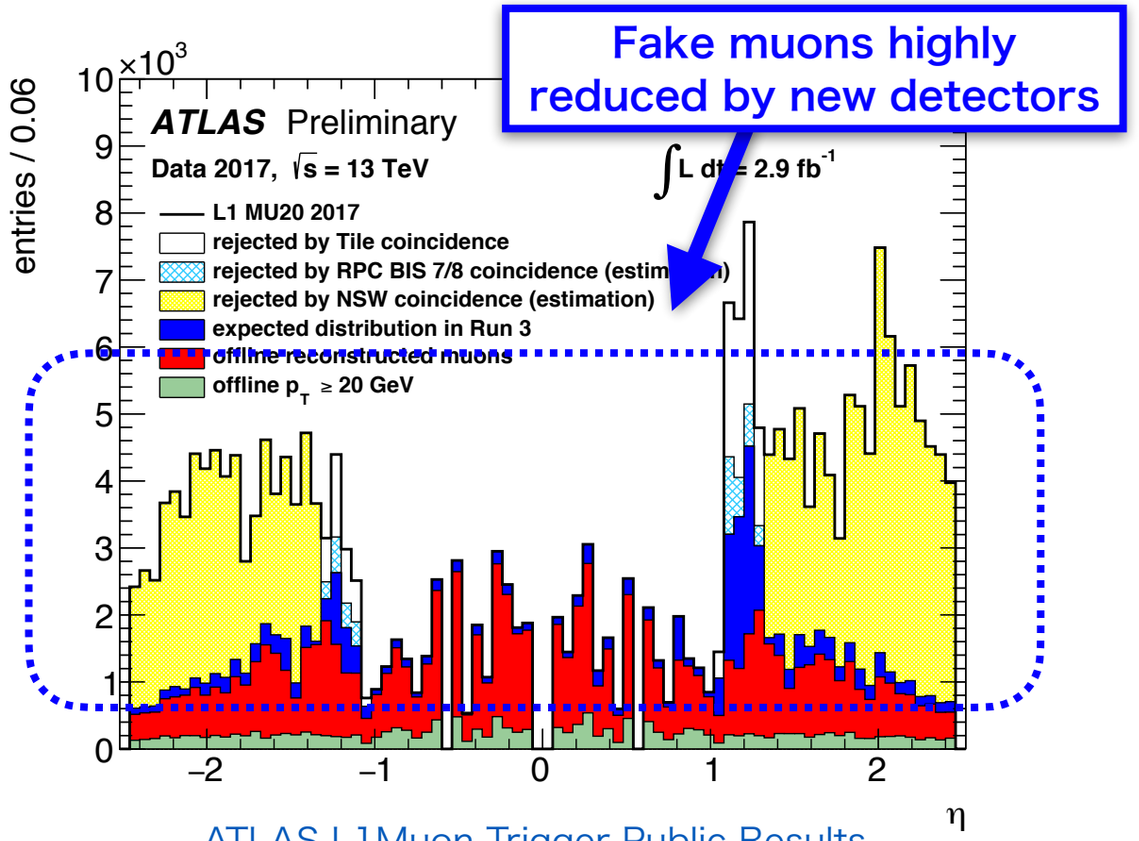
- Rejection power for **low p_T muons** is estimated from a single muon MC simulation sample.
  - Higher reduction for low p_T muons relative to Run 2 trigger.
  - **~ 95%** relative efficiency for muons with p_T > 20 GeV.

Trigger rate

- Rejection power for **fake muons** is estimated from 2017 data. (fake muons cannot be modeled by MC)
  - **~ 90%** of fake muons are reduced by new inner muon detectors compared to Run 2 logic.
  - Expected trigger rate in Run 3 is **13 kHz** . (**~ 53%** rate reduction)



ATLAS L1Muon Trigger Public Results

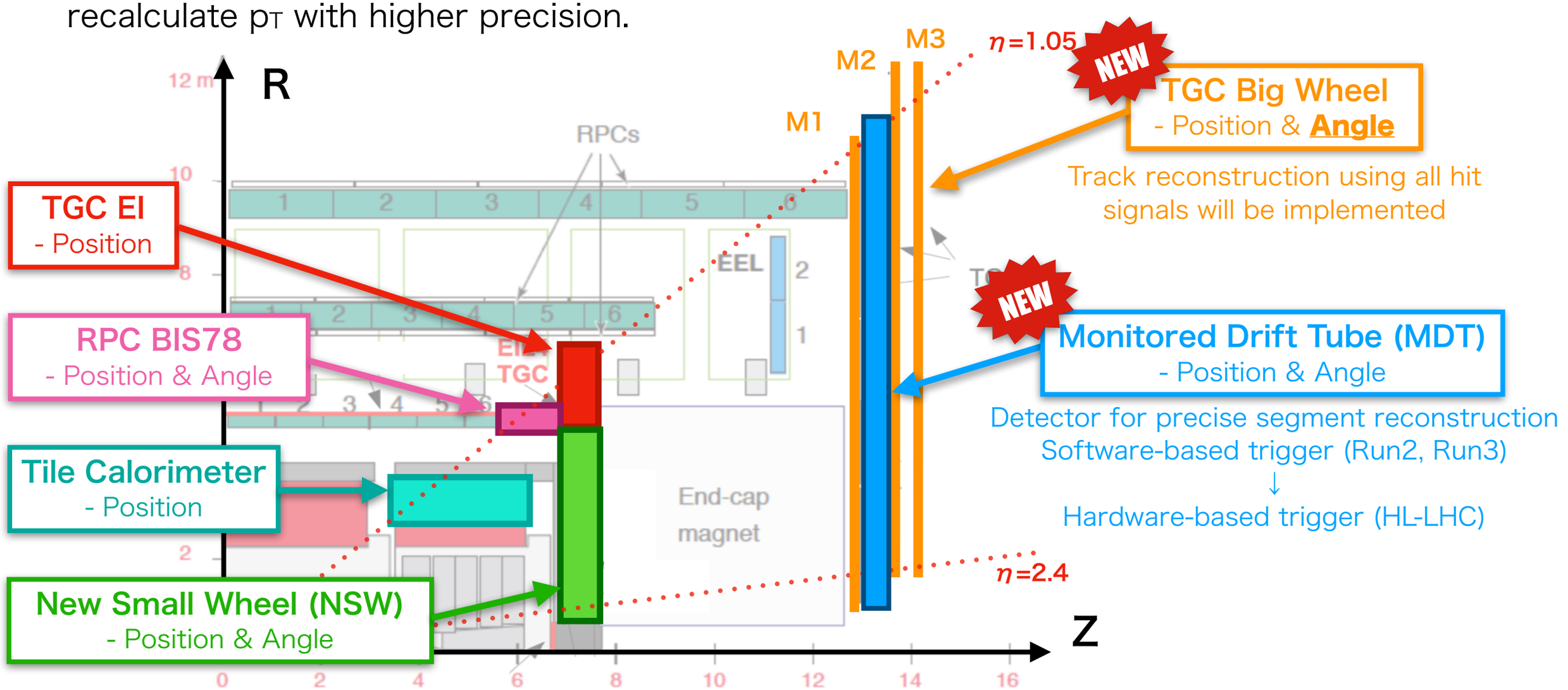


ATLAS L1Muon Trigger Public Results

HL-LHC

Level-0 endcap muon trigger in HL-LHC

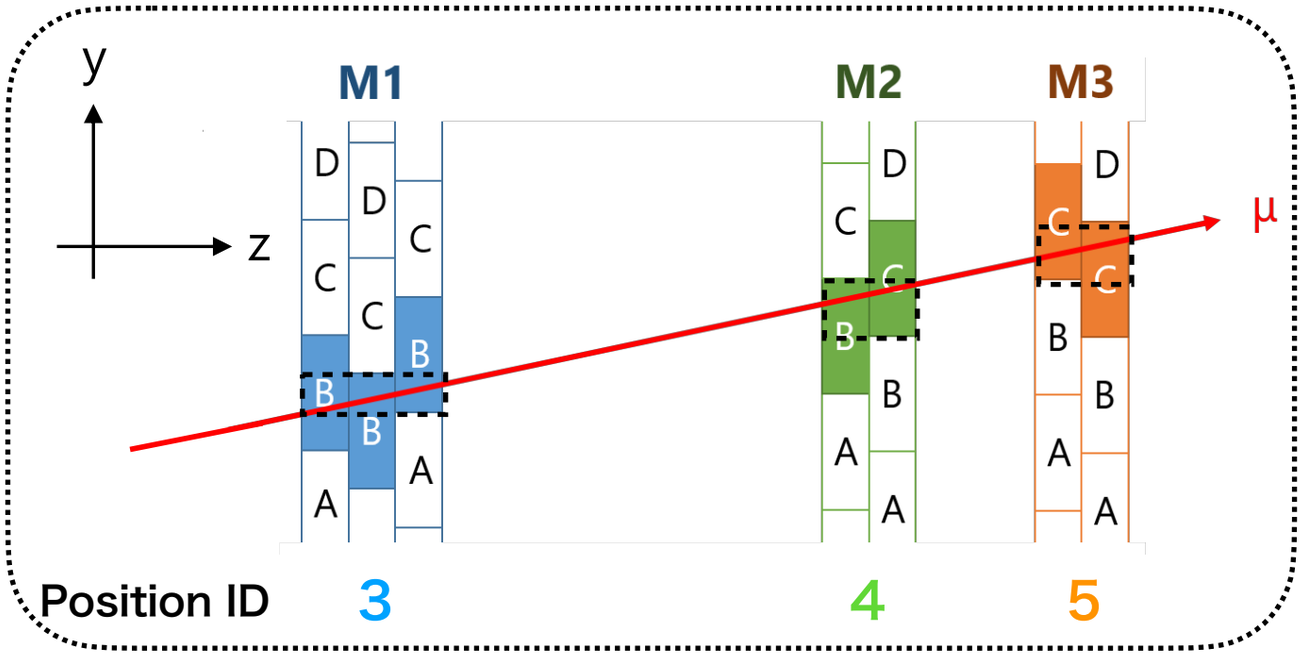
- Required to reconstruct muon candidates with an improved momentum resolution to suppress trigger rate with minimal efficiency loss.
- Trigger and readout electronics will be replaced to extend latency and acceptable rate.
  - All TGC hit signals transferred from new boards on the detector side.
    - Track reconstruction using full-granular information will be enabled.
  - MDT (precision measurement detector) will be included in the first-level trigger to recalculate p_T with higher precision.



TGC track reconstruction

- Tracks are reconstructed in TGC with a **pattern matching** algorithm.
  - Comparing the TGC hits with predefined hit-lists for high-p_T muons.
  - Each predefined hit pattern has angle and position information associated to a track segment.
  - Coverage of the lowest p_T in the hit-lists is 4 GeV

- TGC tracks extracted in two steps
  ① Take coincidence to set a position in each station.
  ② Extract track information from the pattern list.



① Station Coincidence

M1 Coincidence

Hit ch: B B B → M1 Position ID: **3**

M2 Coincidence

Hit ch: B C → M2 Position ID: **4**

M3 Coincidence

Hit ch: C C → M3 Positon ID: **5**

② Extraction of track information

Input (Position ID, 16 bit)			Output (Track segment, 18 bit)
3	4	4	Position η_a , Angle $\Delta\theta_a$
3	**4**	**5**	Position η_b , Angle $\Delta\theta_b$
3	5	5	Position η_c , Angle $\Delta\theta_c$

Hardware design of Sector Logic in HL-LHC

- Endcap Sector Logic in HL-LHC is required to have
  ① Enough I/O ports to handle hit data from every TGC channel. (~ 6700 ch)
  ② A few hundred Mbits of memory resources to reconstruct track segments.

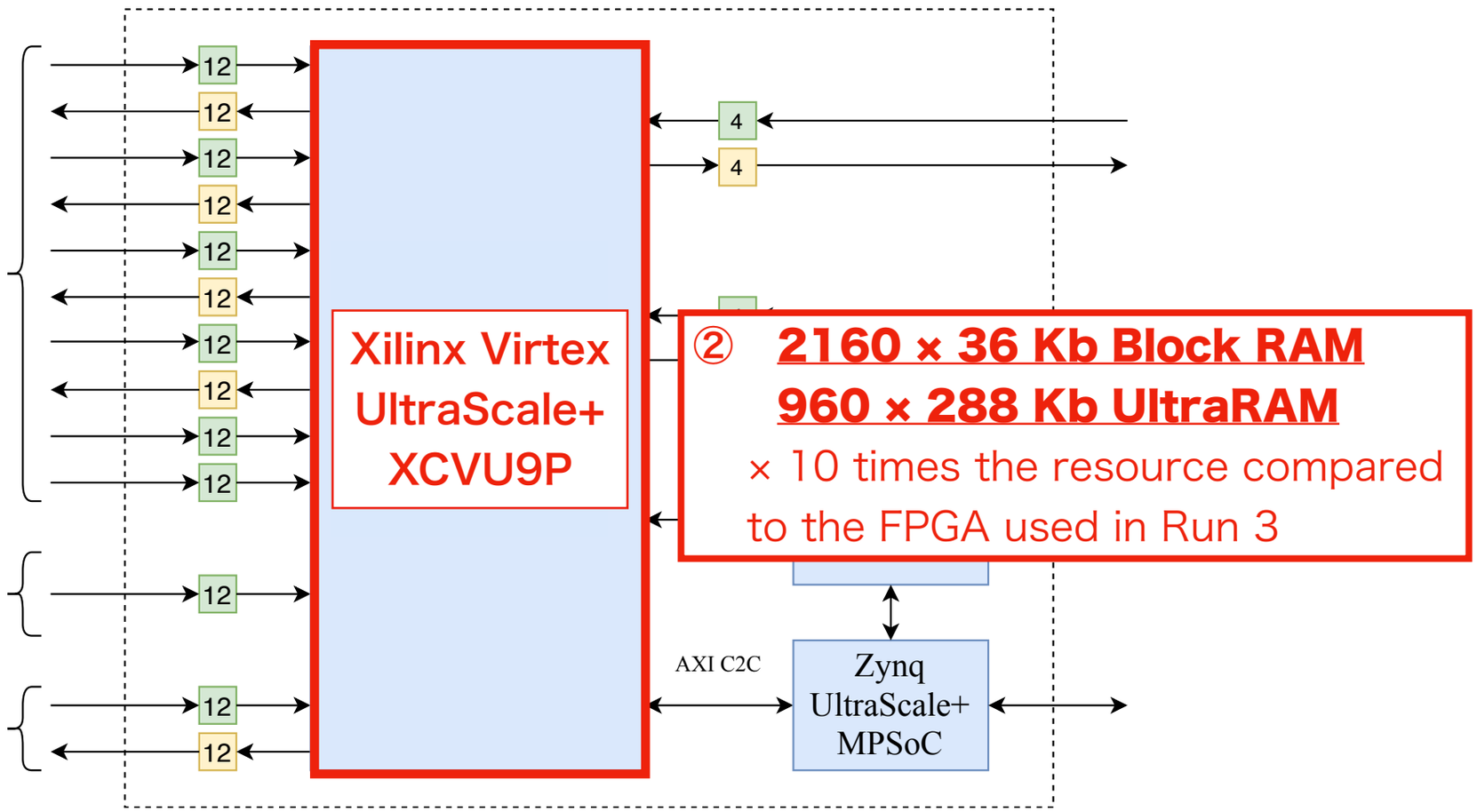
① Optical interfaces are placed to use **GTY*** connection

For TGC BW, TGC EI (~ 6700 ch)
8.0 Gbps/lane

For NSW, RPC BIS78, Tile
6.4 - 9.6 Gbps/lane

For MDT
9.6 Gbps/lane

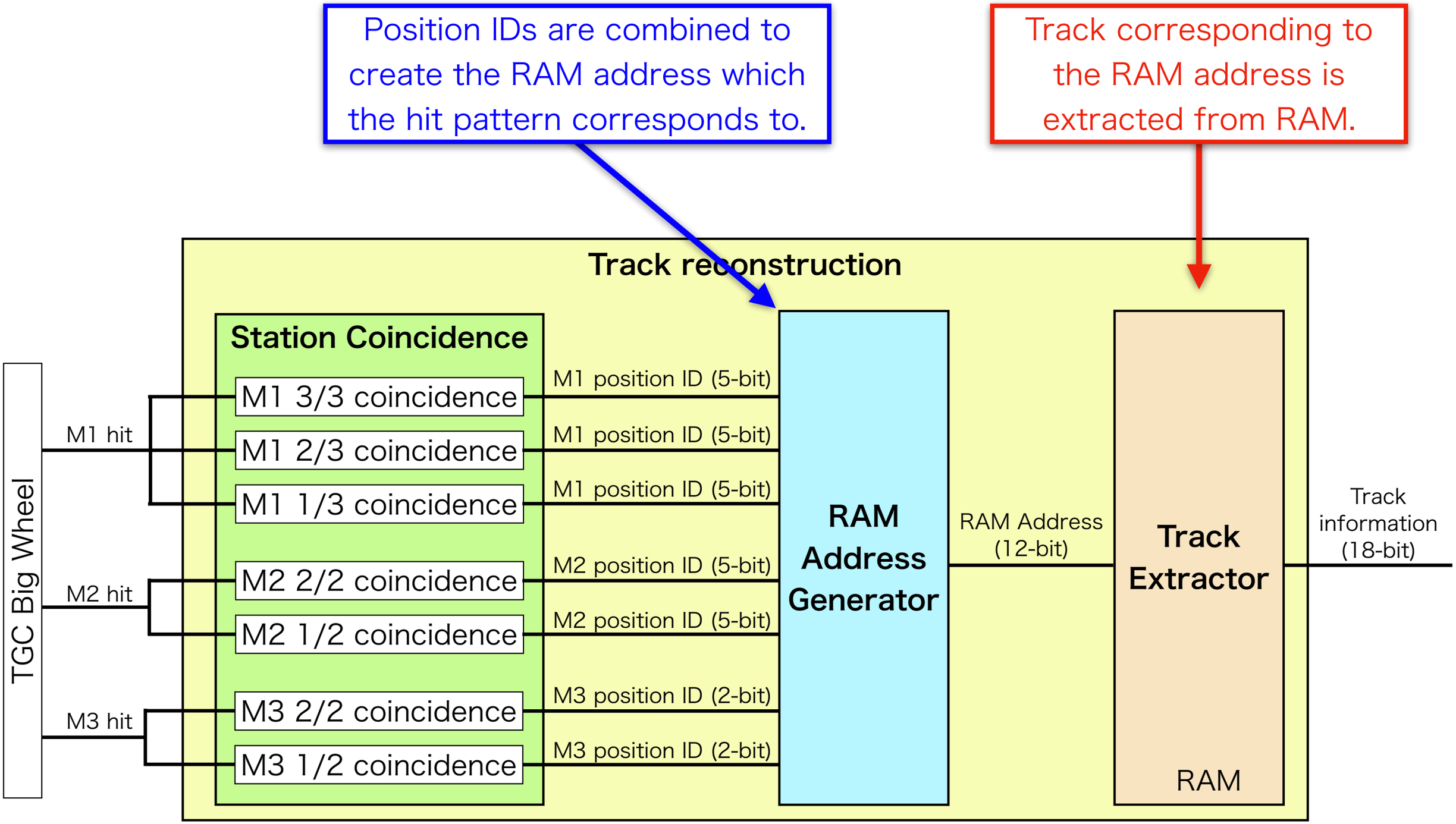
Schematic of Sector Logic



*** GTY: multi-gigabit transceivers for Xilinx UltraScale FPGAs**

- The design of schematic and layout is ongoing.

Firmware implementation for track reconstruction



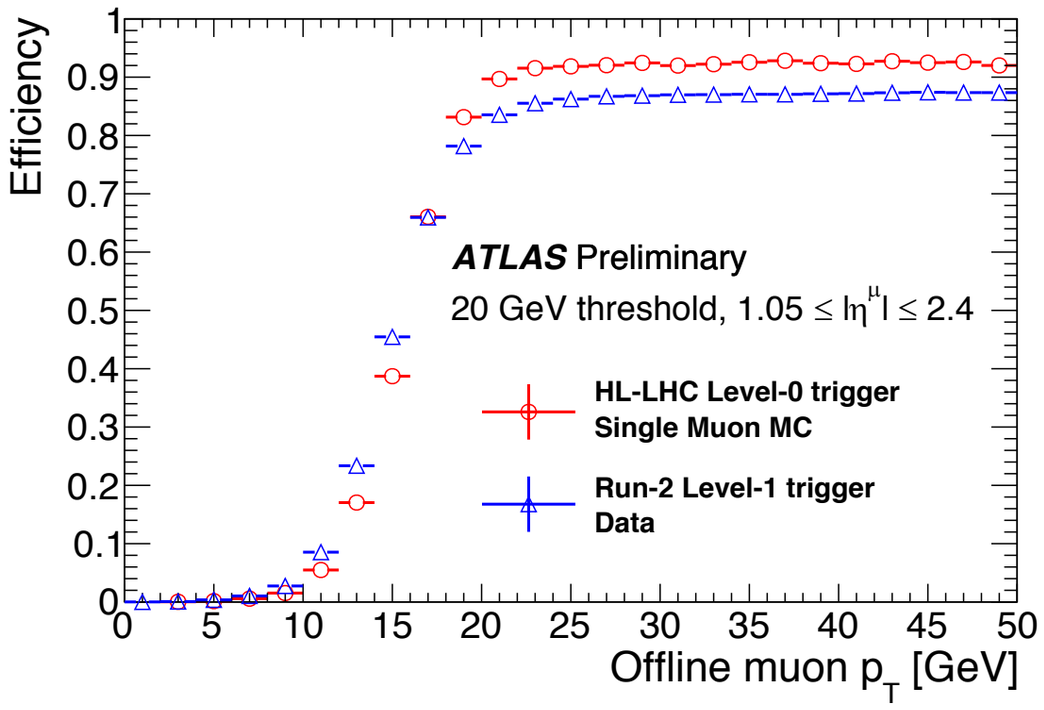
Performance of Level-0 endcap muon trigger in HL-LHC

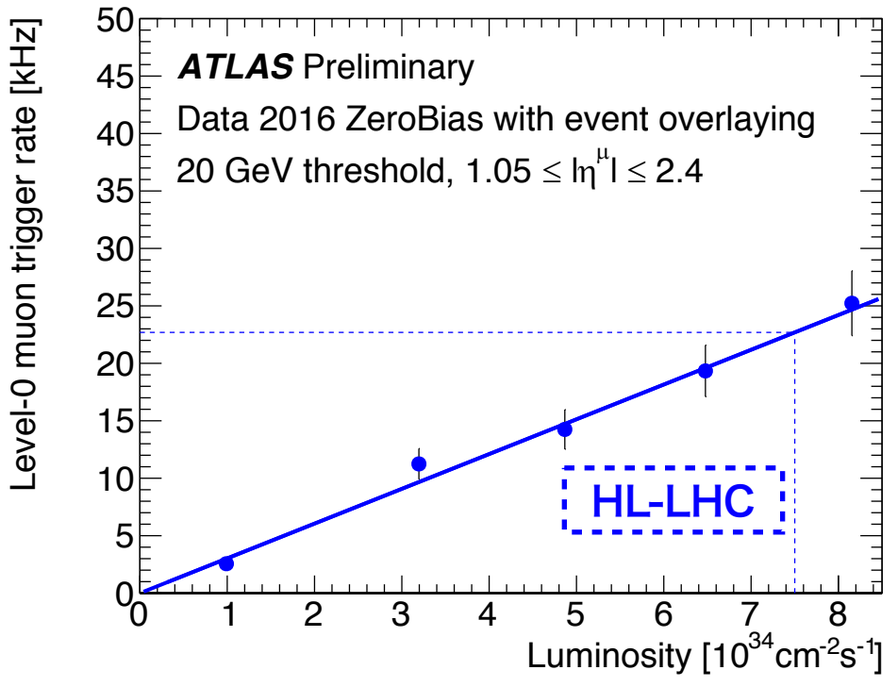
Efficiency

- Expected efficiency of the new trigger algorithm with respect to offline muons in an MC sample. Compared to Run 2 trigger.
  - **Higher efficiency (~ 4%)** in the plateau region due to the looser coincidence.
  - **Better rejection** for low p_T muons.

Trigger rate

- Estimated trigger rate from Run-2 data taken with random trigger to reproduce higher luminosity expected in HL-LHC.
  - Rate for 20 GeV threshold is about **23 kHz .**
    (constitutes only about **2.3%** of the assumed total Level-0 trigger rate of 1 MHz)
  - Further rate reduction in the next step with MDT is expected.





ATLAS L0Muon Trigger Public Results

Summary

- Continuous upgrades of the hardware-based (Level-1/0) endcap muon trigger is planned for Run 3 and HL-LHC.

Run 3

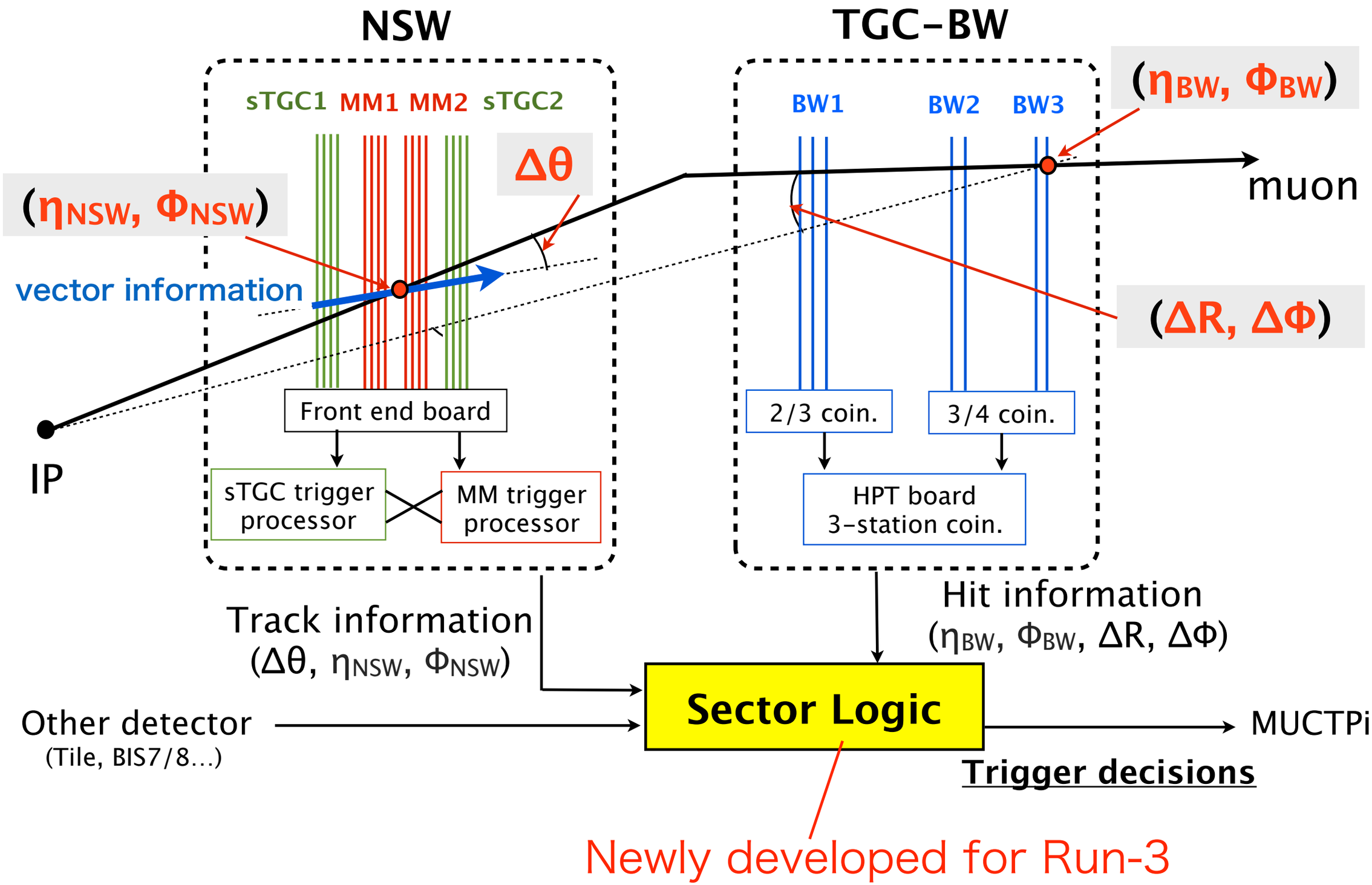
- New inner muon detectors with fine track information will be installed.
  - ▶New trigger processor board (SL) has been produced for Run 3.
- New trigger using new detectors shows higher reduction of low p_T muons compared to current trigger system.
- Estimated Level-1 endcap muon trigger rate for 20 GeV threshold is **~ 13 kHz** .
  (@ 2×10^{34} $cm^{-2}s^{-1}$)

HL-LHC

- Trigger and readout electronics will be replaced.
  - ▶Fast track segment reconstruction will be implemented.
  - ▶Preliminary design of the trigger processor board and firmware has been made.
- New trigger shows ~ 4% higher efficiency than current trigger system.
- Estimated Level-0 endcap muon trigger rate for 20 GeV threshold is **~ 23 kHz** .
  (@ 7.5×10^{34} $cm^{-2}s^{-1}$)
  - ▶Further rate reduction is expected by MDT track trigger.

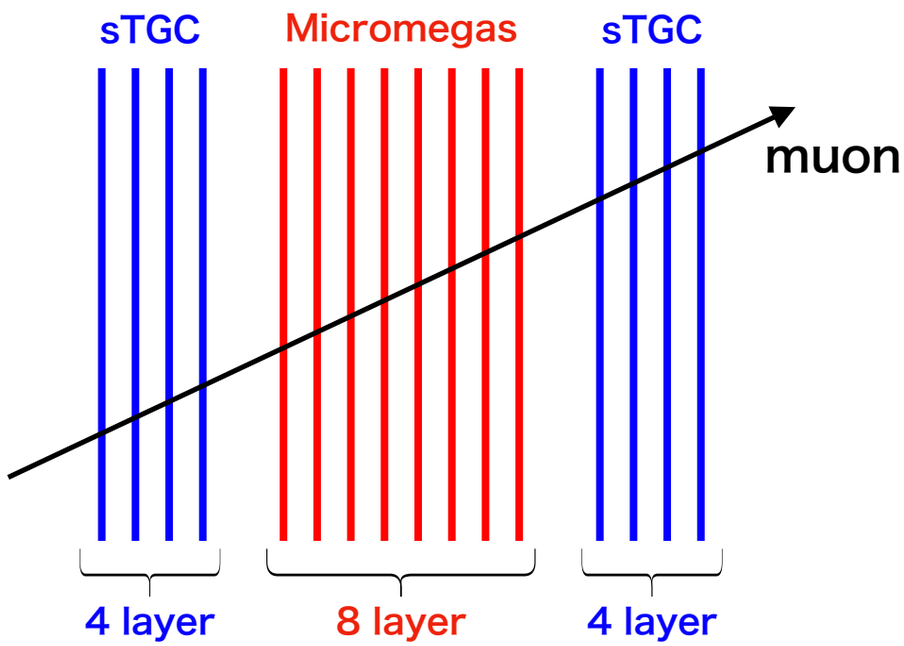
Back up

Endcap muon trigger system in Run 3

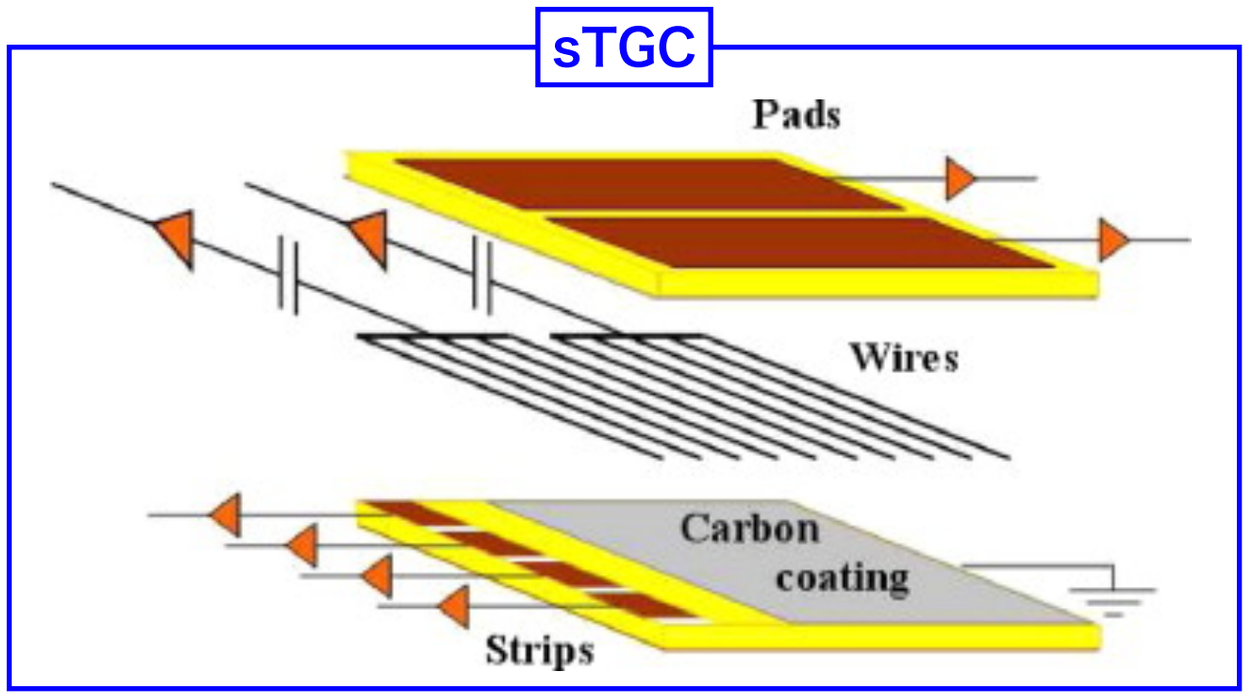


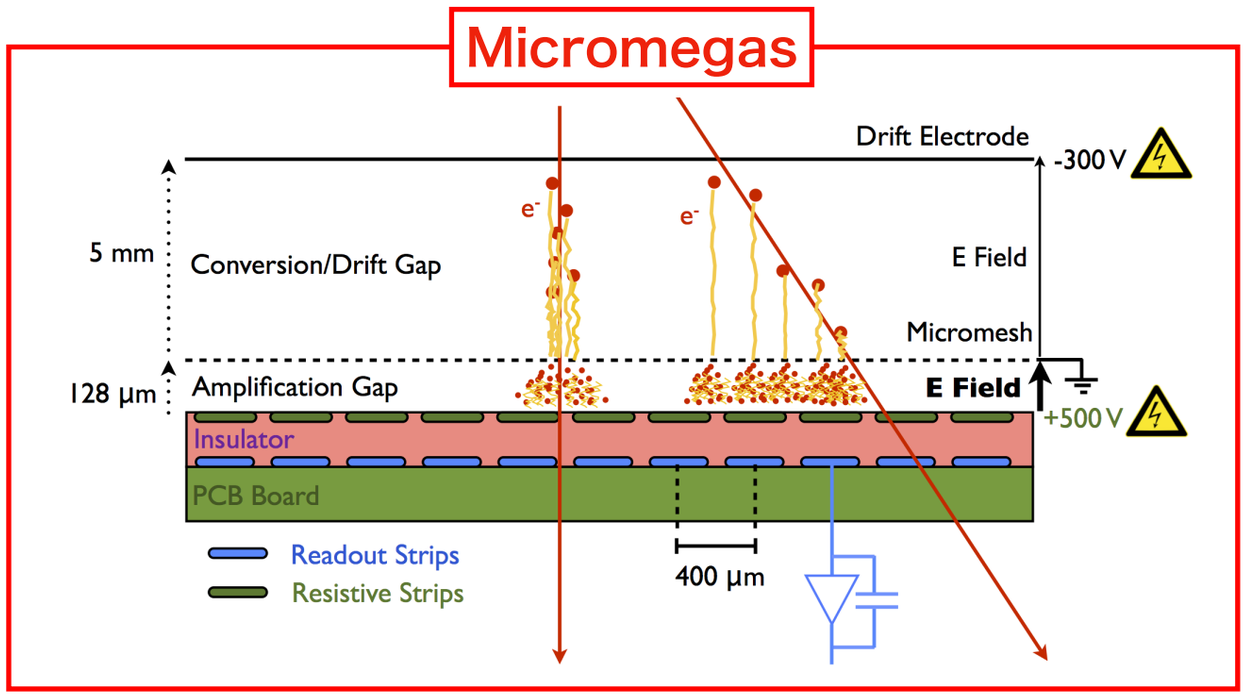
New Small Wheel

- Consist of small-strip TGC and Micromegas
  - **sTGC (small strip TGC)**
    - Strips with a 3.2mm pitch for precision readout (Current strip width of TGC is > 15 mm)
    - Cathode plane on the other side has pads for triggering
  - **Micromegas (micro mesh gaseous structure)**
    - Main tracking chamber for precise segment reconstruction
    - 8 layers are sandwiched by 4 layers of sTGC

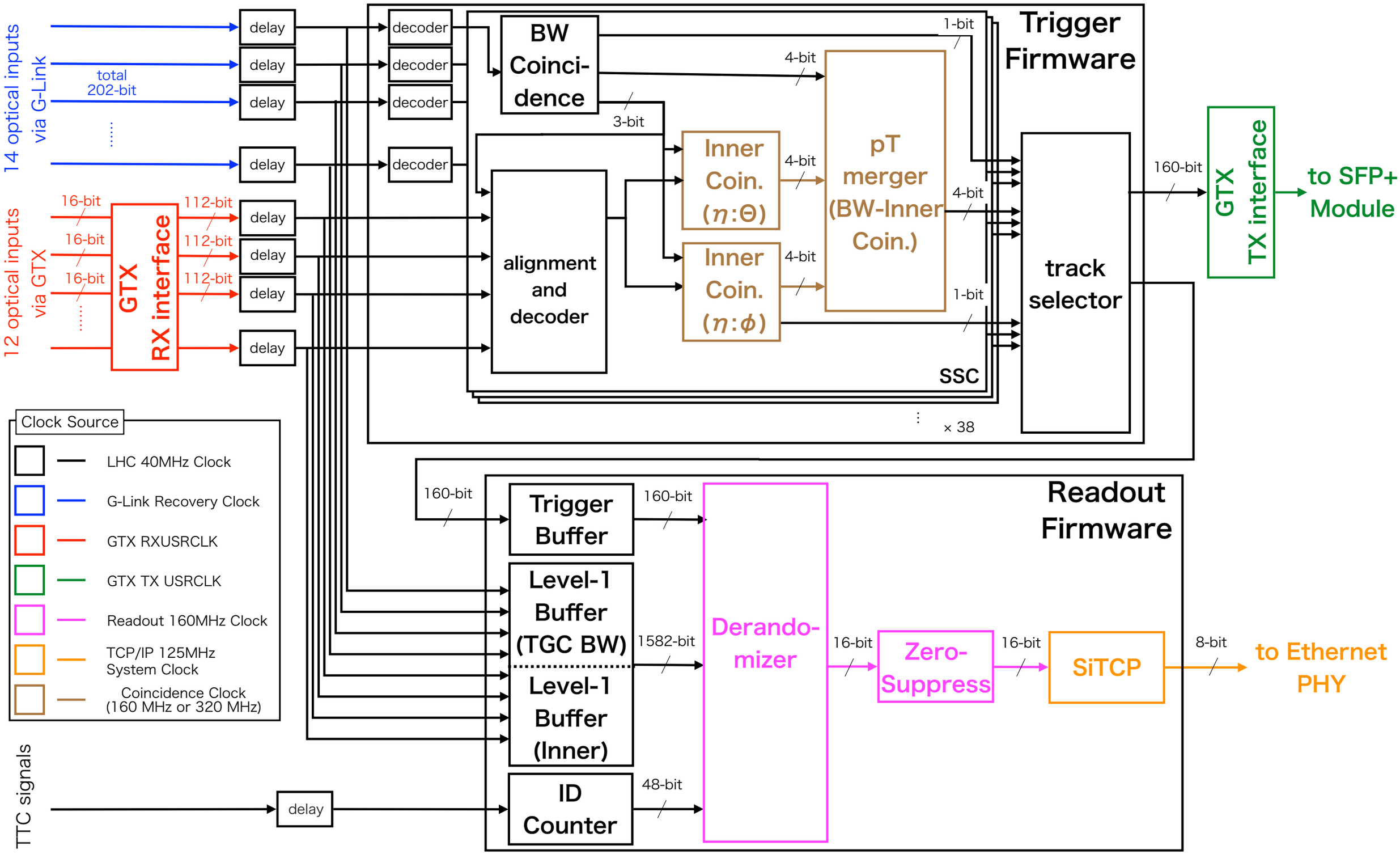


Position resolution : ~ 30 μm
Angle resolution : ~ 0.3 mrad





Block diagram of SL firmware in Run 3



Readout logic in Run-3

① L1 Buffer :
Stores data from detectors until the L1 Accept signal arrives

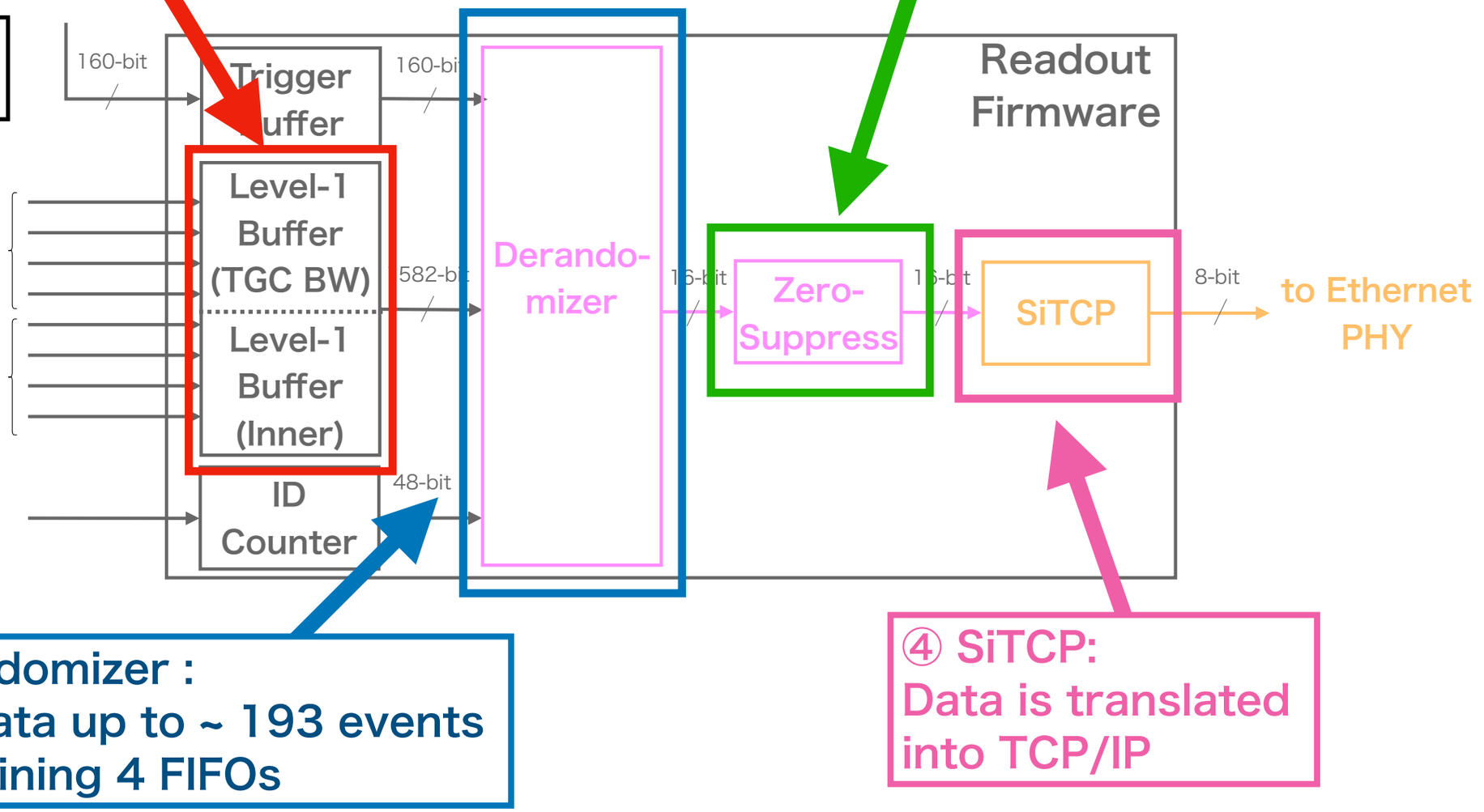
③ Zero Suppress:
Data suppression by rejecting “zero” data

Trigger decision information from Trigger logic

Hit information from TGC BW

Hit information from Inner muon detectors

TTC signals



② Derandomizer :
Buffer data up to ~ 193 events by combining 4 FIFOs

④ SiTCP:
Data is translated into TCP/IP

Clock Source

LHC 40 MHz clock

Readout 160 MHz clock

TCP/IP 125 MHz system clock

FPGA resource utilization in Run 3

Resource	Utilization	Available	Utilization %
LUT	32468	254200	12.77
BRAM	479.50	795	60.31
I/O	401	500	80.20
GTX	12	16	75.00

- Resource utilization is calculated by Vivado software.
  - Firmware includes full readout and trigger firmware.
- BRAMs are mainly used for large LUTs for coincidence logics.
  - TGC BW coincidence : ~ 9.6%
  - NSW coincidence : ~ 24.7%
  - RPC coincidence : ~ 7.5%

Estimated latency requirement in Run3

Latency contributions of New Sector Logic in units of BC (25 ns)

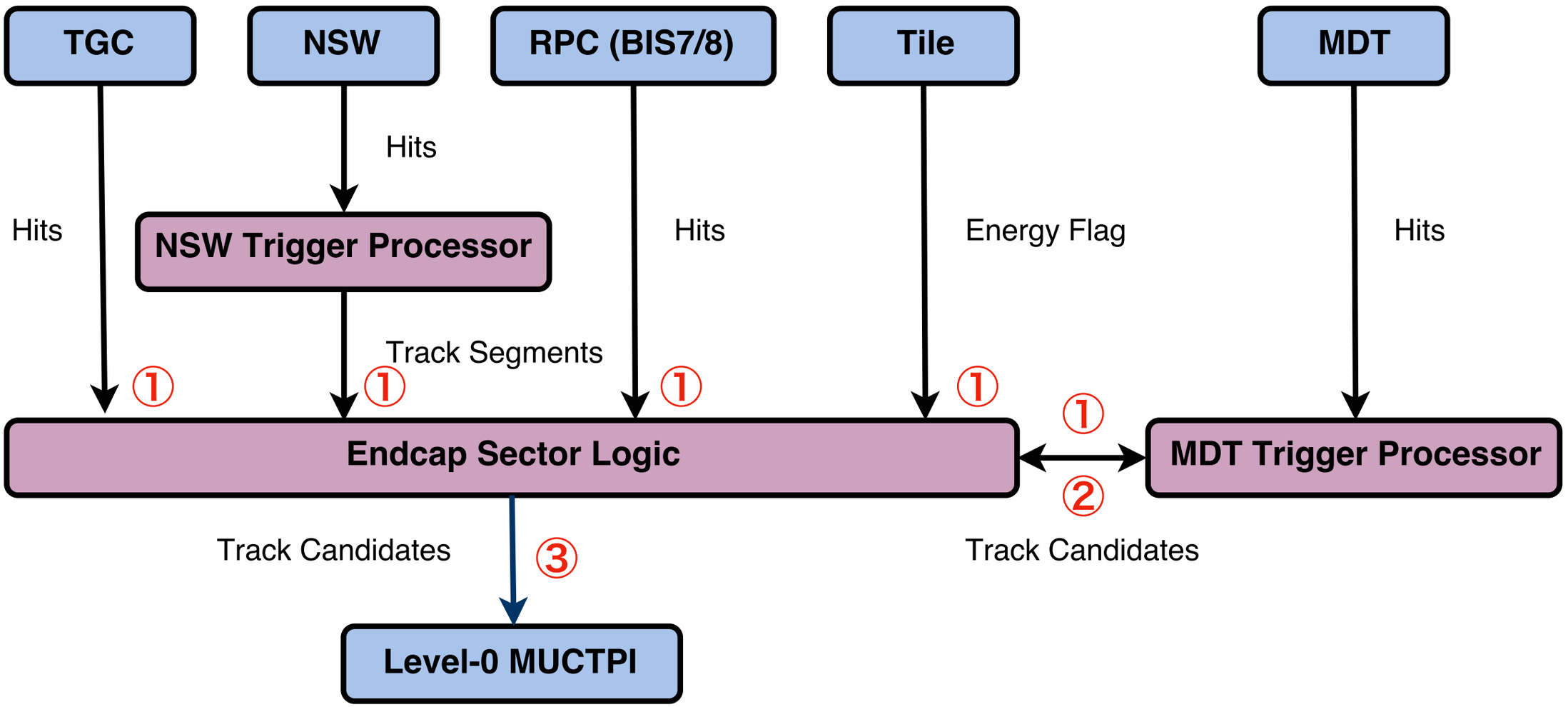
Latency to process NSW signals

Receive signal from NSW		41.1
Optical Rx + De-serializer	2.5	44
Variable Delay	1	45
Decoding/Alignment of NSW data (LUT)	1	46

Receive signals from BW		37
Optical Rx + De-serializer	2	39
TGC R-Phi coincidence (LUT)	2	41
Waiting for NSW signals	**5**	46
BW - NSW coincidence (LUT)	2	48
Track selection + p_{T} encoding	1	49
Serializer (128 bit/clk., 6.4 Gb/s) + Optical Tx	2	51
Optical fibre to MUCTPI (10 m)	2	53

- New Sector Logic will receive NSW signals 41.1 BCs after bunch crossing
  - Deserializing and decoding will take ~ 4.5 BCs after receiving signals
  - NSW coincidence will start at 46 BCs after bunch crossing
- Coincidence between TGC BW and NSW must be finished in 2 BCs (50 ns)

Level-0 endcap muon trigger system

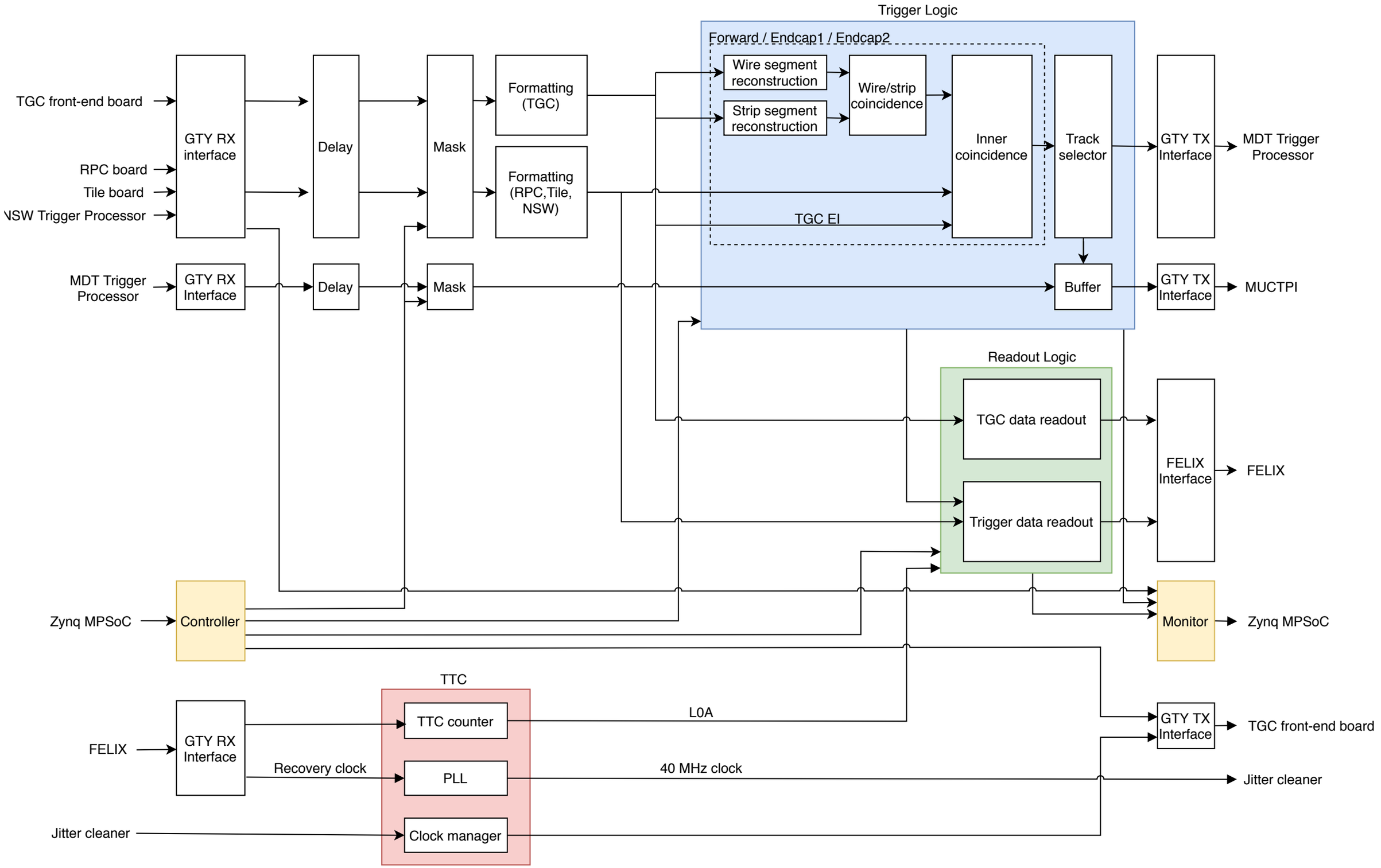


① Sector Logic (SL) receives hit and track information from TGC, NSW, RPC and Tile, and provides track candidates to MDT trigger processor.

② MDT trigger processor recalculates the track candidate p_T with better momentum resolution using MDT hits, and sends them back to SL.

③ SL sends the final candidates to MUCTPI.

Block diagram of SL firmware in HL-LHC



Estimated FPGA resource utilization in HL-LHC

	BRAM (Mb)	URAM (Mb)	HP I/O	GTY
Availability	75.9	270.0	448	120
Trigger Logic	20.5	123	-	-
Readout Logic	23.8	-	-	-
Interface	-	-	-	90 - 92
Control/monitor	-	-	O(10)	-
Total	44.3	120	O(10)	90 - 92

- Estimation based on extrapolation from resource utilization of partially developed firmware.
- Largest contribution to the URAM utilization is the TGC wire track reconstruction.

Estimated latency requirement in HL-LHC

Estimated latency contributions of Sector Logic in HL-LHC

Contents	Latency
TGC hit signal arrival	0.888 μs
Coincidence of TGC BW	1.013 μs
TGC BW and TGC EI coincidence	1.063 μs
TGC BW and RPC BIS78 coincidence	1.360 μs
NSW track candidate and TileCal signal arrival	1.425 μs
TGC BW and NSW (TileCal) coincidence	1.450 μs
Final selection of track candidate	1.475 μs
⋮	⋮

0.125 μs

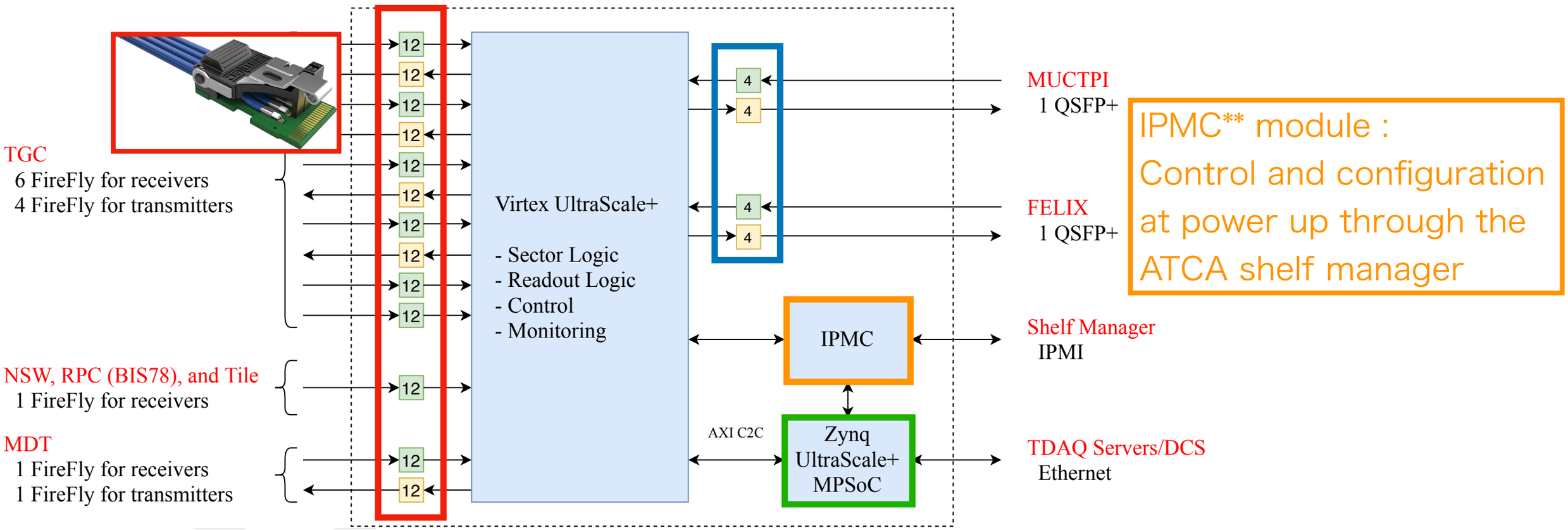
- The TGC track reconstruction is required to be finished in **0.125 μs**

Hardware design of Sector Logic in HL-LHC

- Xilinx Virtex UltraScale+ is implemented on a ATCA* blade.

Firefly module :
Handle 12 channels up to
16 Gbps per channel

QSFP+ module :
Handle 4 channels up to
10 Gbps per channel



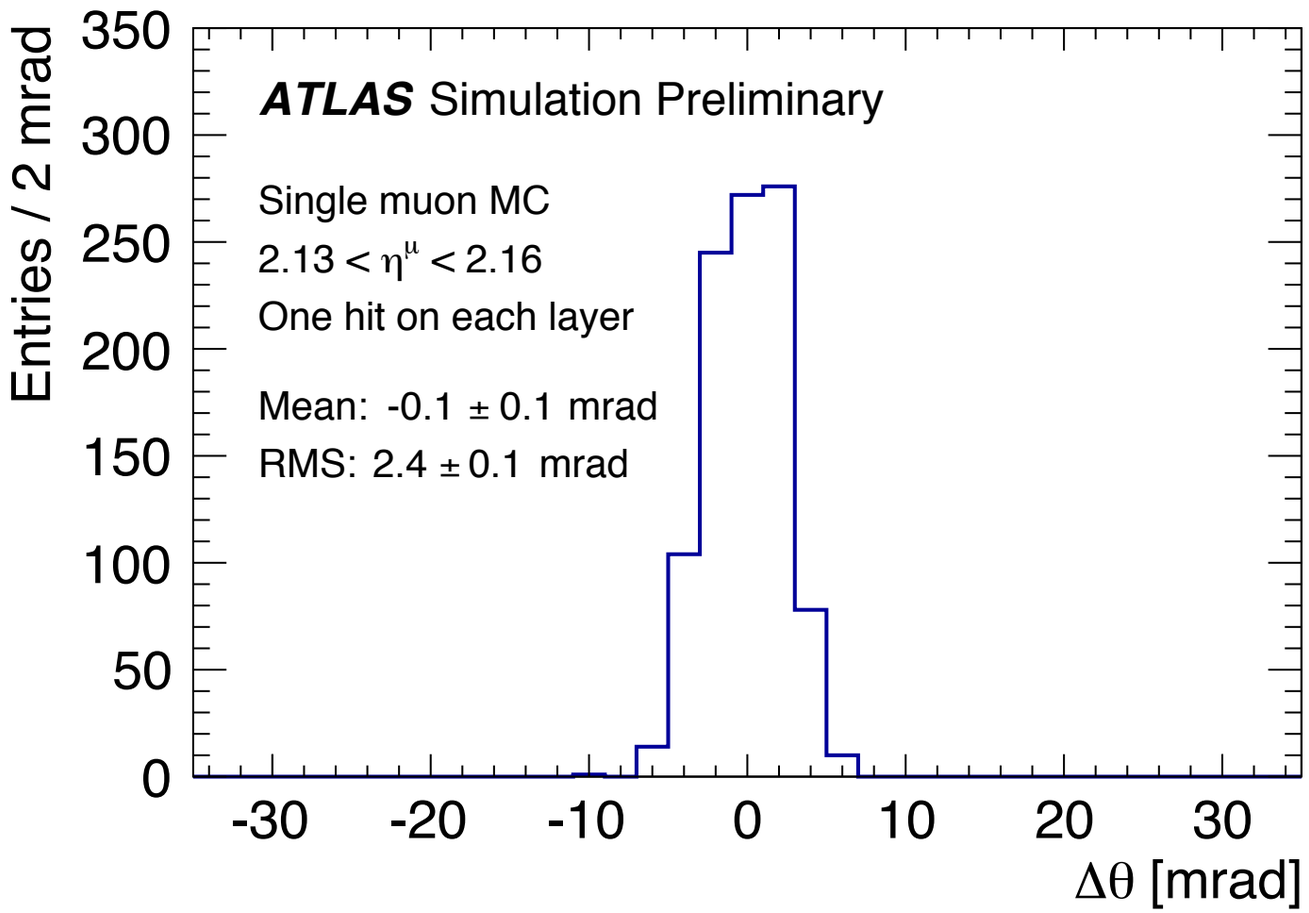
IPMC** module :
Control and configuration
at power up through the
ATCA shelf manager

*Advanced Telecommunication Computing Architecture
** Intelligent Platform Management Controller
*** Multiprocessor System-on-chip

MPSoC*** mezzanine card :
Interface for the ATLAS Run Control,
Configuration and Monitoring

Initial test of track segmentation

- A test firmware of TGC pattern matching algorithm is implemented in an FPGA to estimate performance.



ATLAS L0Muon Trigger Public Results

- Test result with the evaluation kit VCU118.
  - It shows **high efficiency and better angular resolution.**

- Expected memory usage for the full η range is about 100 Mbit, which is one-third of 345.9 Mbit of RAM resources on XCVU9P.