22nd Real Time Conference (Virtual)

# Development of next-generation timing system for the Japan Proton Accelerator Research Complex

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J-PARC Center

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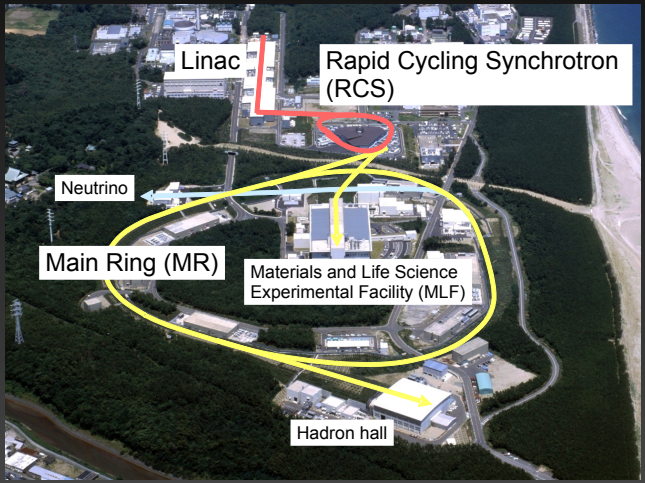
# Contents

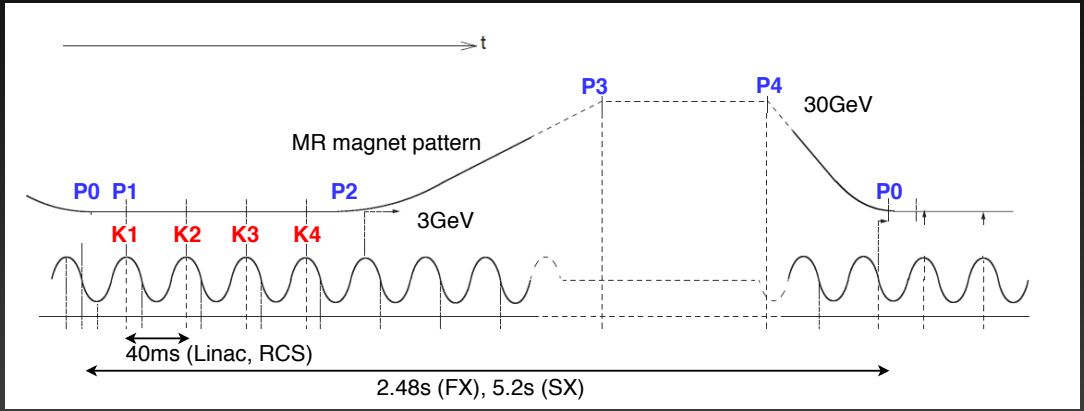
# Japan Proton Accelerator Research Complex (J-PARC)




- Accelerators: 400 MeV linac, 3 GeV RCS, 30 GeV Main Ring (MR)
- Experimental facilities: MLF (n, $\mu$), Hadron hall, Neutrino
- Beam operation started in 2006

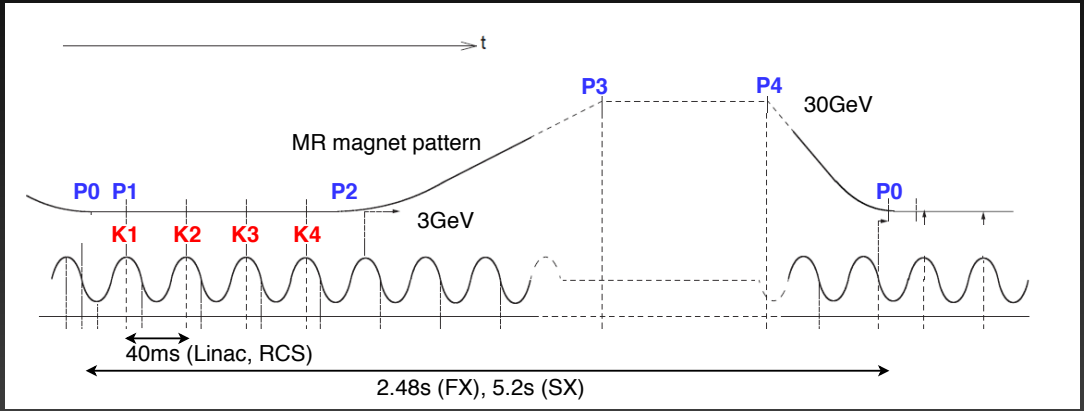
- High intensity: 1 MW (RCS), 750 kW (MR)
- A precise and stable timing system is necessary to avoid beam losses and residual activation
  - jitter below 1 ns

# J-PARC timing chart



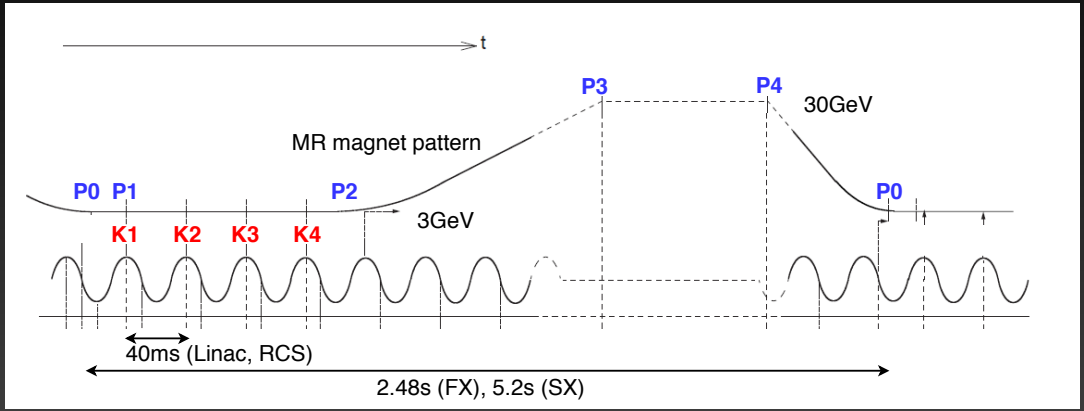

- MR accelerates protons from 3 GeV to 30 GeV at repetition period of 2.48 s (FX) or 5.2 s (SX)
- J-PARC machine cycle defined by MR cycle

# J-PARC timing chart




- Linac, RCS running at 25 Hz rep rate: Tick of J-PARC timing
- Four RCS beams injected to MR, others (FX: 58, SX: 126) delivered to MLF
- Beam parameters (intensity, macro pulse width, chopping width, injection painting) different for destinations

# J-PARC timing chart




- Role of timing system: to give appropriate instructions to the accelerator devices for various operating conditions
- Continuous user operation / single shot for commissioning / etc...

# Categories of J-PARC timing signal

**Scheduled timing:**

- Defined by the programmed delay from the 25 Hz reference trigger sent from the central control building (CCB)
- Most devices use scheduled timing

**Synchronization timing:**

- Generated by the accelerator devices for synchronization to the beams
- Linac chopper gate, RCS extraction kicker, MR injection kicker, etc.

We focus on the scheduled timing in this presentation.

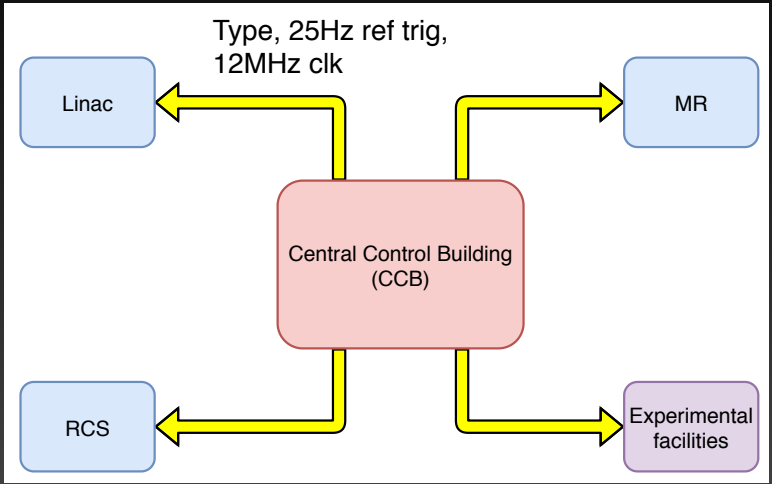
1. Introduction

2. Original timing system

3. Next-generation timing system

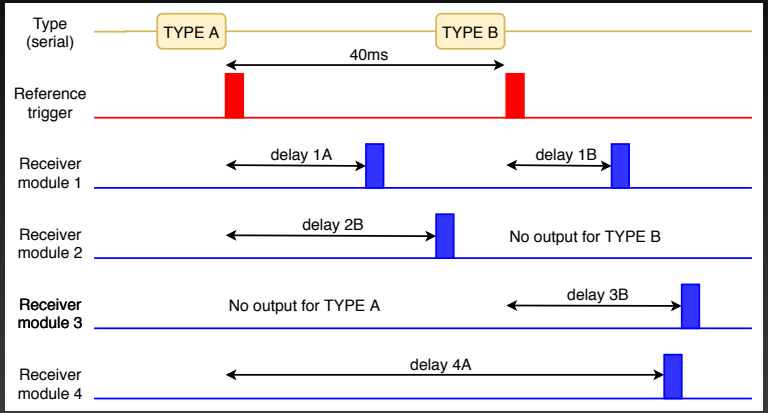
4. Conclusion

# Scheduled timing




- 25 Hz reference trigger, 12 MHz clock, and Type are sent from CCB to facilities
  Star configuration: same signal delivered
- Type represents the operation of next 25 Hz cycle

# Operating principle of scheduled timing




According to type, receivers work as follows:

- Output pulse with programmed delay
- No output
- Continue counting for longer delay beyond reference trigger

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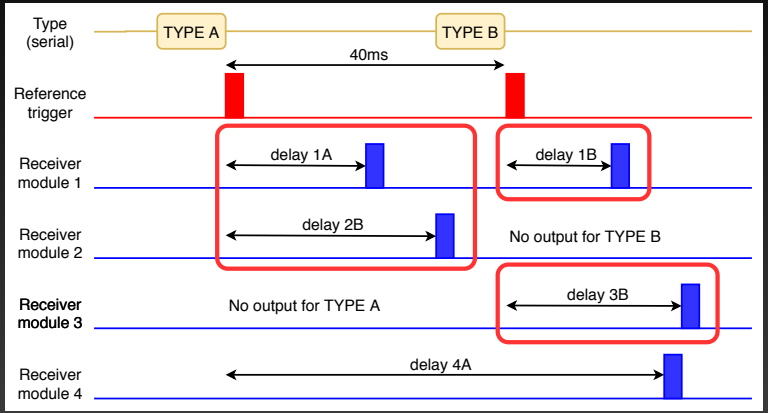


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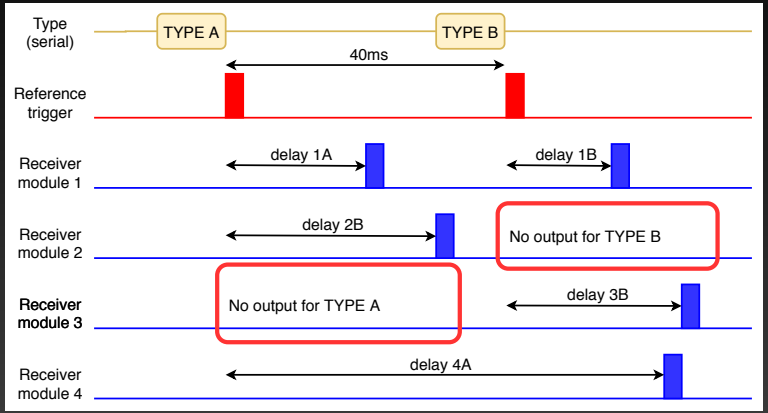


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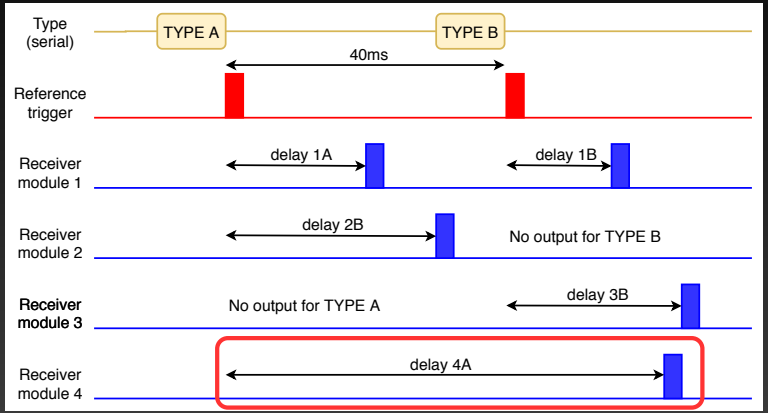


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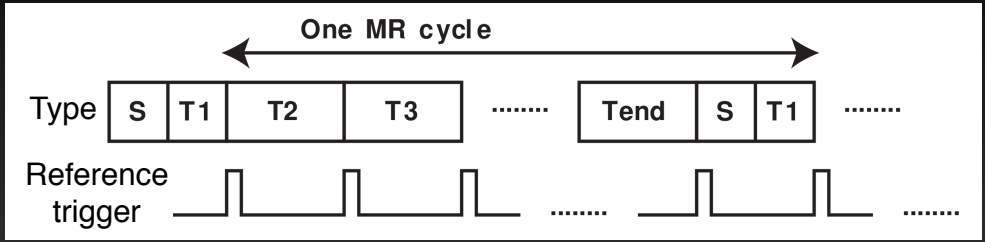
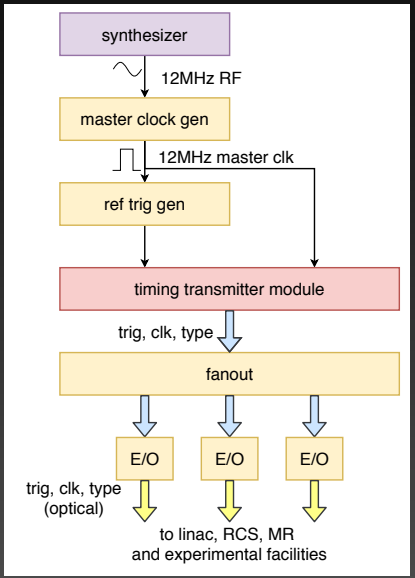



Type sequence:

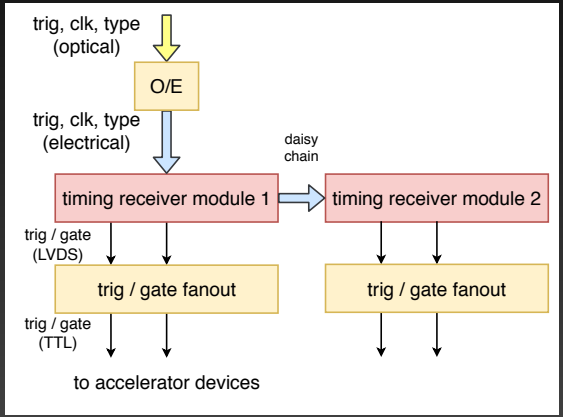
- A type sequence represents operation in a MR cycle
- End code or jump code indicates the end of cycle
- Changing type sequence, accelerator operation is switched
- Special word "S" sent additionally at the beginning of type sequence

# Timing transmitter station in the CCB




- High-precision synthesizer and clock generator generate 12 MHz master clock
- Reference trigger generated by counting clocks
- Timing transmitter module sends serialized 32-bit type code prior to reference trigger
  - MSB: special flag
  - Each 8-bit for linac, RCS, MR. 7-bit reserved
- Three signals sent to facilities via fanout and E/O

# Timing receiver station in the facilities

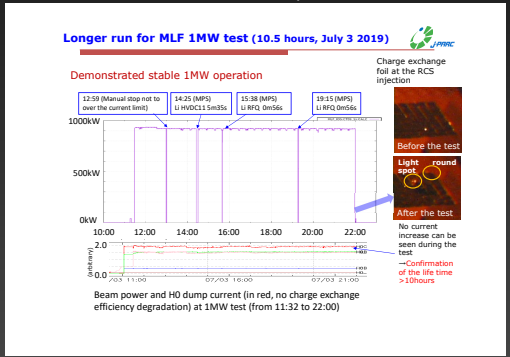



- Three delivered optical signals are input to the timing receiver module via O/E
- Receiver module picks up control word from LUT by taking specified 8-bit from the 32-bit type code
- Behaves as the operating principle in previous slide
- 96 MHz delay counter clock from 12 MHz clock by PLL
- Output level converted NIM modules
- Daisy chain possible

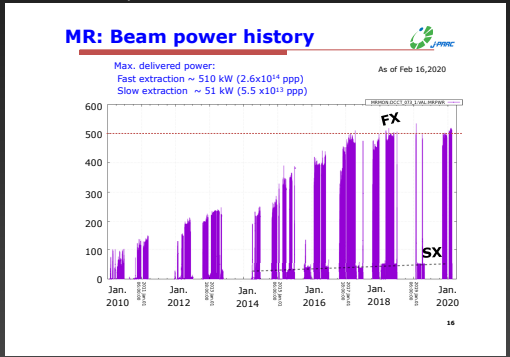
# Original timing system works nicely

The original timing system working without major problems since 2006.
The stable / precise timing system serving the high intensity beam operation.

RCS 1 MW continuous operation demo:




MR beam power reached 510 kW:



# Why next-generation system?

Optical component (Finisar v23826) was discontinued, no successors:



O/E, E/O modules are no longer in production and the original system cannot be maintained for longer period, while we have enough spare modules.

We started development of the next-generation system from 2016.

1. Introduction

2. Original timing system

3. Next-generation timing system

4. Conclusion

## Design considerations

- Impossible to replace whole system at once. Compatibility to the original system is most important

→ Popular timing system solutions (MRF, WR) not considered

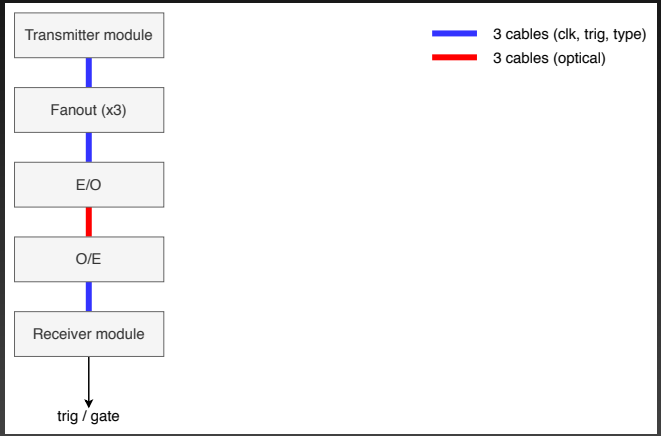
- Three cables per station is infrastructure burden
- Metal cable between O/E and receiver may pick up noises from pulsed PS or high intensity beam. Receiver hang ups experienced

→ High speed serial communication containing three signals on single optical cable

- A set of VME and NIM crates requires space and cost. MR control rooms have limited space (and budget)

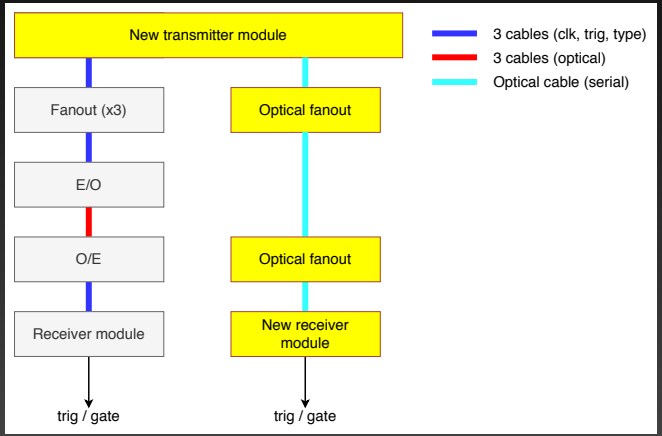
→ Small form factor (PLC) receiver also developed

# Configuration




- Yellow: newly developed modules
- New transmitter outputs serialized optical signal containing ref trig, clk, type
  - SFP as optical device
  - All connections are optical
- Optical fanout
- New receiver: VME and PLC. Works same as original
- Also outputs same three signals so that original receivers can be used as is

# Configuration

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- New transmitter outputs serialized optical signal containing ref trig, clk, type
  - SFP as optical device
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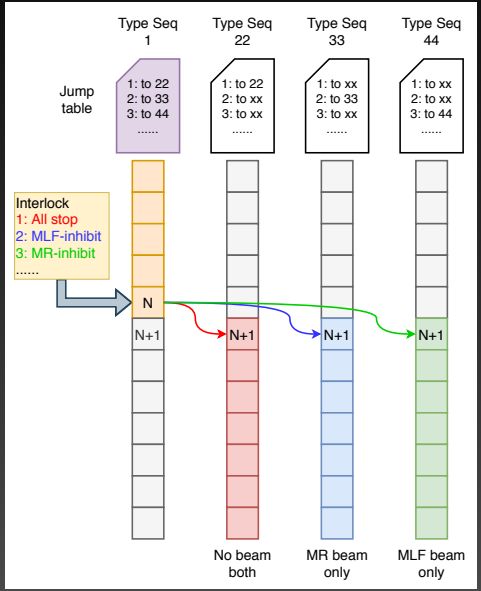
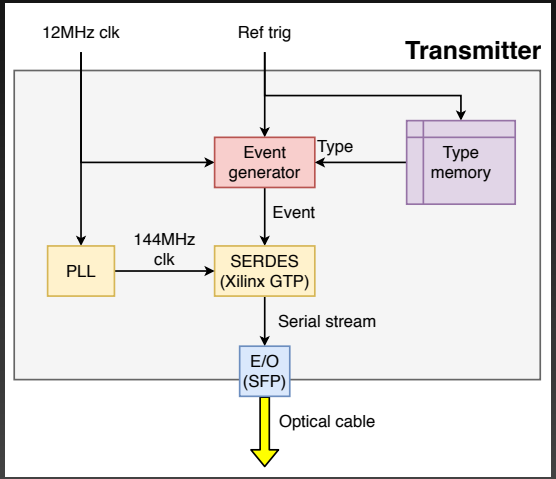
- Also outputs same three signals so that original receivers can be used as is

# New transmitter function: shift-jump




- In original system, switching of type sequence is allowed only the end of the type sequence
- "Beam-on" trigger for measurement is stopped when interlock by modifiying LUT by fast reflective memory network
- "Shift-jump" function: according to the jump table for the interlock types, the type sequence is switched so that beam-on trigger is suppressed

# High speed serial communication: transmitter




- At each reference trigger, type picked up from type memory
- New transmitter module generates an event every 12 MHz clock
  - Payload of high speed serial communication
- GTP on Xilinx Spartan-6 used
- Serial stream converted to optical signal by SFP module

# Protocol

- A sequence: 12 consecutive 8 bit words
  - Repetition at 12 MHz
  - K28.5 (comma), event (E), 10 bytes data
  - 8B/10B encoded, 1.44 Gbps
  - All events are used for generation of 12 MHz clock at receiver

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| sequence | K28.5 | E | D(p1) | D(p2) | D(p3) | D(p4) | D(p5) | D(p6) | D(p7) | D(p8) | D(p9) | D(p10) |

# Protocol

(1) Null event: sent when idle

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Null | K28.5 | D0.0 | D0.0 | D0.0 | D0.0 | D0.0 | D0.0 | D0.0 | D0.0 | D0.0 | D0.0 | D0.0 |

E(null)=D0.0 (0x00)

(2) Trigger event

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Trig | K28.5 | E(trig) | D0.0 | D0.0 | D0.0 | D0.0 | D0.0 | D0.0 | D0.0 | D0.0 | D0.0 | D0.0 |

E(trig)=D1.0 (0x01)

(3) Type event: before trigger

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Type | K28.5 | E(type) | type1 | type2 | type3 | type4 | D0.0 | D0.0 | D0.0 | D0.0 | D0.0 | D0.0 |

E(type)=D2.0 (0x02)

(4) S event: at beginning of type sequence

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| S | K28.5 | E(S) | D0.0 | D0.0 | D0.0 | D0.0 | D0.0 | D0.0 | D0.0 | D0.0 | D0.0 | D0.0 |

E(S)=D3.0 (0x03)

(S) S count event

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Scnt | K28.5 | E(Scnt) | Scnt1 | Scnt2 | Scnt3 | Scnt4 | D0.0 | D0.0 | D0.0 | D0.0 | D0.0 | D0.0 |

E(Scnt)=D4.0 (0x04)

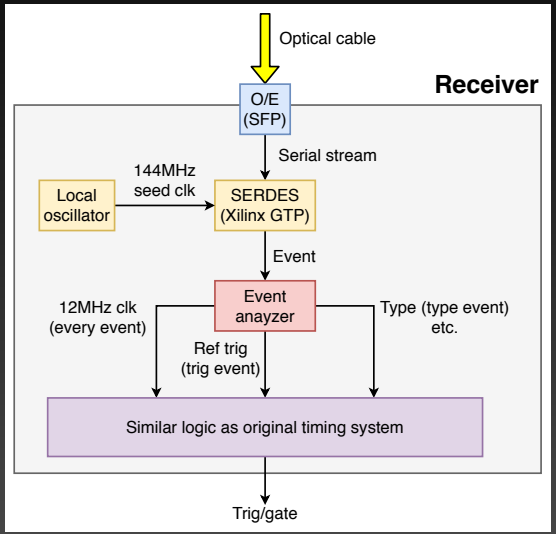
(6) trig count event

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Tcnt | K28.5 | E(Tcnt) | Tcnt1 | Tcnt2 | Tcnt3 | Tcnt4 | D0.0 | D0.0 | D0.0 | D0.0 | D0.0 | D0.0 |

E(Tcnt)=D5.0 (0x05)

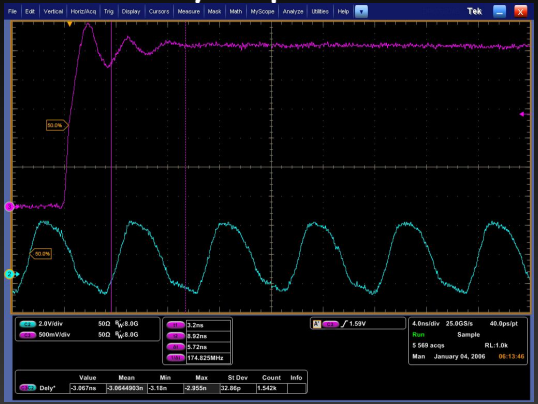
- Many reserved events

# High speed serial communication: receiver




- On the receiver GTP, Clock and Data Recovery (CDR) is used to decode the 144 MHz clock and data
- 12 MHz clock is generated looking at commas
- Event analyzer extracts trigger, type, and other information
- Clock, trigger, and type are fed into the same circuit as original modules
- As a whole, the new receiver behaves in the same way as the original system

# Pitfall: latency of pure GTP is not deteministic at power-up





- Phase of recovered 144 MHz clock different at each power-ups
  - Normal applications for data transfer do not care
- Critical issue for timing system
- Any solutions?

# Yes, solution found!

The solution is found in R. Giordano's TNS articles:

- R. Giordano and A. Aloisio, "Fixed-Latency, Multi-Gigabit Serial Links With Xilinx FPGAs," in IEEE Transactions on Nuclear Science, vol. 58, no. 1, pp. 194-201, Feb. 2011
- We appreciate their good work

We implemented fixed-latency logic according to the reference.



## Fixed-Latency, Multi-Gigabit Serial Links With Xilinx FPGAs

Raffaele Giordano and Alberto Aloisio

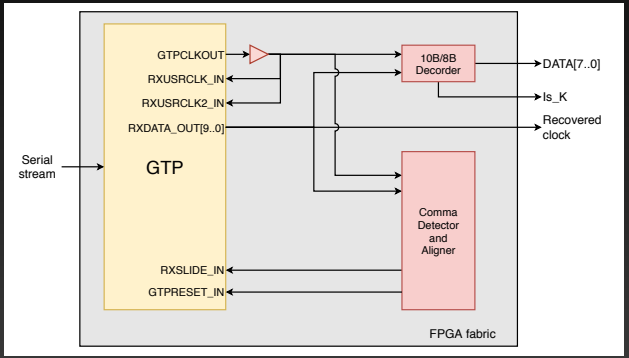
***Abstract*—Most of the off-the-shelf high-speed Serializer-Deserializer (SerDes) chips do not keep the same latency through the data-path after a reset, a loss of lock or a power cycle. This implementation choice is often made because fixed-latency operations re-**

higher precision is achieved with PTP when the latency of the up-link and down-link are constant and equal.

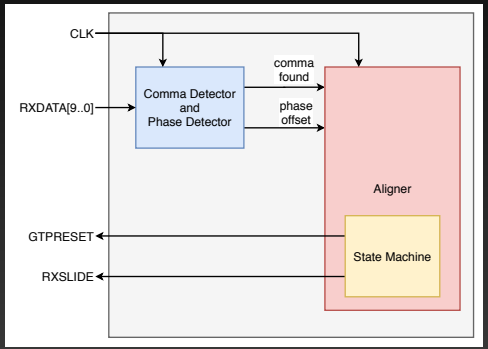
Fixed-latency links also find application in data-acquisition

# Fixed-latency logic implementation (receiver side)

Overview:




Comma detector and aligner (CDA):




- 10B/8B decoder and CDA are implemented in FPGA fabric, outside of GTP
- Phase offset is measured and fed to aligner
- If offset is even number of UI, RXSLIDE asserted necessary times to adjust phase
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With the logic, deterministic latency is realized.

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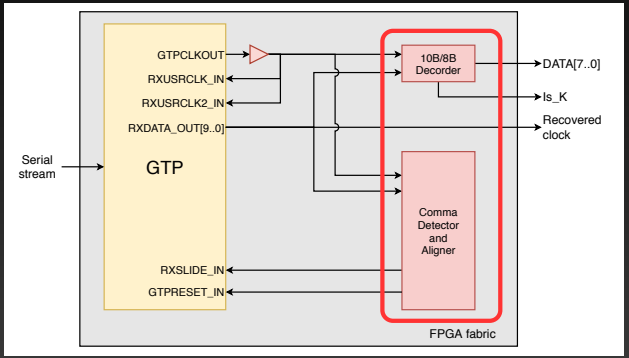


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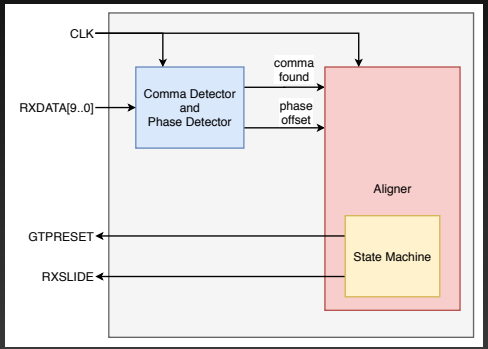


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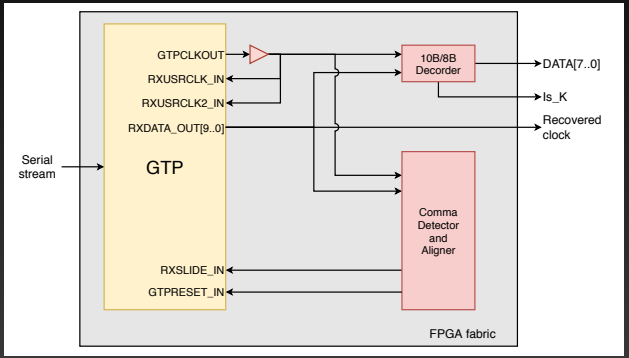


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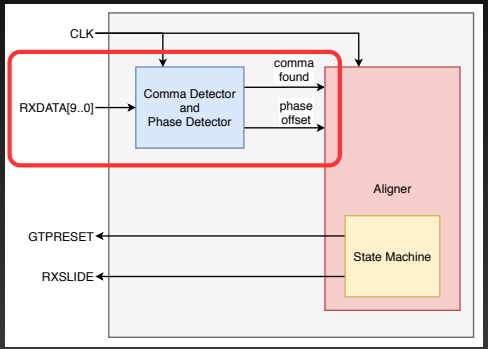


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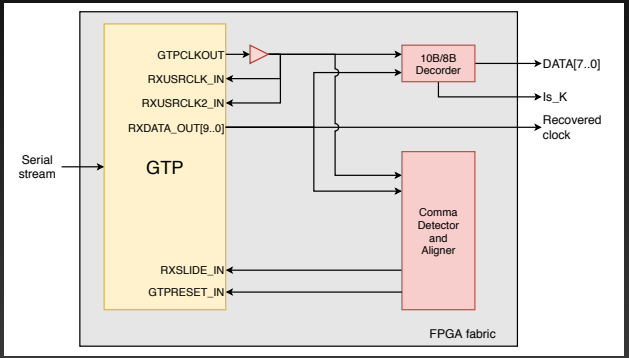


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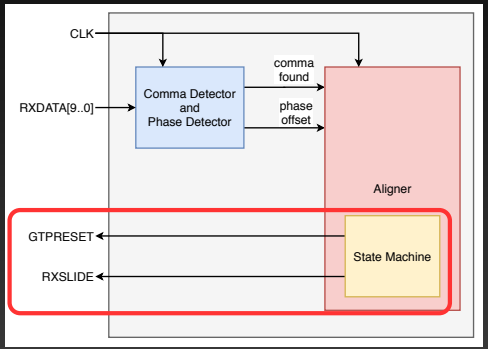


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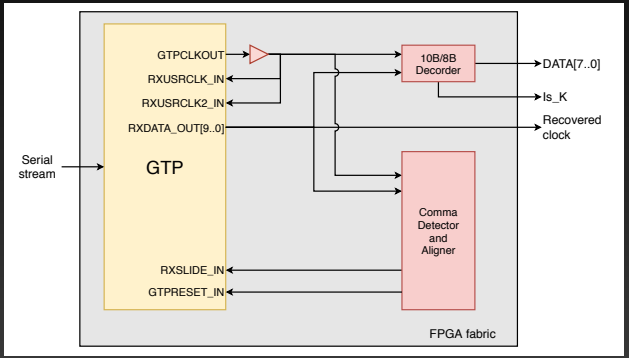


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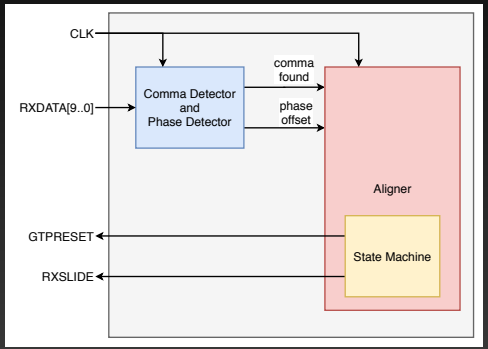


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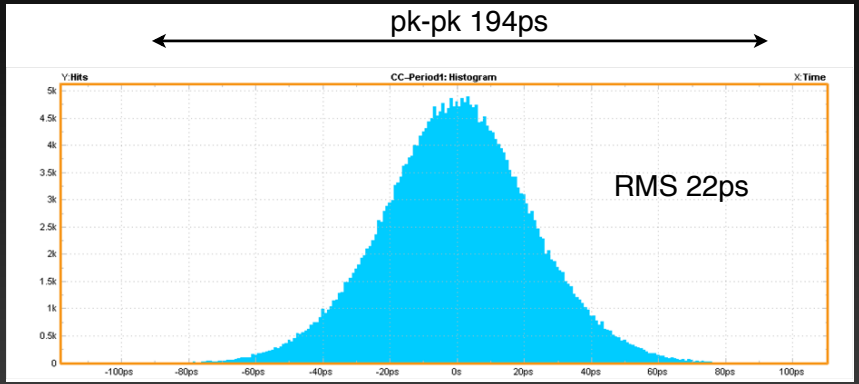
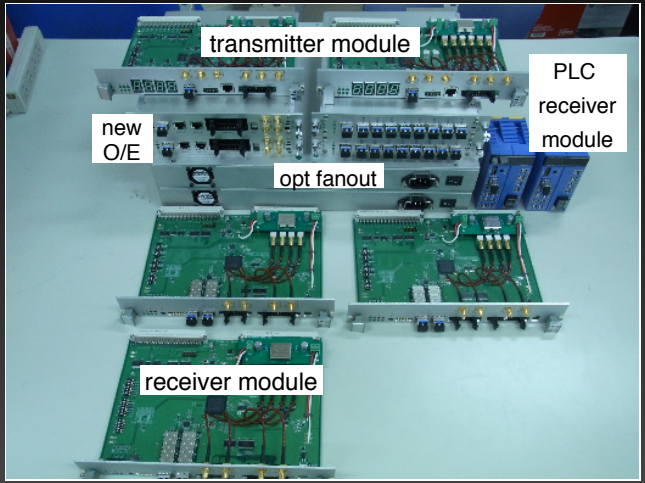
# 12 MHz clock jitter measurement by Tek DPOJET




- 12 MHz clock used for reference of 96 MHz counter clock and accelerator digital clocks (LLRF, etc)
- RMS 22 ps and pk-pk 200 ps, sufficiently low
- Trigger jitter similar (not measured by DPOJET)

Next-generation system performance confirmed.

# Current status




- Original transmitter module was replaced with new transmitter in January 2020
- Until now, 12 receiver stations with 36 new receiver modules completed at linac and RCS
- Another 12 receiver stations to be done in this FY
- PLC receiver modules will be installed at new power supply buildings in MR

# Conclusion

- J-PARC timing system is designed to fit the operation of the accelerator complex, which has multiple beam destinations
- Original system has been working nicely, while key optical component is obsolete. Next-generation timing system has been developed with emphasis on compatibility
- Next-generation system utilizes high speed serial communication technology. Fixed latency logic is implemented
- Successfully deployed in 2020

Note:
The serial communication framework is based on common technologies.
It can be implemented with newer FPGAs.
Next-generation system expected to be sustainable.