PAUL SCHERRER INSTITUT

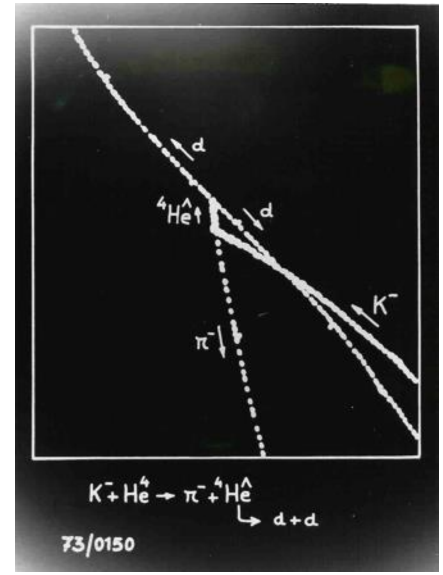
IEEE NPSS NUCLEAR & PLASMA SCIENCES SOCIETY

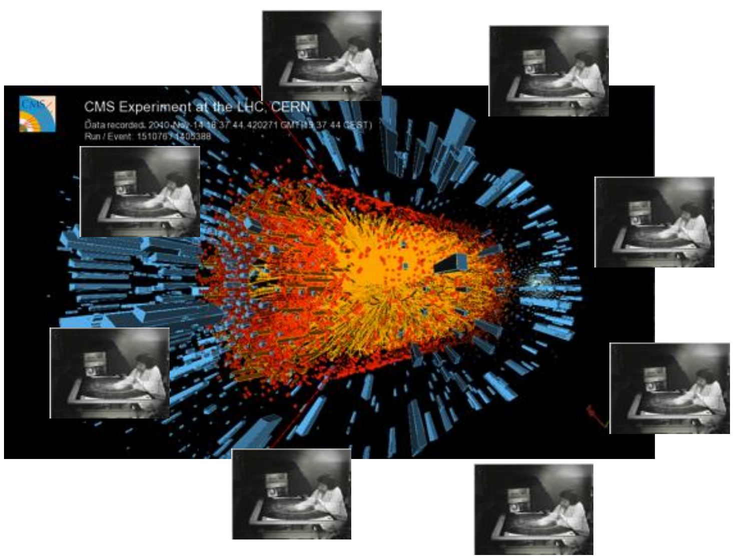
Paul Scherrer Institute, Switzerland

Stefan Ritt

Front-end Electronics, Waveform Digitizing and Signal Processing

“Manual” DAQ



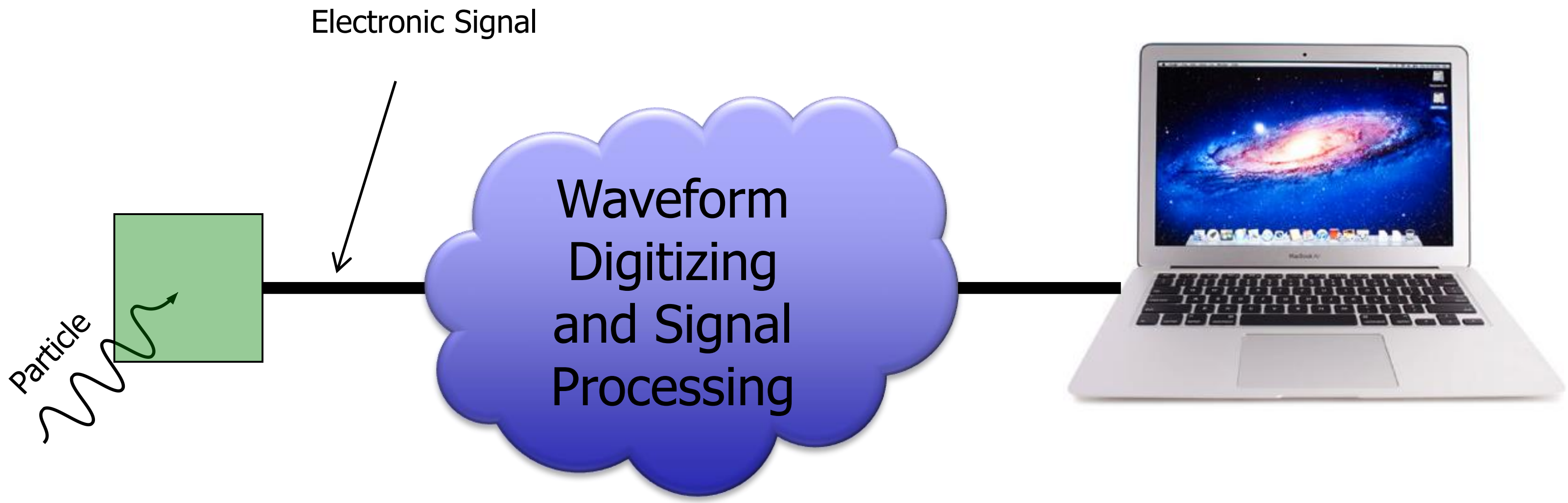


1000 tracks per 25 ns
A4 paper @ 5 g
Truck load @ 40 t

How much paper
per second?

200’000 t
5000 Trucks !!!

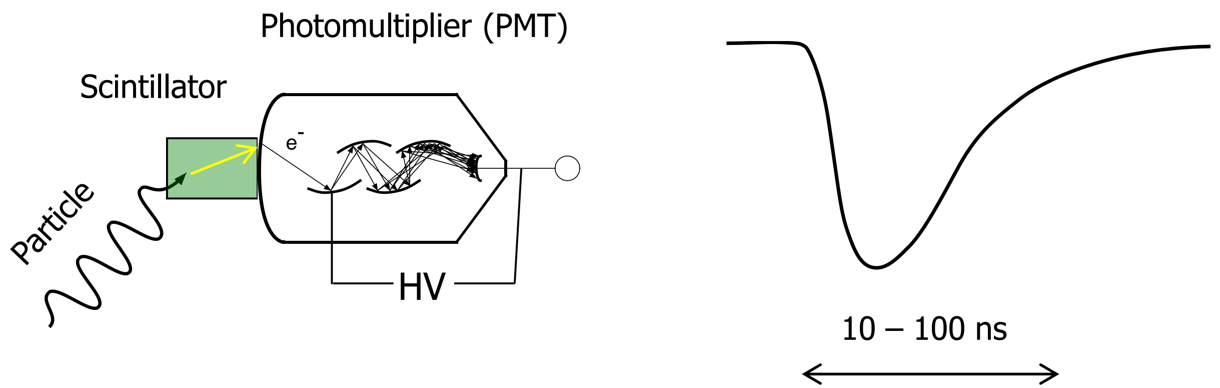
Electronic Signal Acquisition



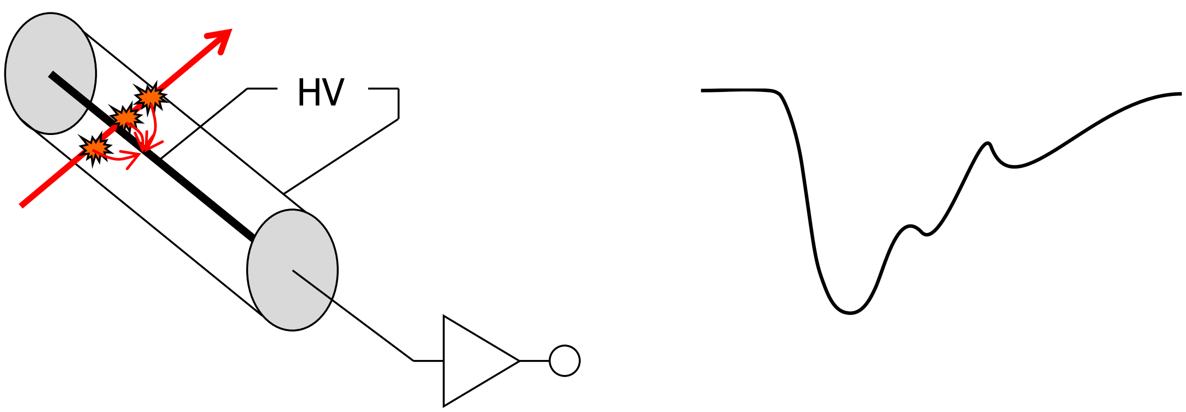
- ADC & TDC technologies
- Signal shaping
- Ultra-fast digitizing (>1 GSPS)
- Digital pulse processing
- Applications

Signals in particle physics

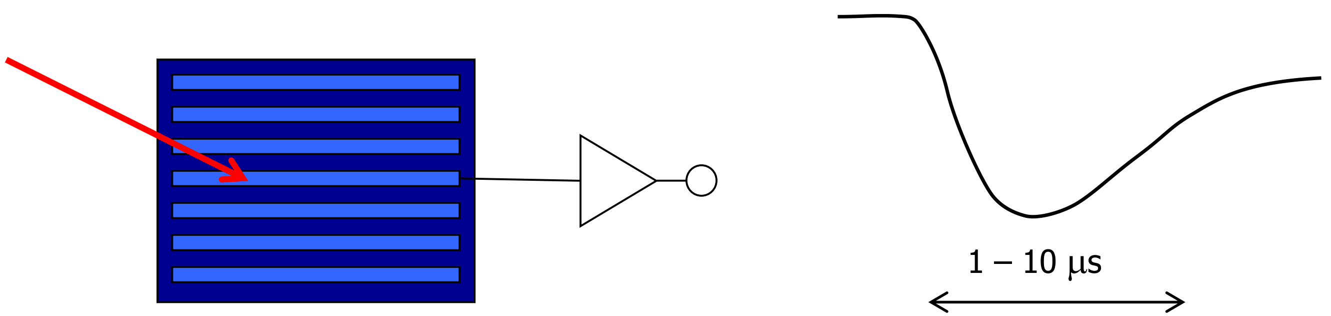
Scintillators (Plastic, Crystals, Noble Liquids, …)



Wire chambers
Straw tubes

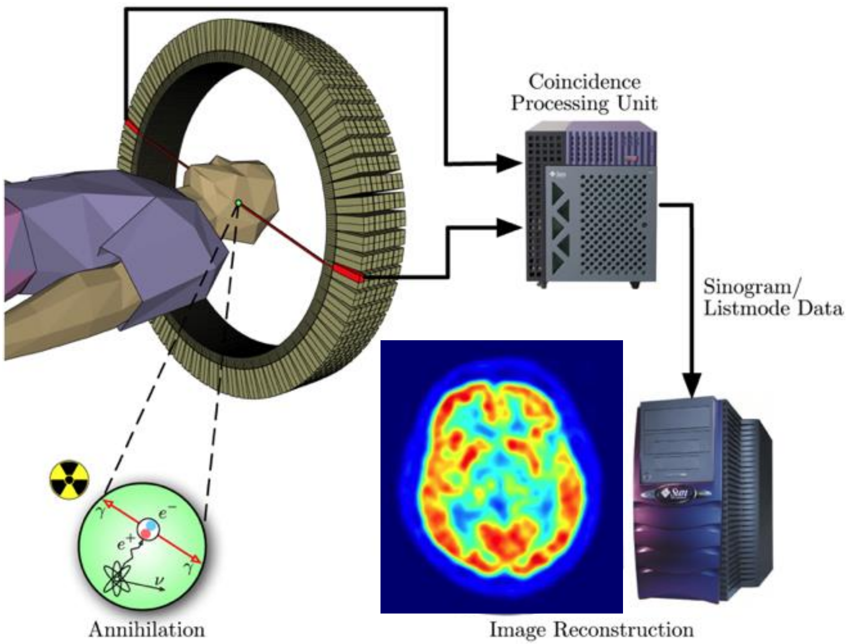


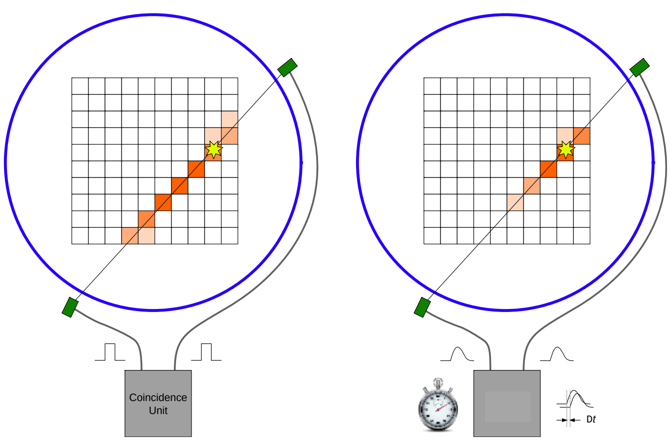
Silicon
Germanium



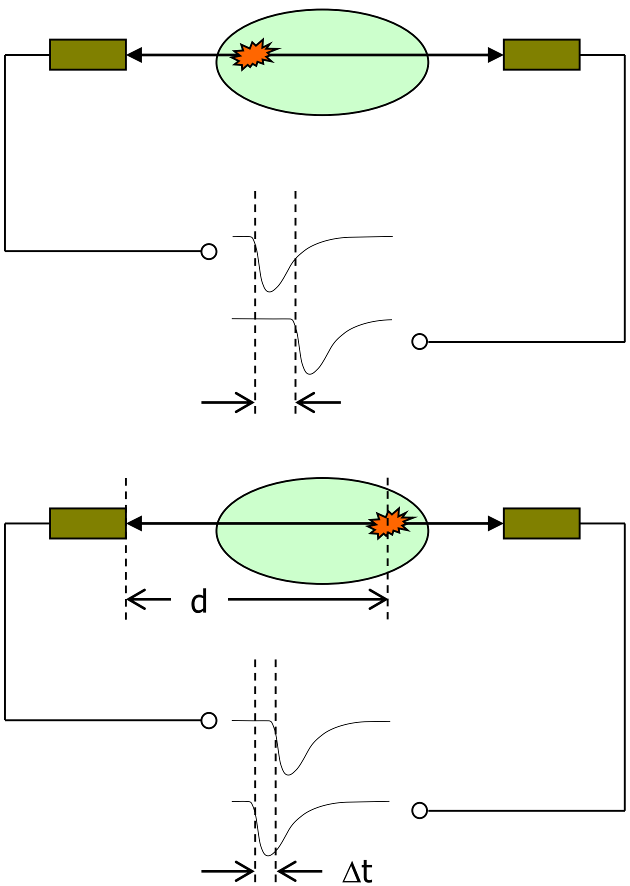
Measure precise timing: ToF-PET

Positron Emission Tomography





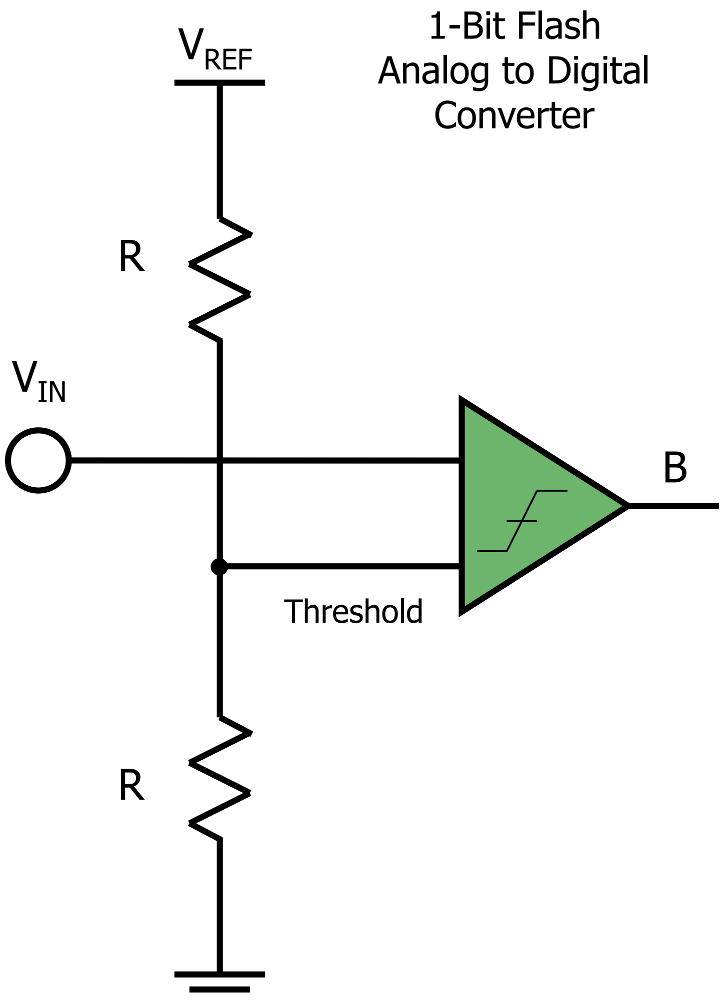
Time-of-Flight PET

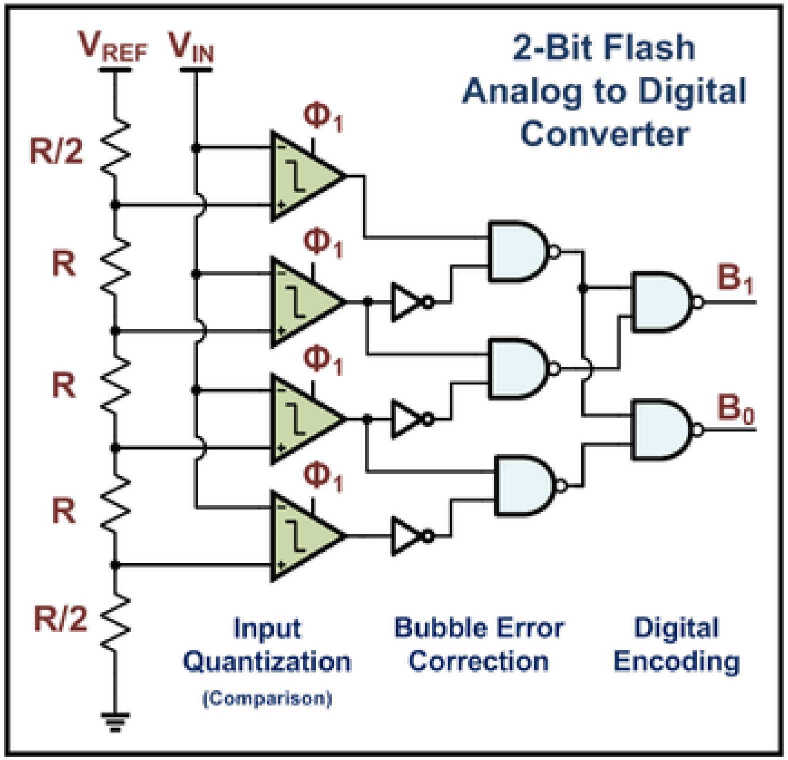


$$d \sim c/2 * \Delta t$$

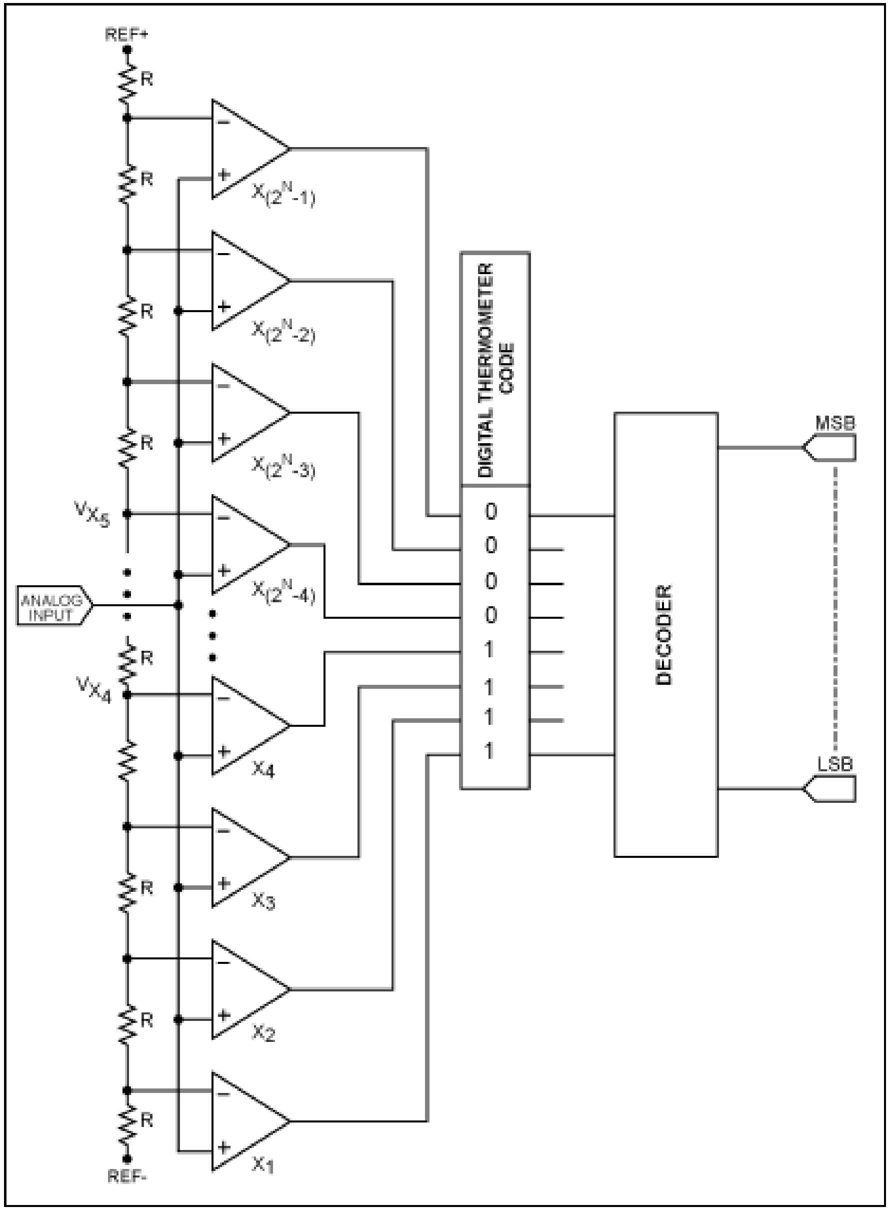
e.g.
d=1 cm → Δt = 67 ps

1-bit & 2-bit ADC



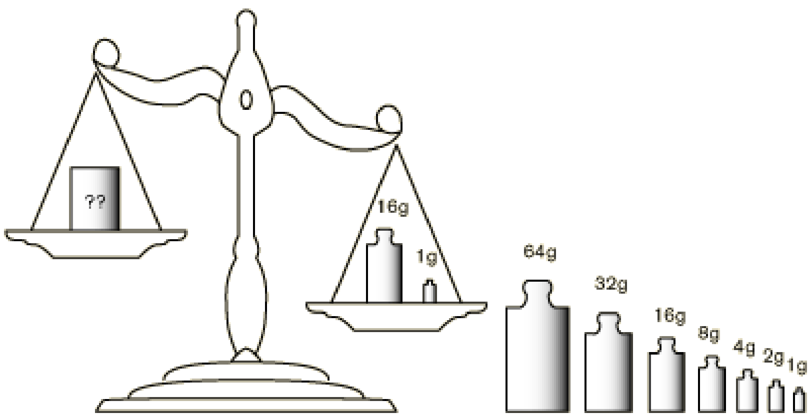


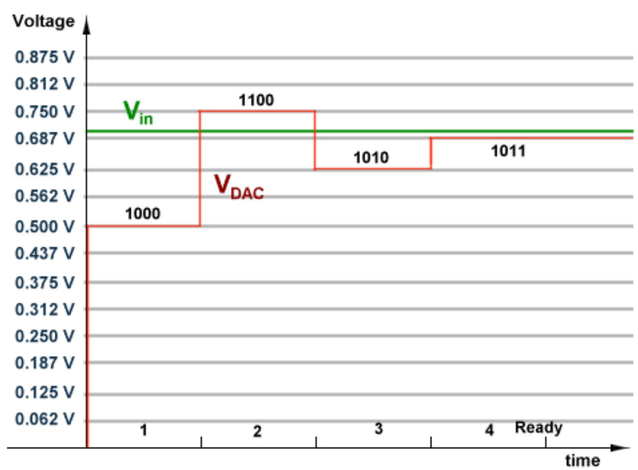
n-bit ADC

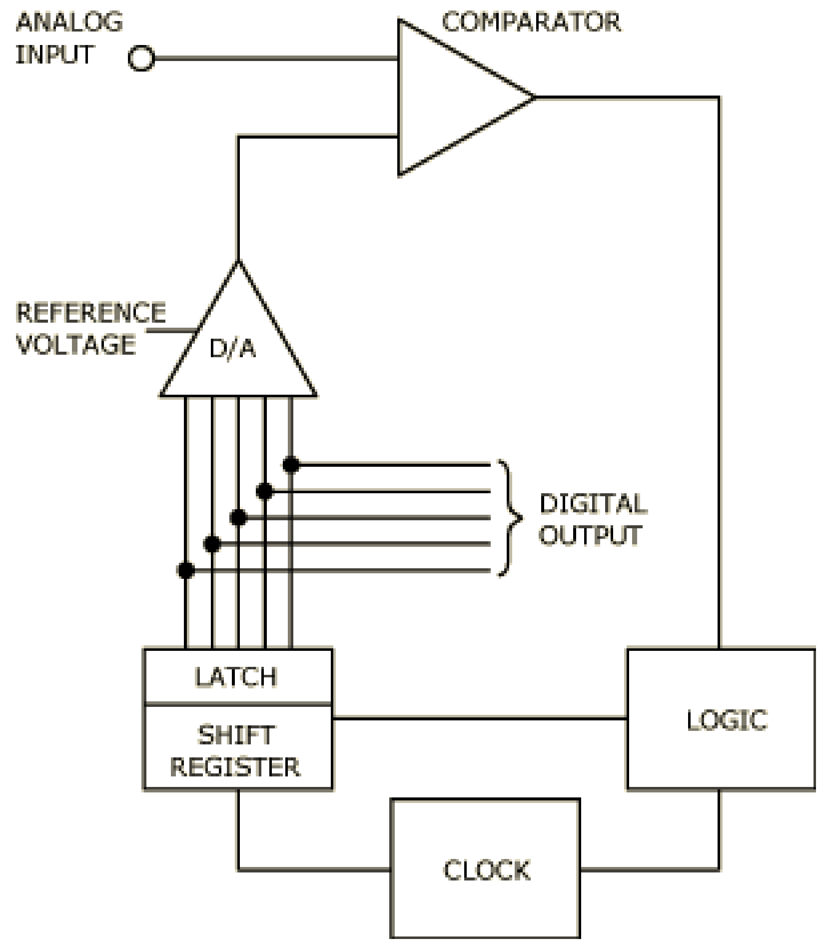


- Flash ADC very fast for small number of bits
- Requires 2^n comparators

Successive approximation ADC

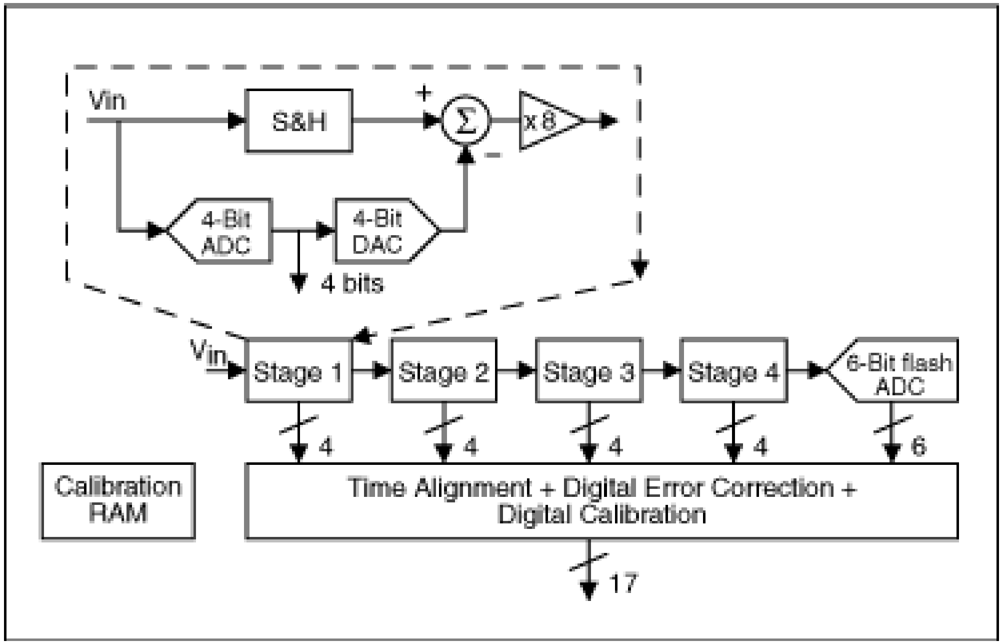


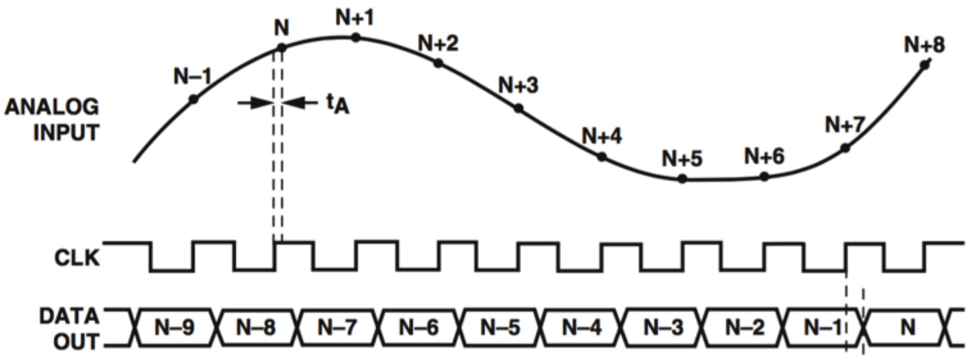




Pipeline ADC

- Combine 4-Bit flash ADC with successive approximation logic
- Only requires 4-Bit flash ADC
- Can convert one sample in each clock cycle
- Has a latency depending on the number of pipeline stages
- Most common technology for fast ADCs (> 10 MHz)

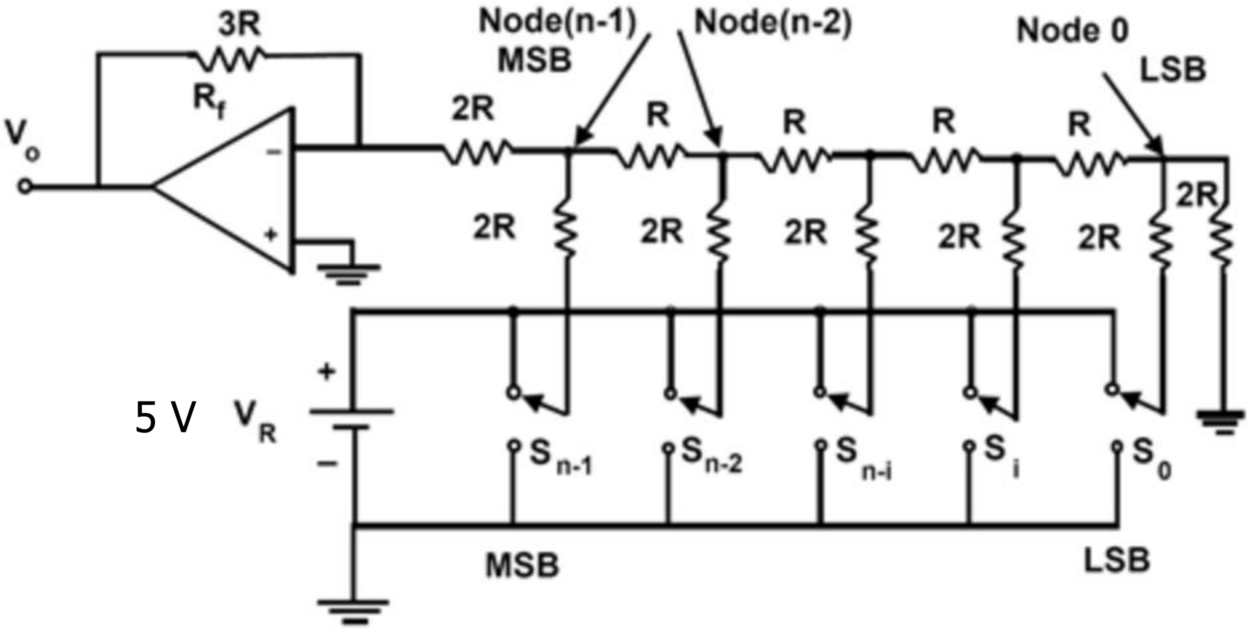




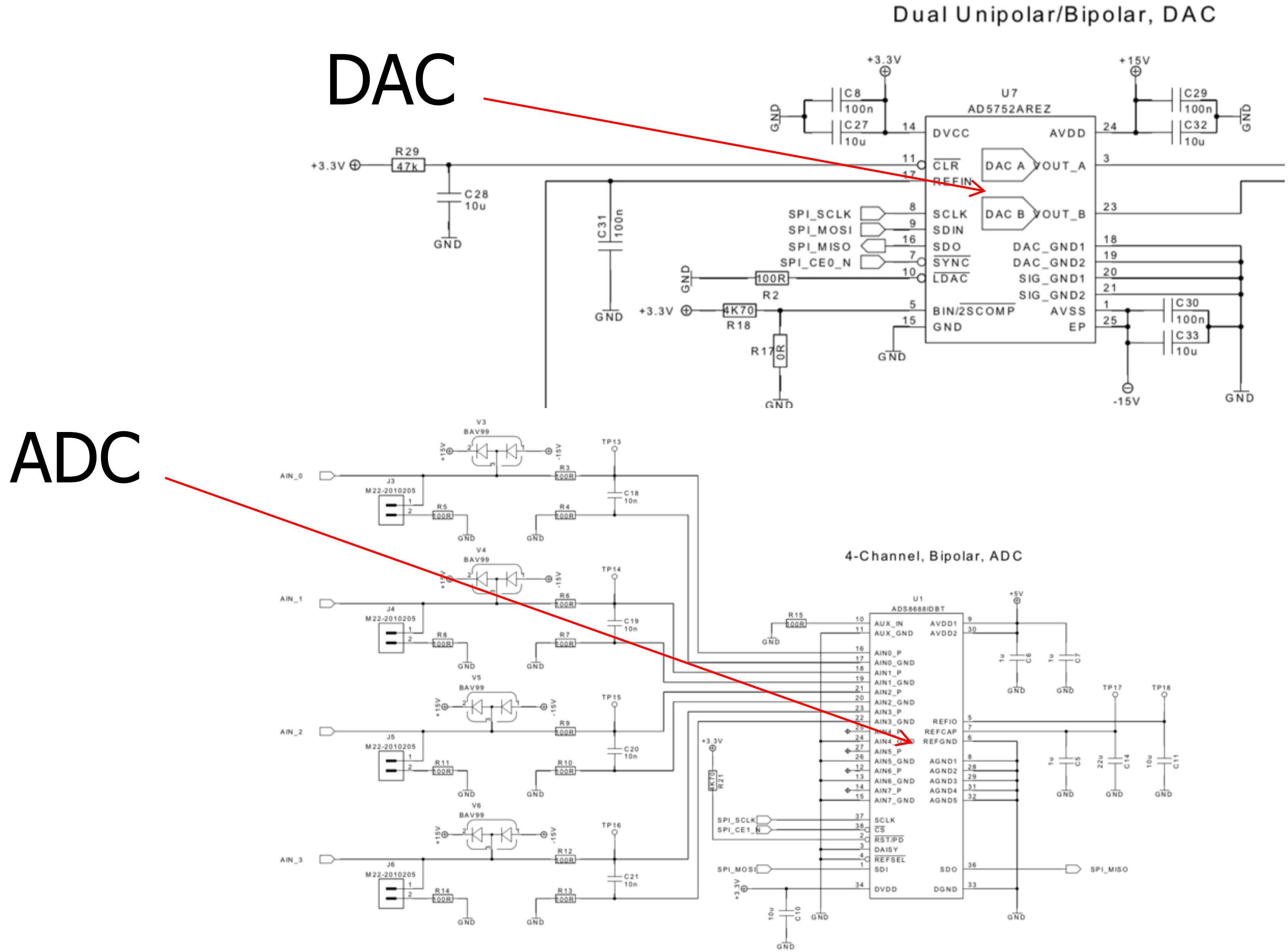
Digital-to-analog converter (DAC)

R-2R Ladder: 0/V_R at $S_0 \ldots S_{n-1}$ give binary weighted output $V_o = S * V_R/32$

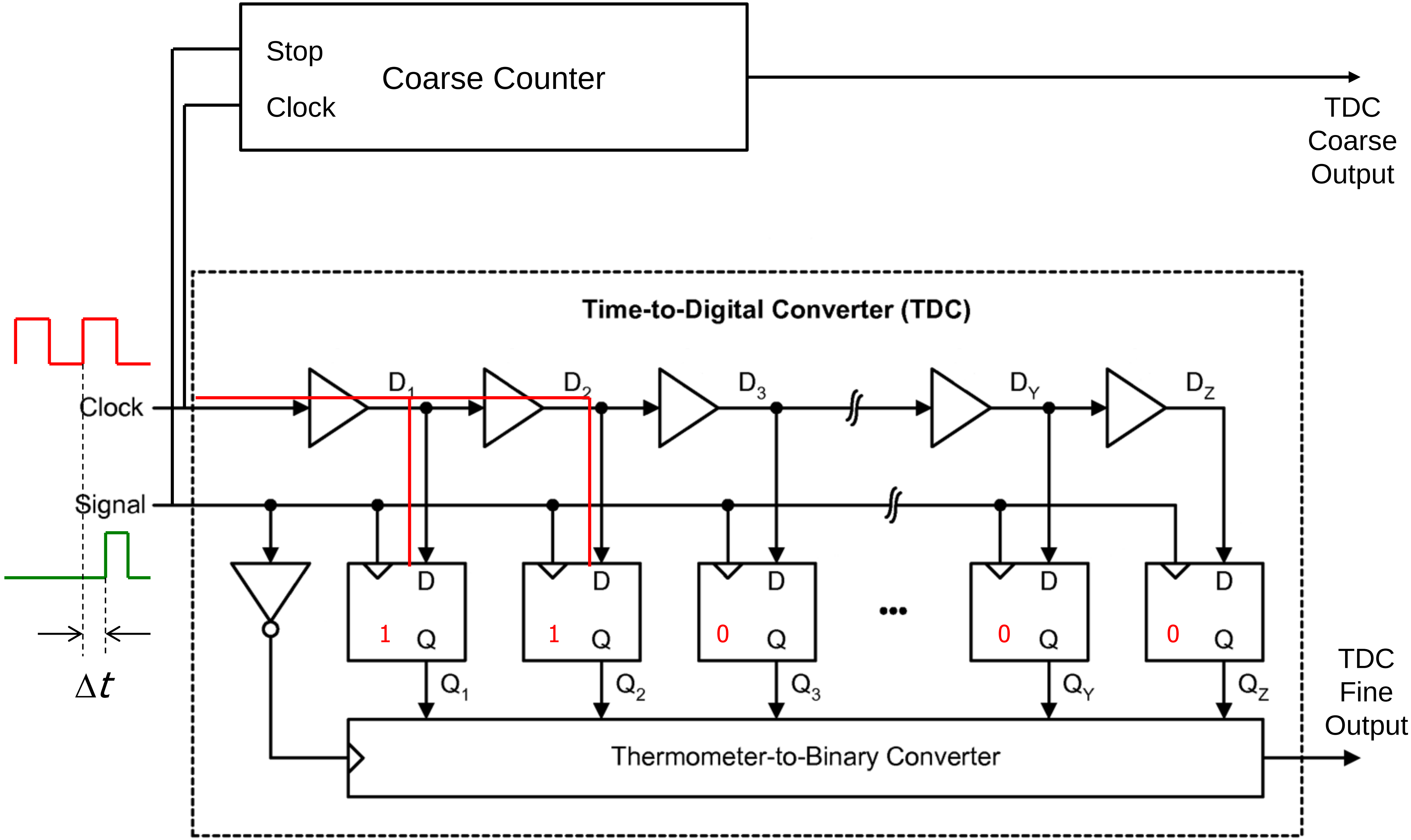
S_{n-1}-S_0	V_O [V]
00000	0
00001	0.16
00010	0.31
00011	0.47
00100	0.63
00101	0.78
...	...
11100	4.38
11101	4.53
11110	4.69
11111	4.84



Raspberry Pi ADC – DAC Board



Time-to-Digital Converter



TDC in FPGA

A 3.9 ps RMS Resolution Time-to-Digital Convertor Using Dual-sampling Method on Kintex UltraScale FPGA

Chong Liu, Yonggang Wang, Peng Kuang, Deng Li, Xinyi Cheng

Real Time 2016 Conference, Padova

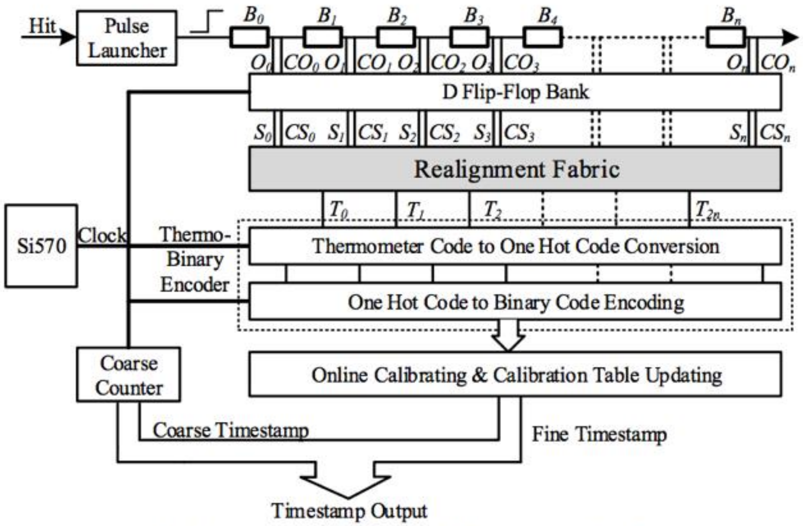
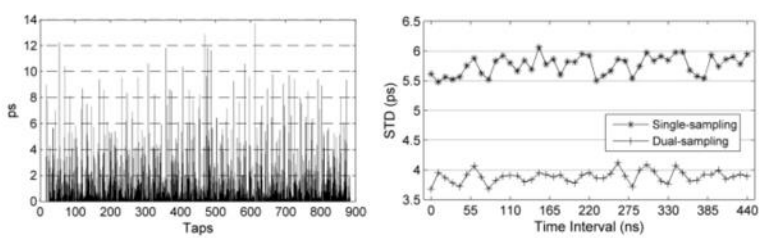
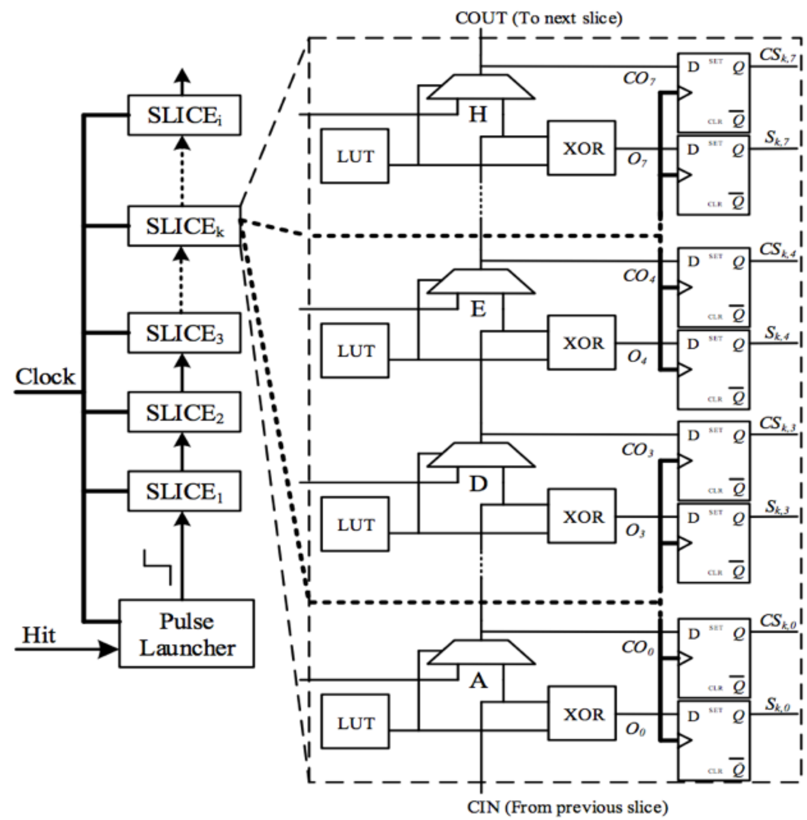


Fig. 1. Diagram of function blocks in a TDL-TDC.



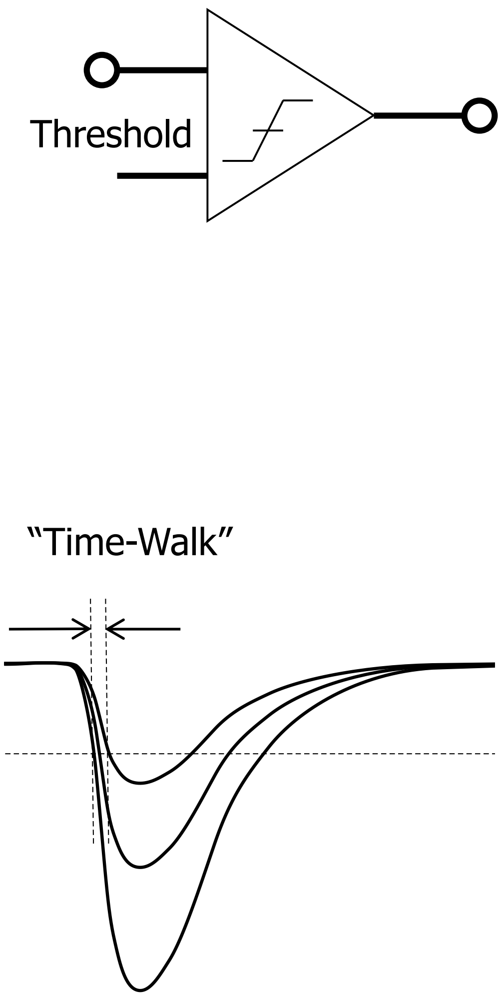
(a) (b)

Fig. 3. (a) Bin width of dual-sampling TDC after bin realignment. (b) RMS resolution of dual-sampling TDC and single-sampling TDC.

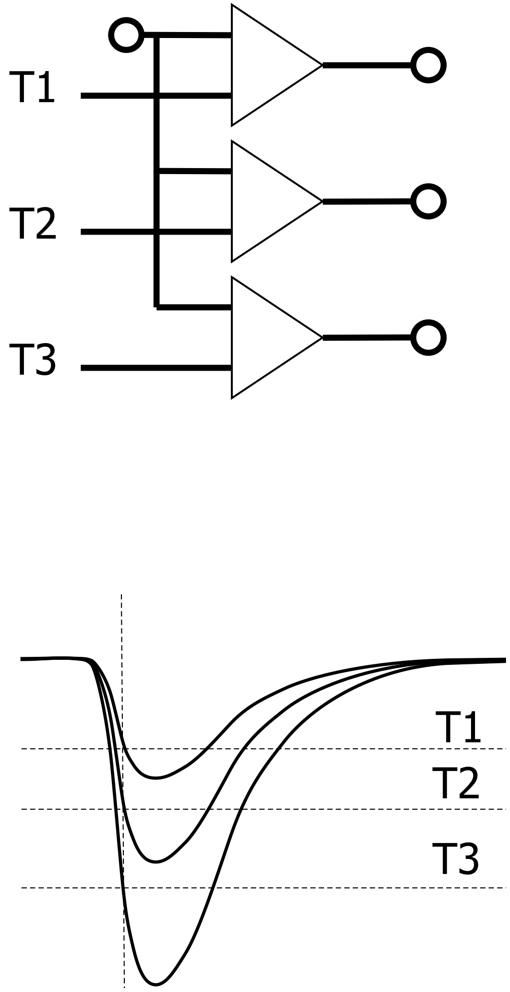


Signal discrimination

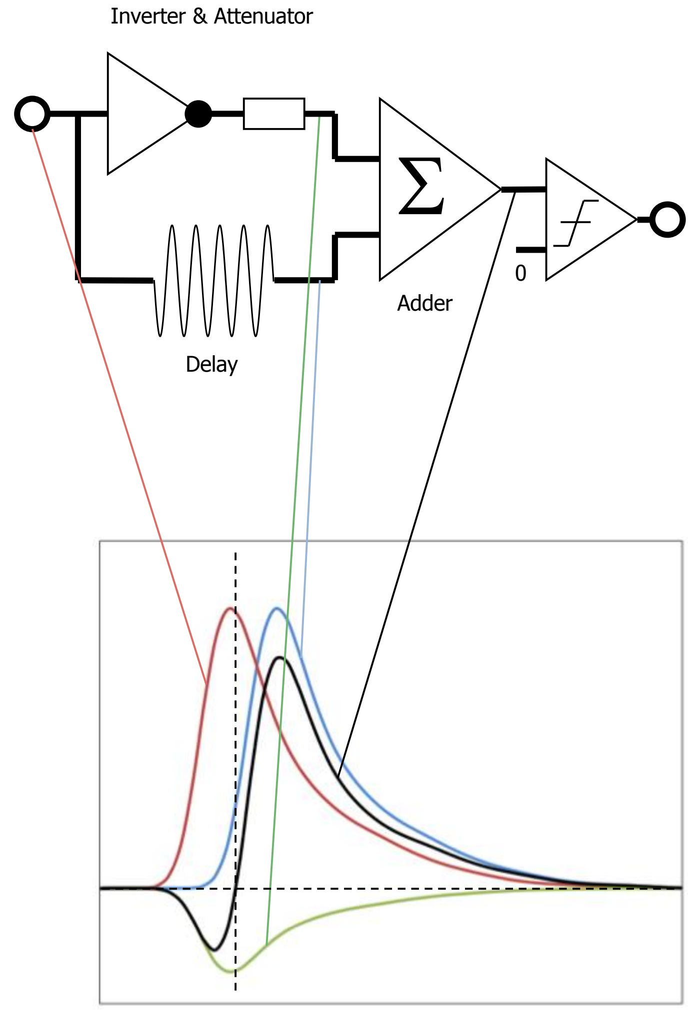
Single Threshold



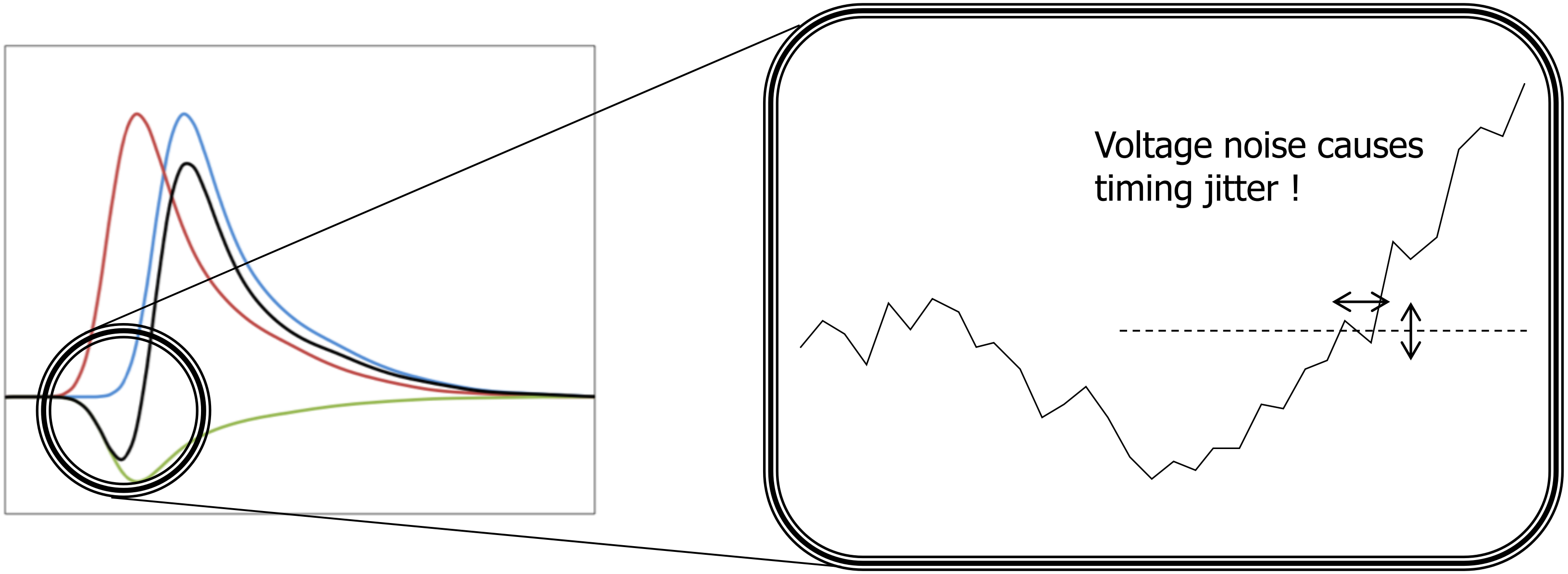
Multiple Thresholds

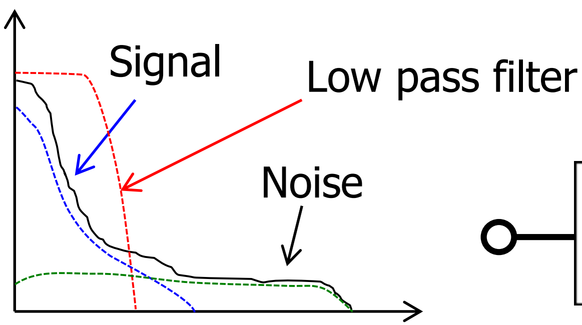


Constant Fraction (CFD)

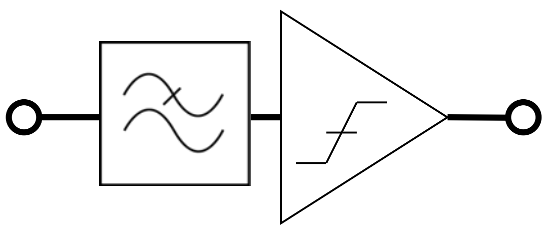


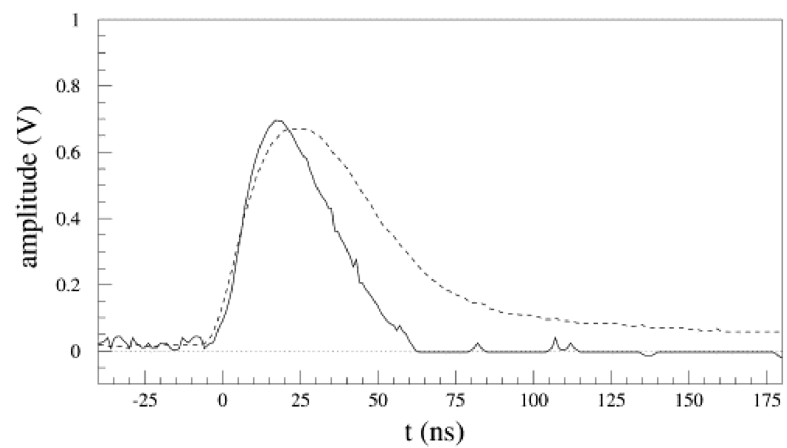
Influence of noise





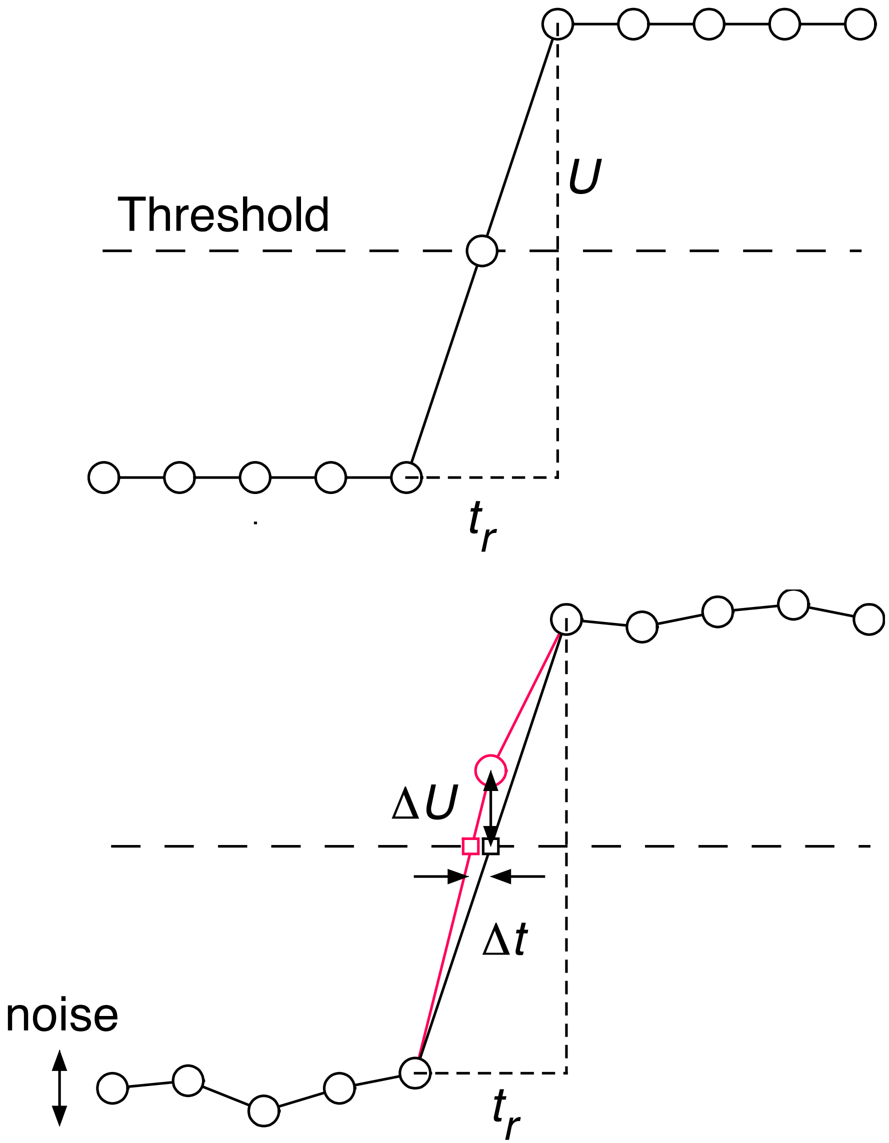
Fourier Spectrum





Low pass filter (shaper) reduces noise while maintaining most of the signal

Noise limited time accuracy



$$\frac{DU}{Dt} \approx \frac{U}{t_r} \longrightarrow Dt = \frac{DU}{U} \cdot t_r$$

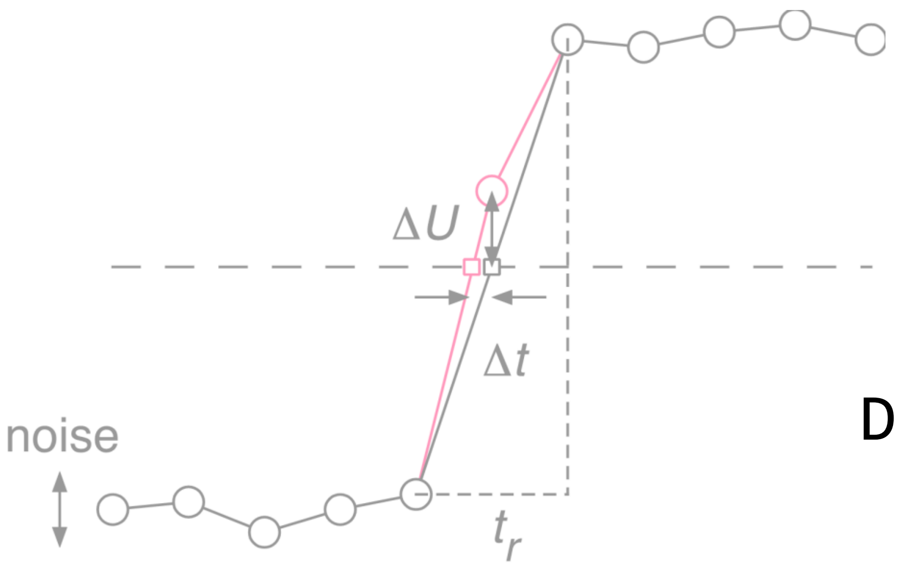
All values in this talk are σ (RMS) !
FHWM = 2.35 x σ

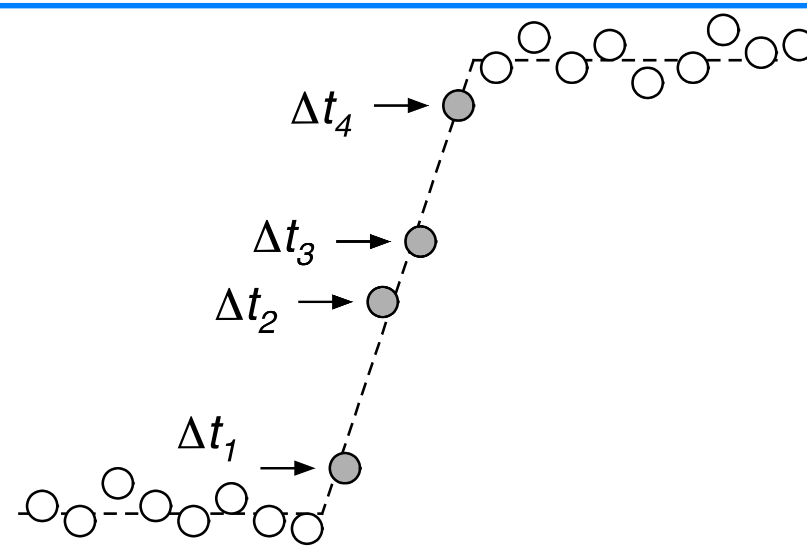
U [mV]	ΔU [mV]	t_r	Δt
100	1	1 ns	10 ps
10	1	3 ns	300 ps

Most today's TDCs have ~20 ps LSB

How can we do better ?

Noise limited time accuracy



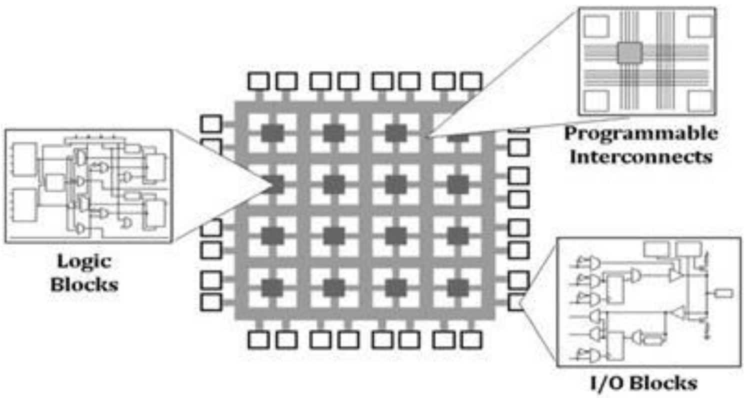


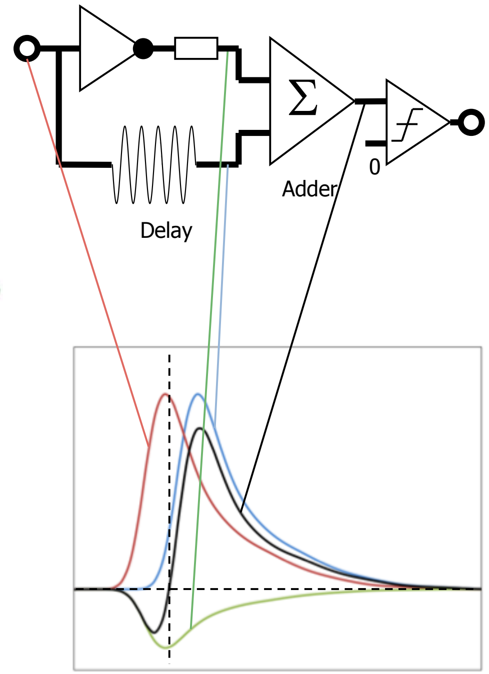
$$\frac{DU}{Dt} \approx \frac{U}{t_r} \longrightarrow Dt = \frac{DU}{U} \cdot t_r$$

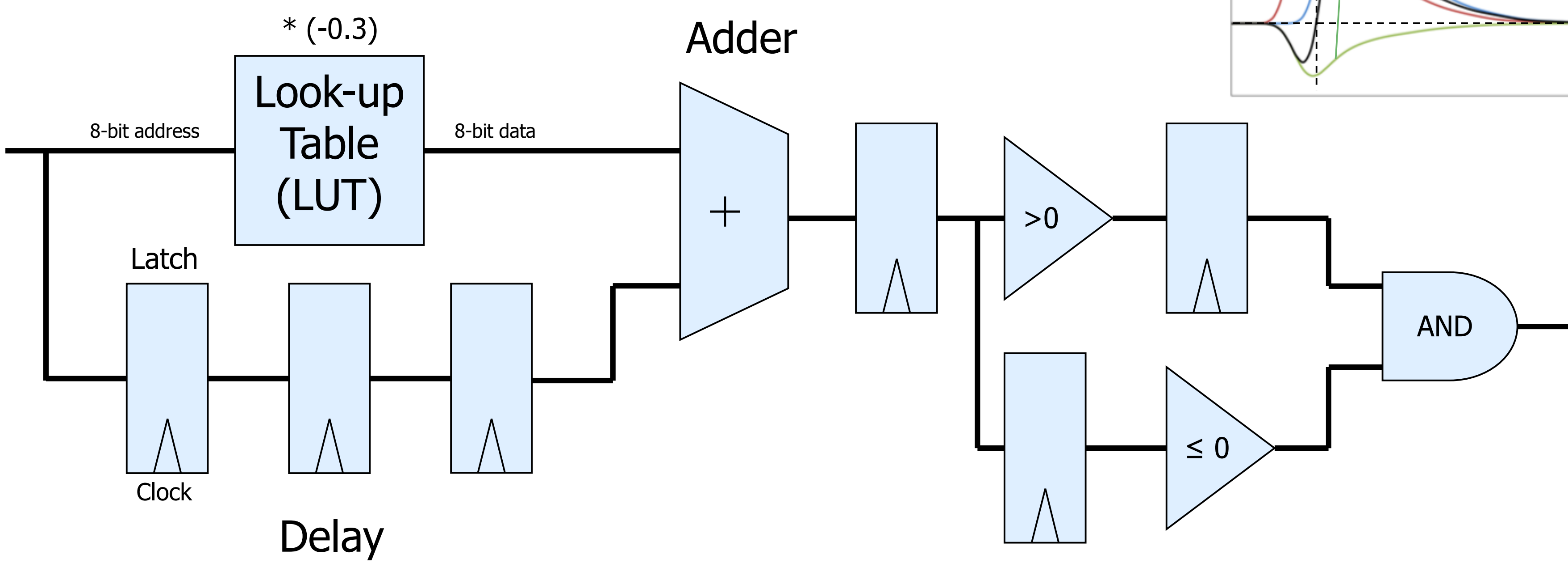
$$Dt = \frac{DU}{U} \cdot t_r \cdot \frac{1}{\sqrt{n}} = \frac{DU}{U} \frac{t_r}{\sqrt{t_r f_S}} = \frac{DU}{U} \cdot \frac{\sqrt{t_r}}{\sqrt{f_S}}$$

Example: CFG in FPGA

FPGA

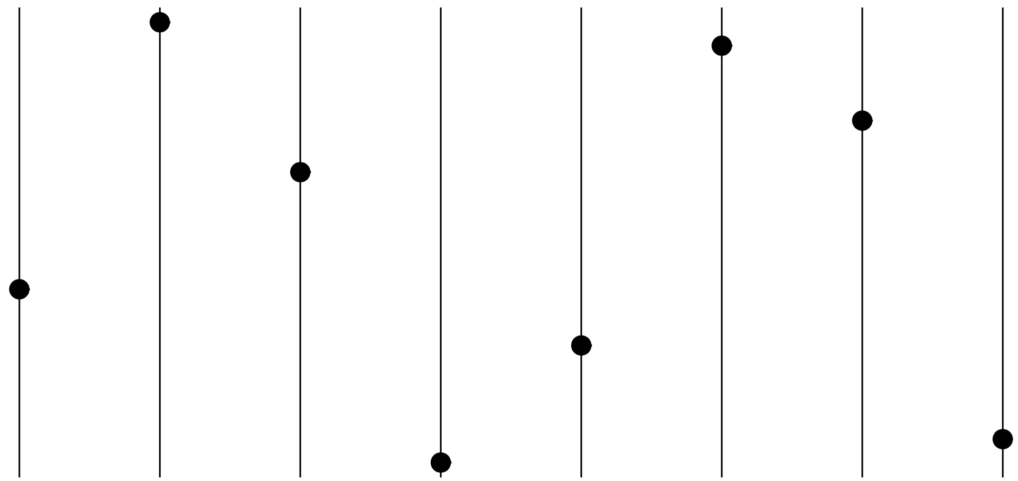




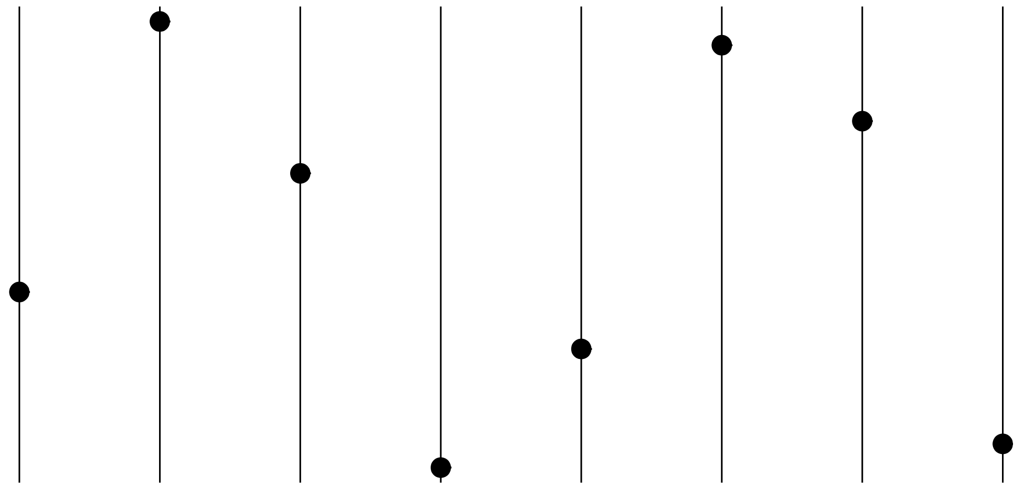


Nyquist-Shannon Sampling Theorem

$f_{signal} < f_{sampling} / 2$

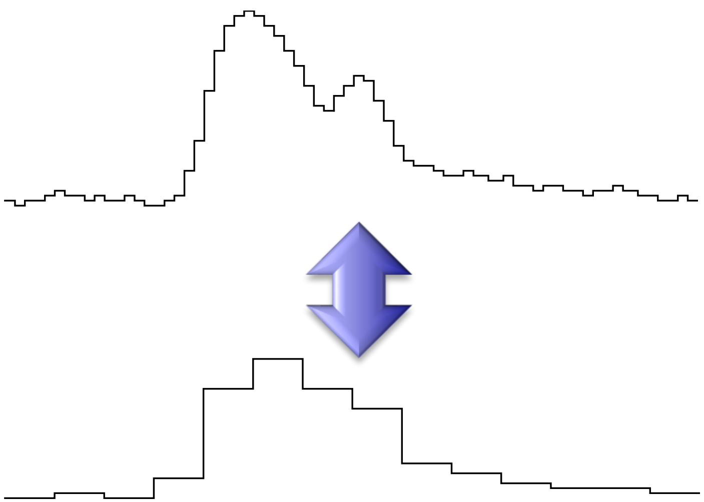


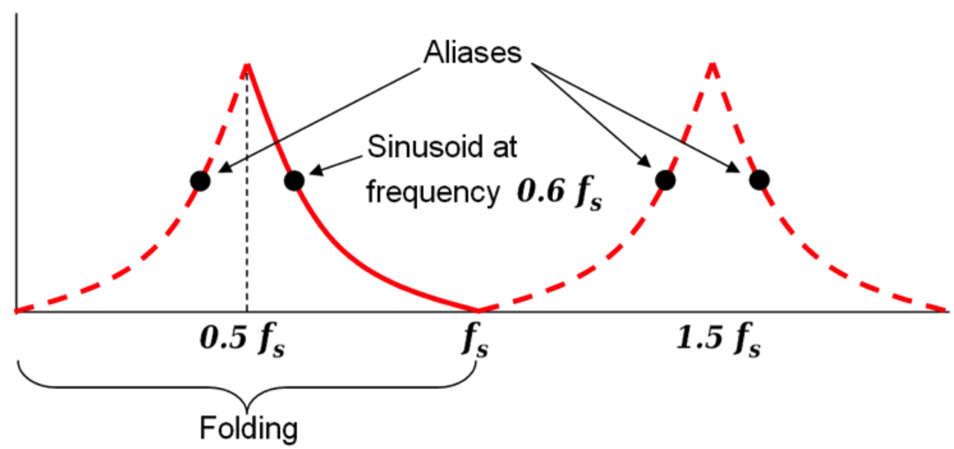
$f_{signal} > f_{sampling} / 2$



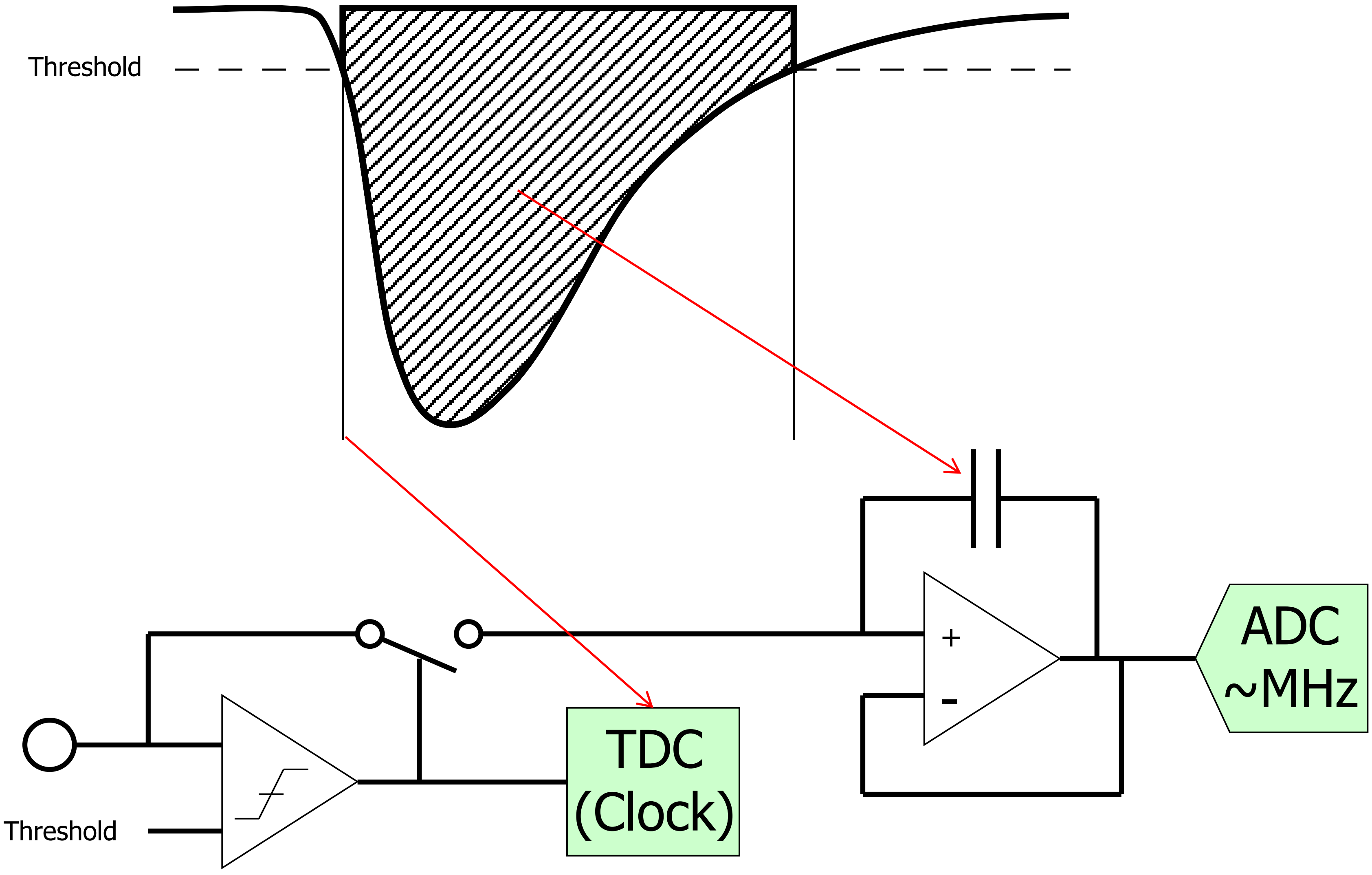
Limits of waveform digitizing

- Aliasing Occurs if $f_{signal} > 0.5 * f_{sampling}$
- Features of the signal can be lost ("pile-up")
- Measurement of time becomes hard
- ADC resolution limits energy measurement
- Need very fast high resolution ADC

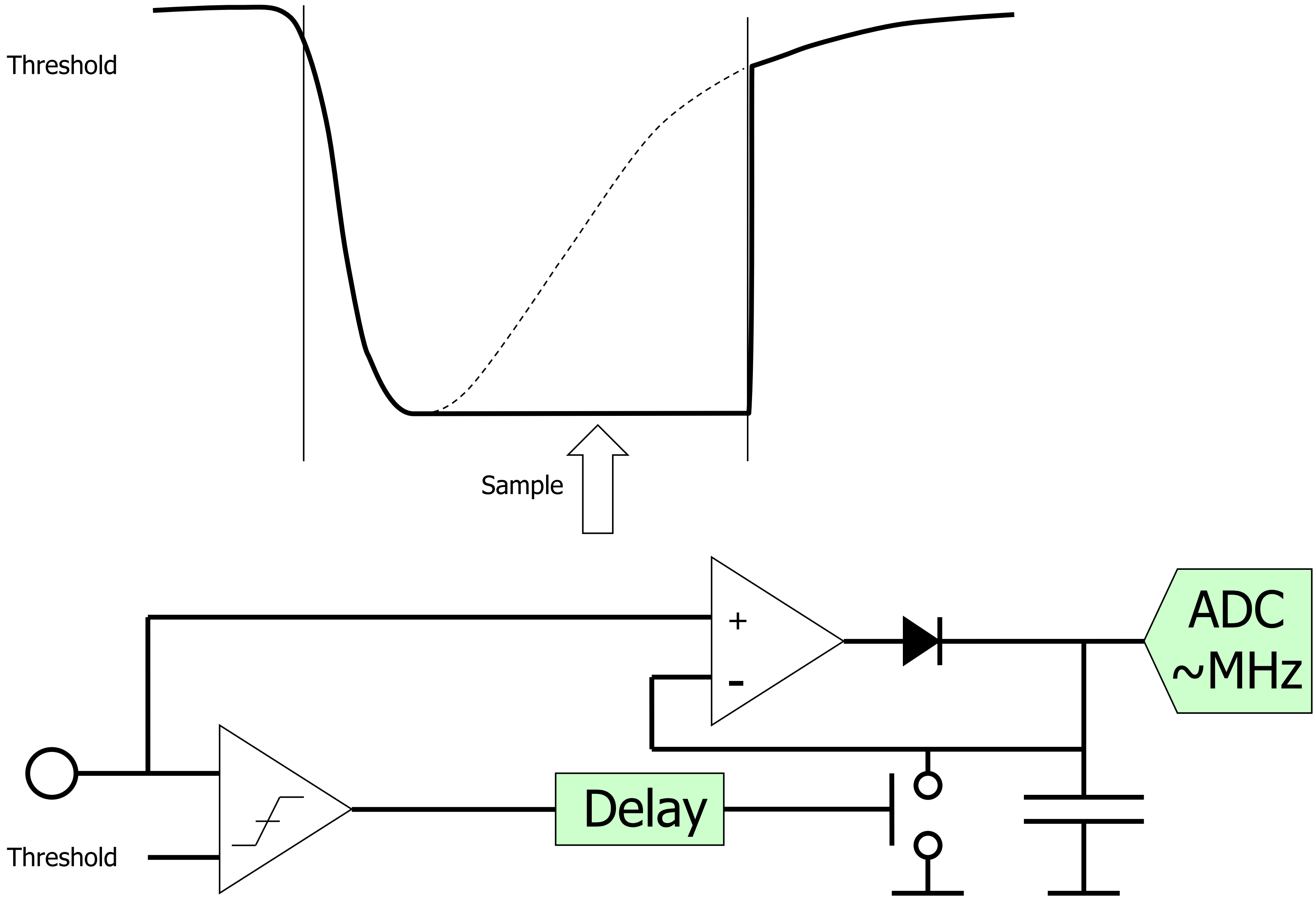




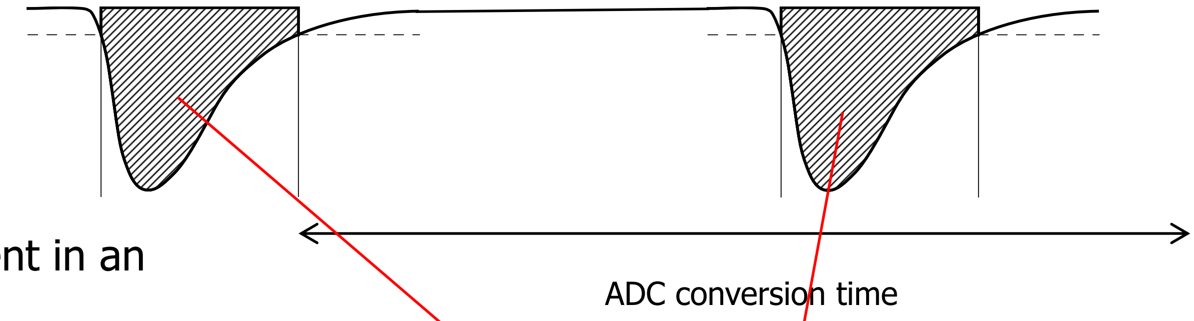
Charge ADCs (QADC)



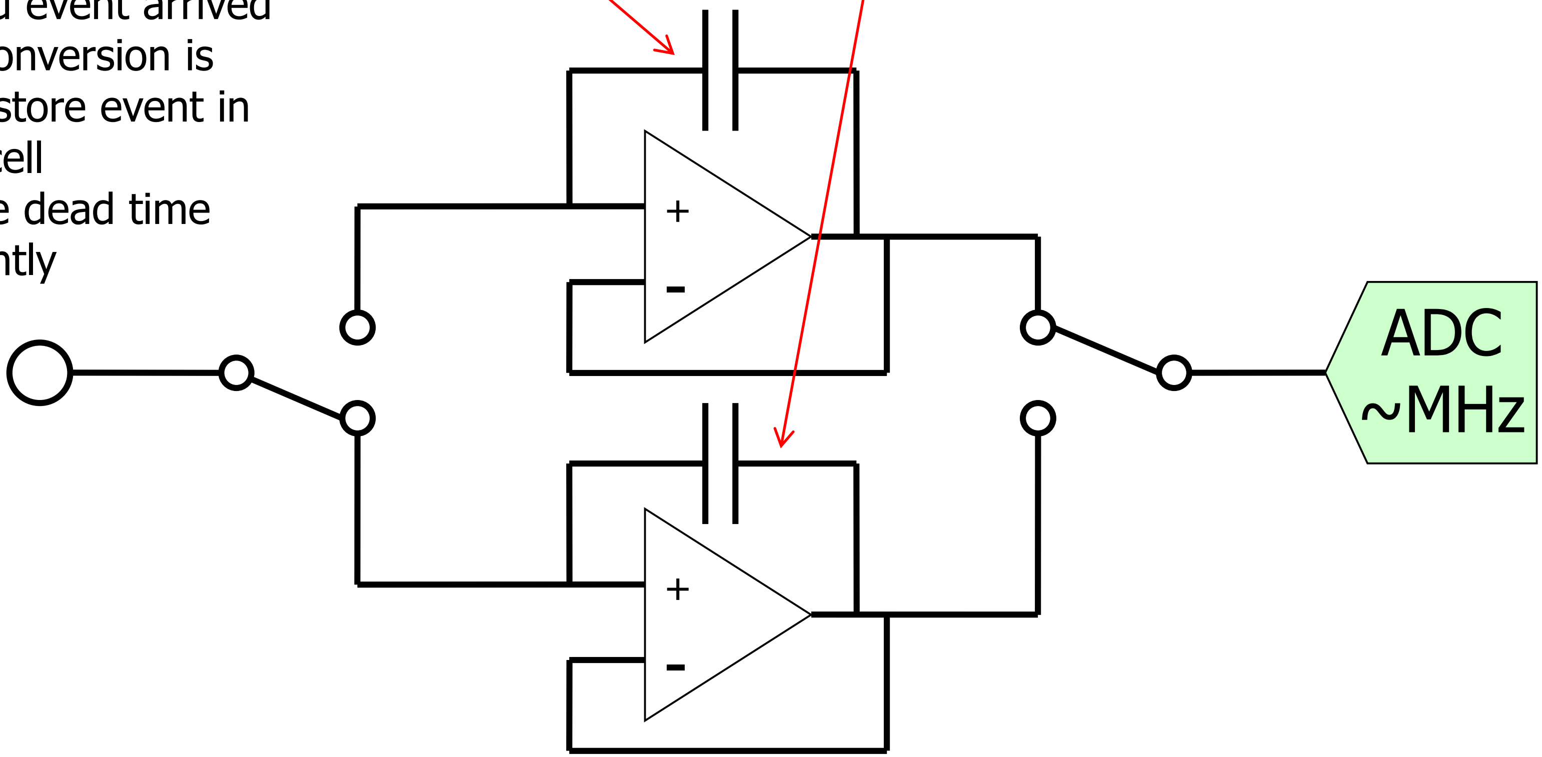
Peak sensing ADC



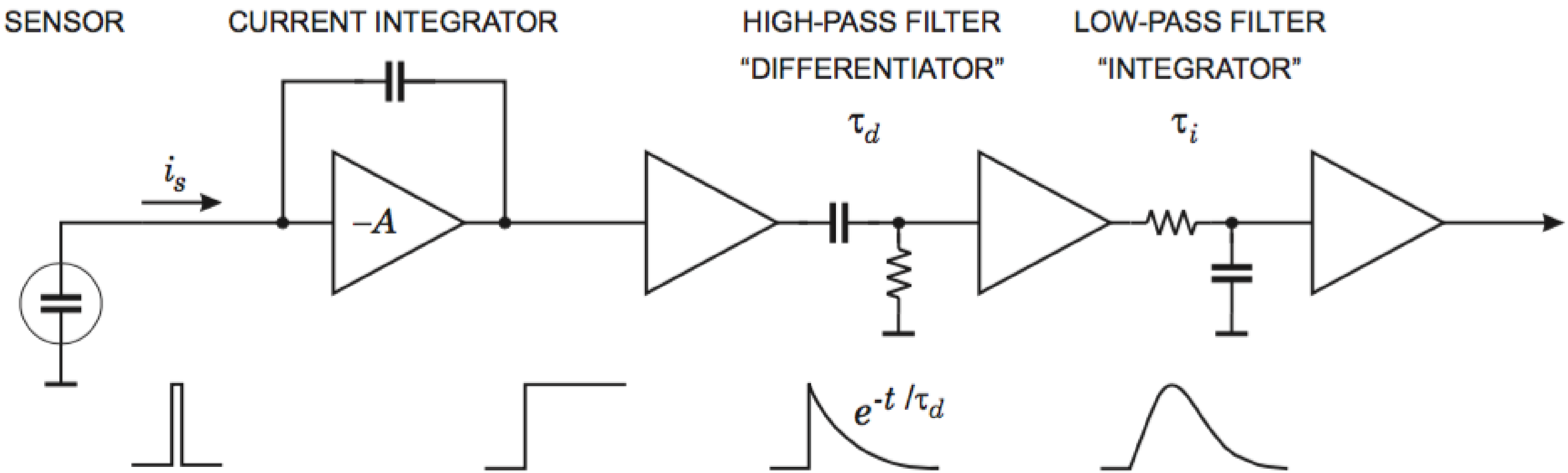
Double buffering



- Store an event in an analog cell
- Start converting cell
- If second event arrived before conversion is ready – store event in second cell
- Decrease dead time significantly

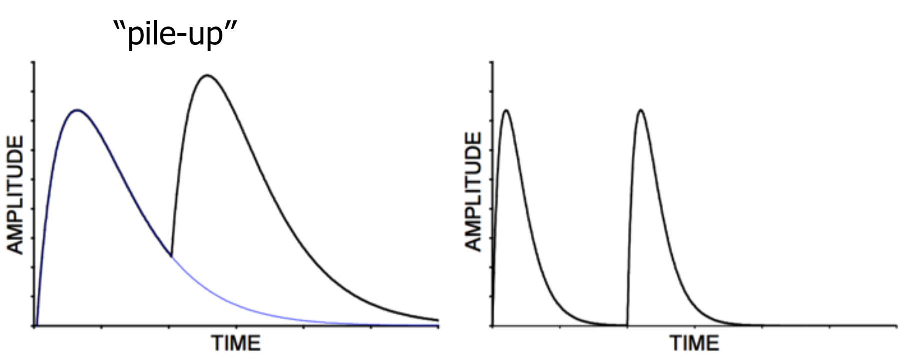


Analog readout chain

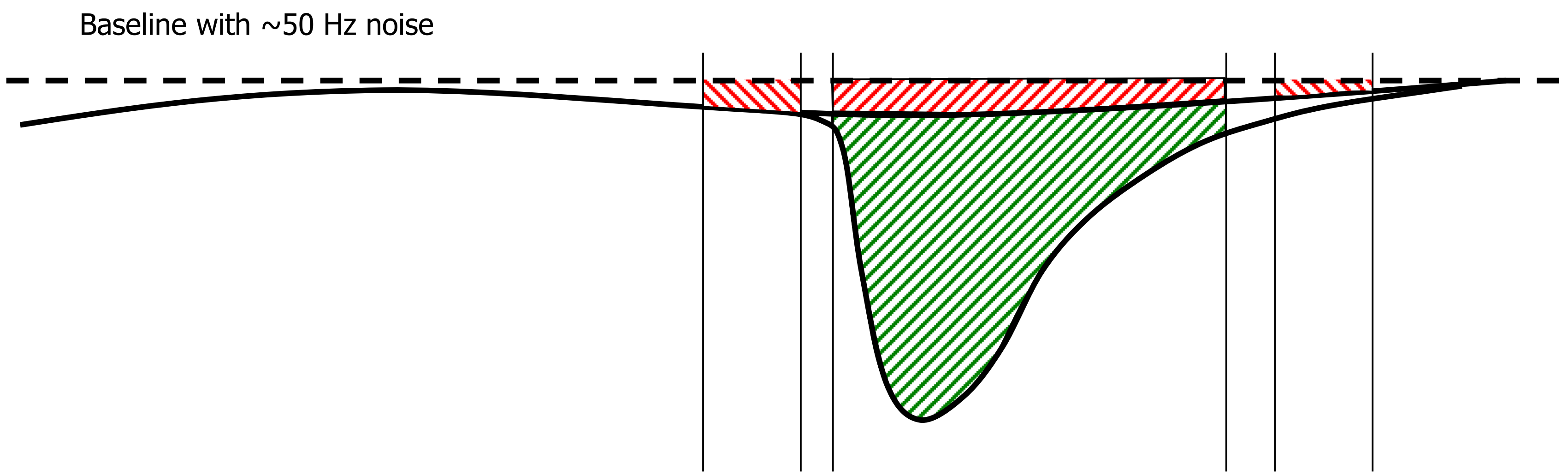


Optimal parameters can greatly improve the signal-to-noise ratio

Effect of slow shaping time:

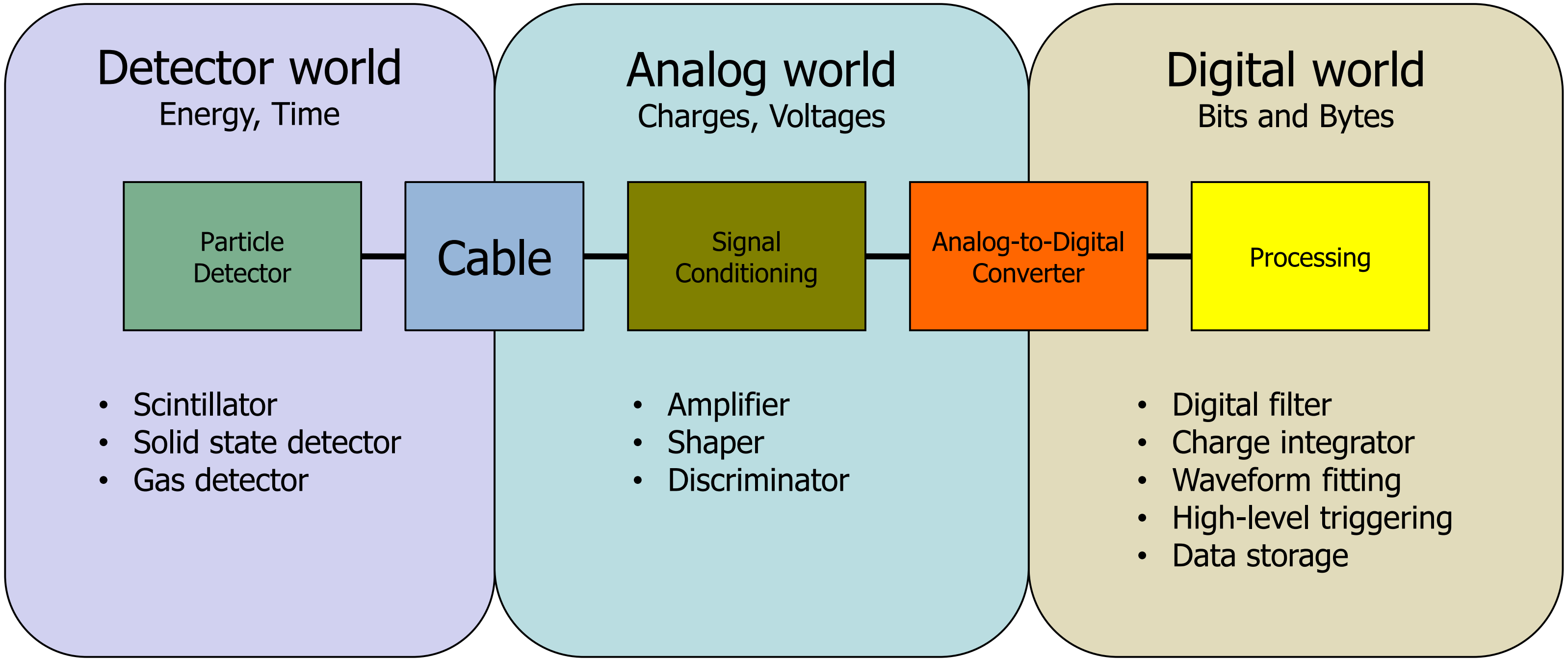


Baseline noise



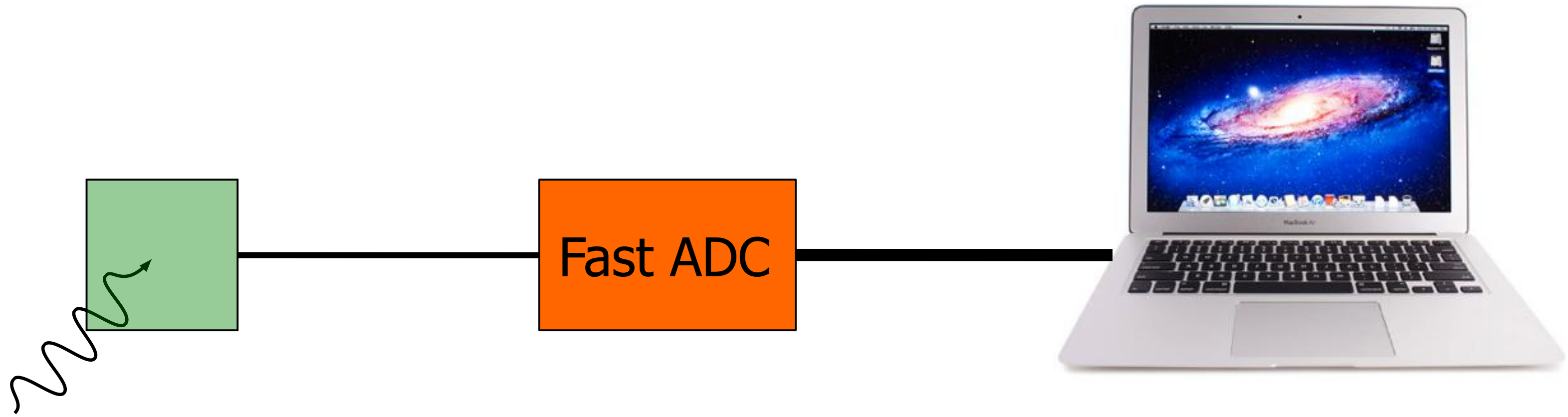
- Charge integration error due to signal “sitting” on fluctuating baseline (e.g. 50 Hz ground loop or artifact of shaper)
- Can be fixed by sampling baseline prior to signal (requires signal delay)
- Sample signal after peak for pile-up recognition

Conventional DAQ chain



Let's go a bit faster…

Ultimate sampling

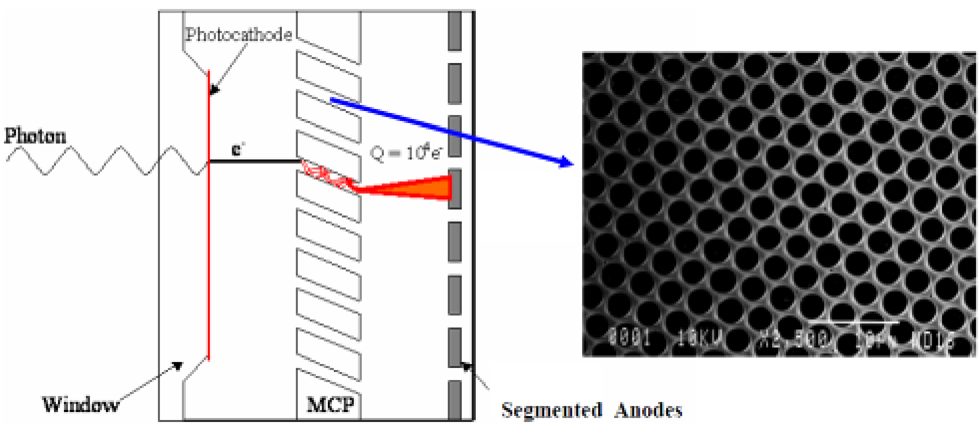


Direct fast sampling without shaping

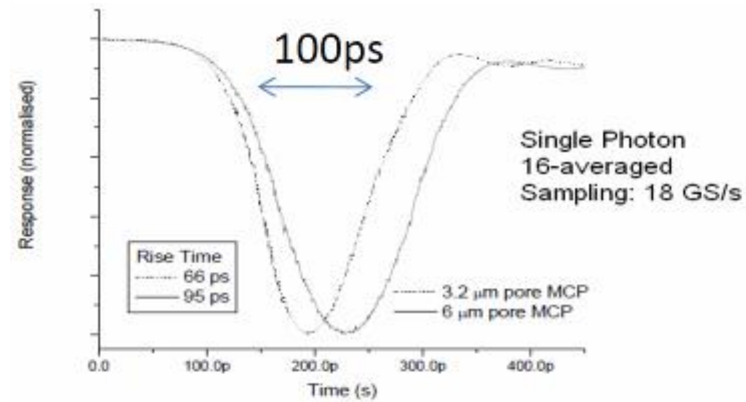
- No shaping artifacts
- Less electronics
- All information if captured if
  $f_{sampling} > 2 * f_{signal}$ and LSB < V_{noise}
- Any shaping circuitry can only *remove* information

What are the fastest detectors?

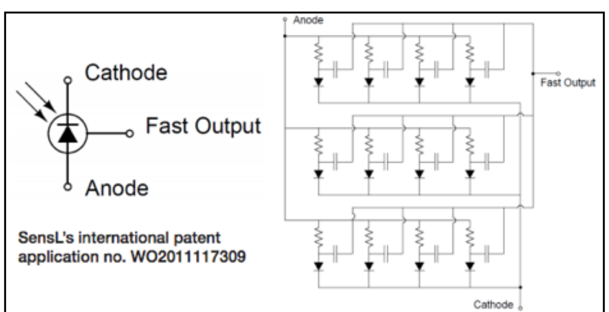
- Micro-Channel-Plates (MCP)
  - Photomultipliers with thousands of tiny channels (3-10 μm)
  - Typical gain of 10,000 per plate
  - Very fast rise time down to 70 ps
- 70 ps rise time → **4-5 GHz BW** → **10 GSPS**
- SiPMs (Silicon PMTs) are also getting < 100 ps

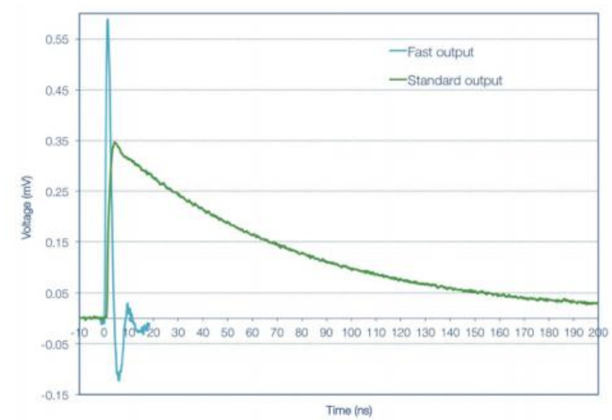


J. Vallerga



J. Milnes, J. Howoth, Photek

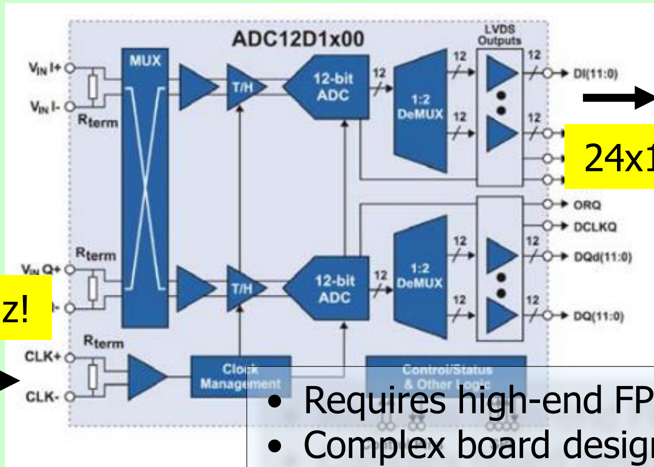




http://sensl.com

Can it be done with FADCs?

- 8 bits – 3 GS/s – 1.9 W → 24 Gbits/s
- 10 bits – 3 GS/s – 3.6 W → 30 Gbits/s
- 12 bits – 3.6 GS/s – 3.9 W → 43.2 Gbits/s
- 14 bits – 0.4 GS/s – 2.5 W → 5.6 Gbits/s



24x1.8 Gbits/s

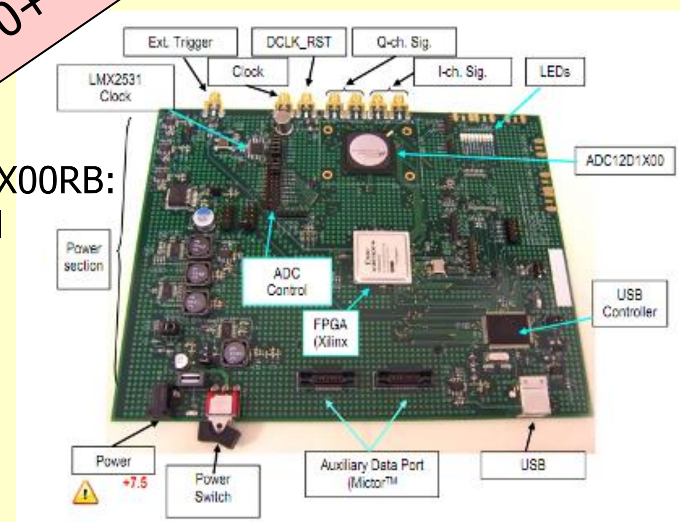
1.8 GHz!

- Requires high-end FPGA
- Complex board design
- High FPGA power

PX1500-4:
2 Channel
3 GS/s
8 bits

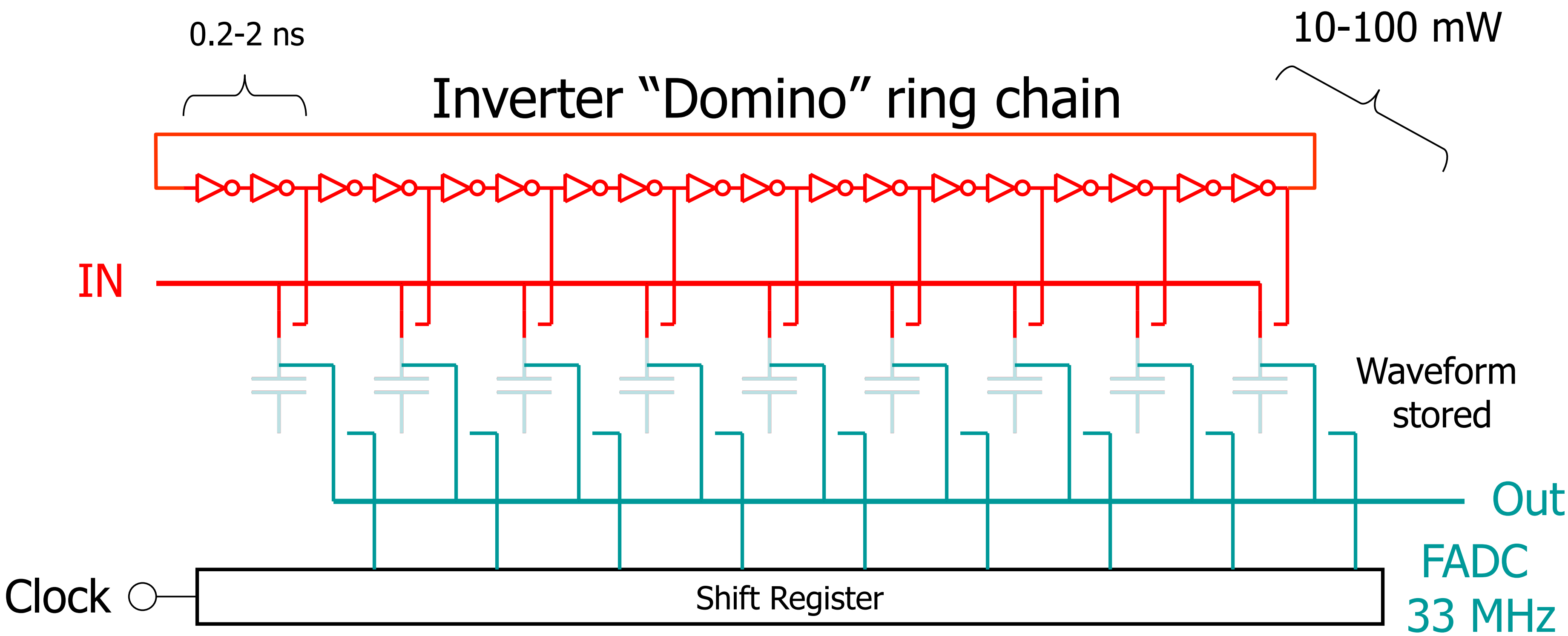
1-10 k$ / channel
What about 1000+ Channels?

ADC12D1X00RB:
1 Channel
1.8 GS/s
12 bits



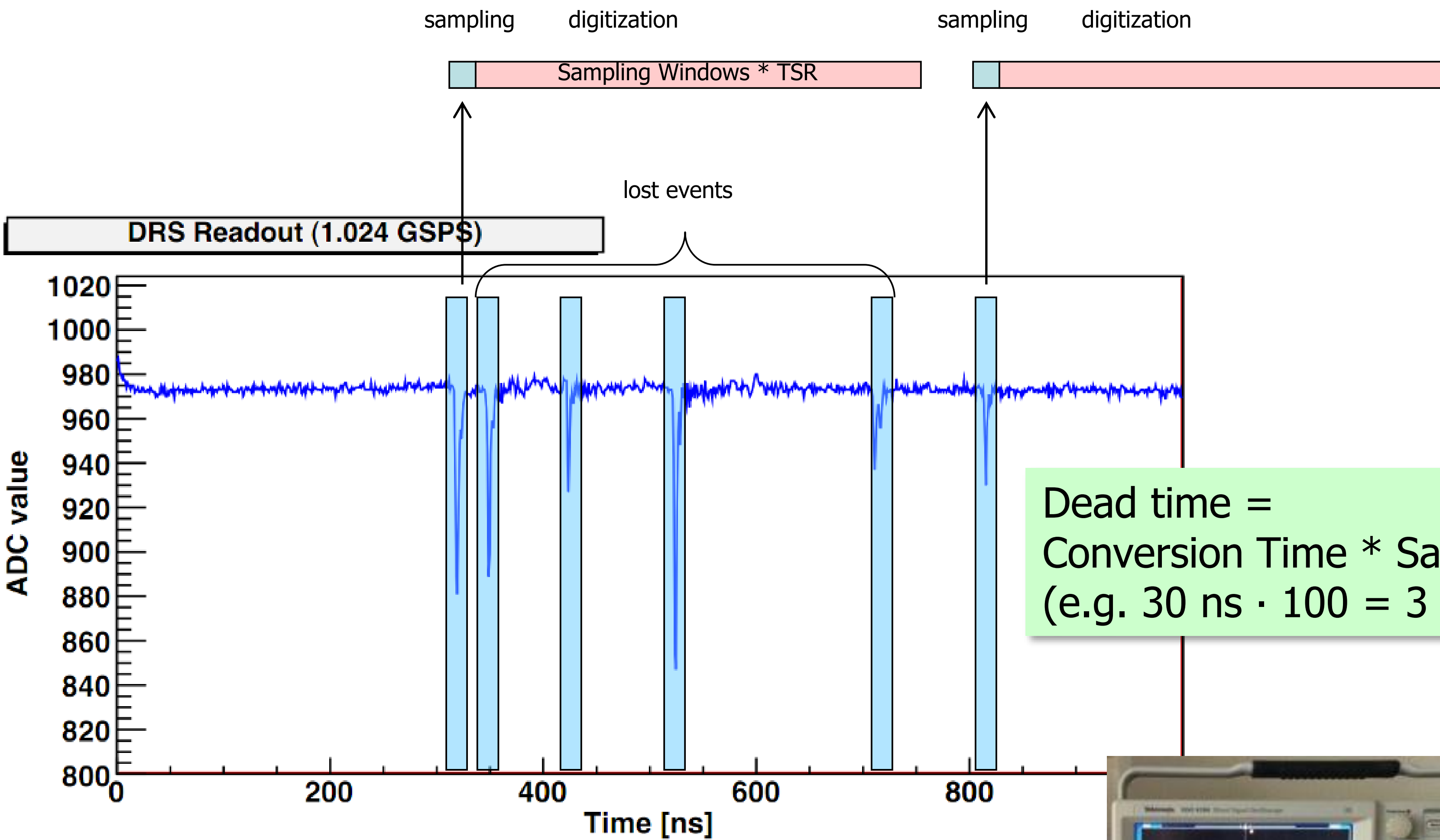
V1761: 2 Channels, 4 GS/s, 10 bits

Switched Capacitor Array (Analog Memory)



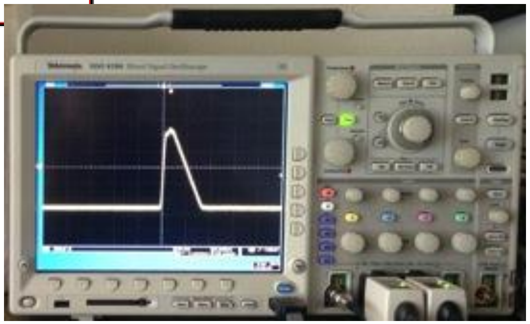
"Time stretcher" GHz → MHz

Triggered Operation



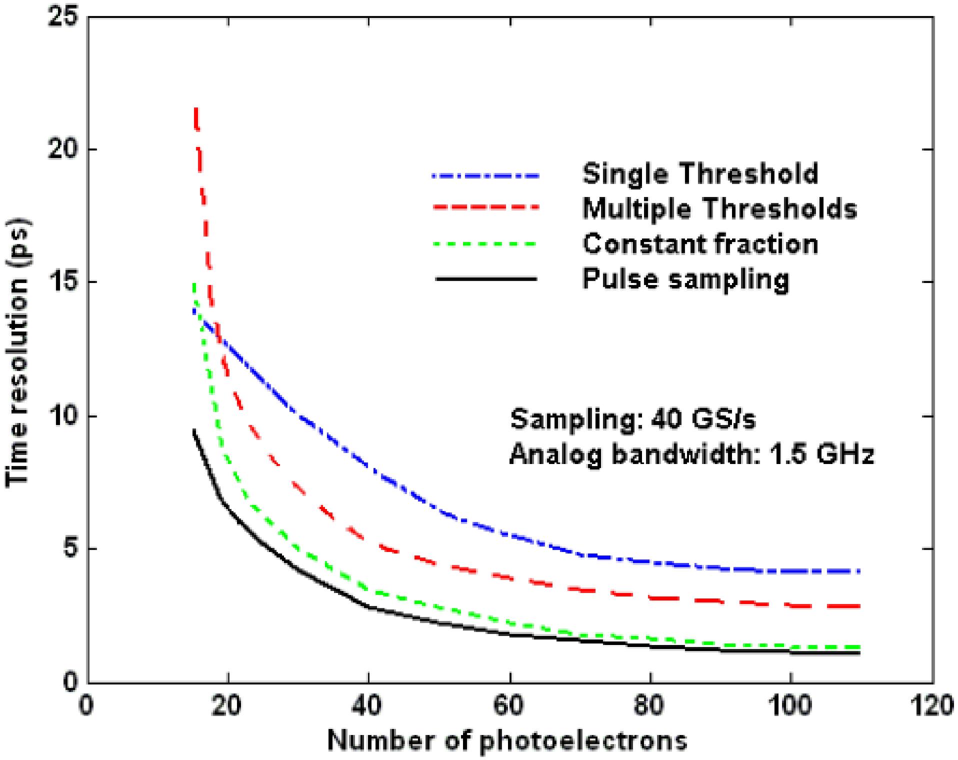
Dead time =
Conversion Time * Samples
(e.g. 30 ns · 100 = 3 μs)

Chips usually cannot sample during readout ⇒ "Dead Time"
Technique only works for "events" and "triggers"



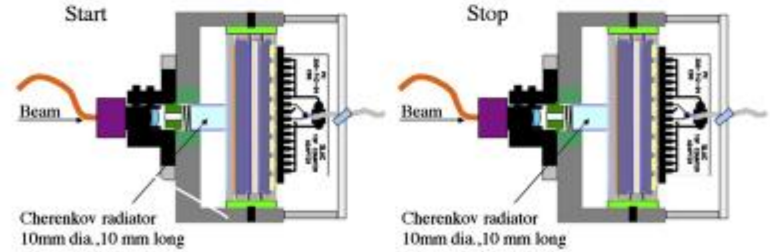
How to measure best timing?

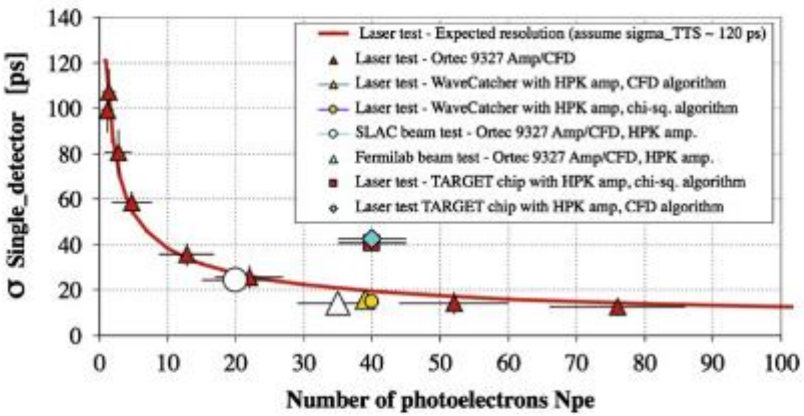
Simulation of MCP with realistic noise and different discriminators



J.-F. Genat et al., arXiv:0810.5590 (2008)

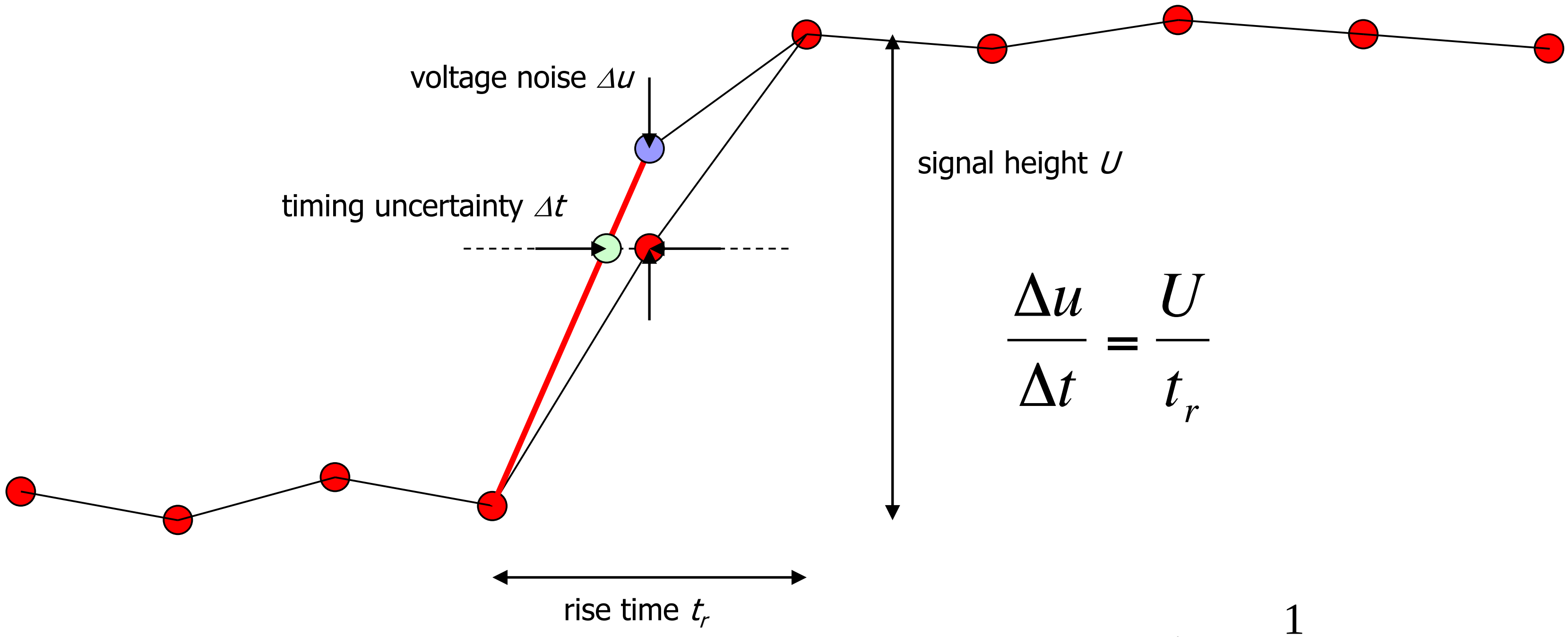
Beam measurement at SLAC & Fermilab





D. Breton et al., NIM **A629**, 123 (2011)

How is timing resolution affected?



$$\frac{\Delta u}{\Delta t} = \frac{U}{t_r}$$

$$t_r \approx \frac{1}{3 f_{3dB}}$$

$$\Delta t = \frac{\Delta u}{U} \cdot t_r = \frac{\Delta u}{U\sqrt{n}} \cdot t_r = \frac{\Delta u}{U} \cdot \frac{t_r}{\sqrt{t_r \cdot f_s}} = \frac{\Delta u}{U} \cdot \frac{\sqrt{t_r}}{\sqrt{f_s}} = \frac{\Delta u}{U} \cdot \frac{1}{\sqrt{3 f_s \cdot f_{3dB}}}$$

number of samples on slope

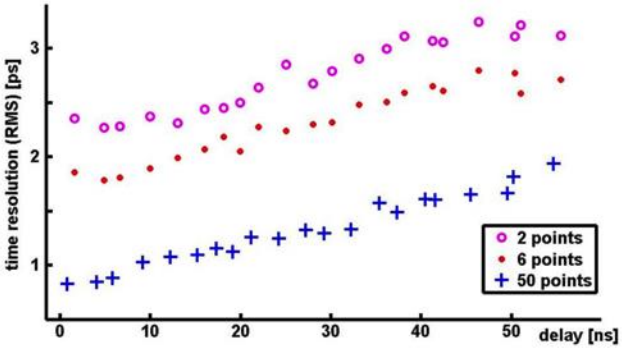
Simplified estimation!

How is timing resolution affected?

$$\Delta t = \frac{\Delta u}{U} \cdot \frac{1}{\sqrt{3 f_s \cdot f_{3dB}}}$$

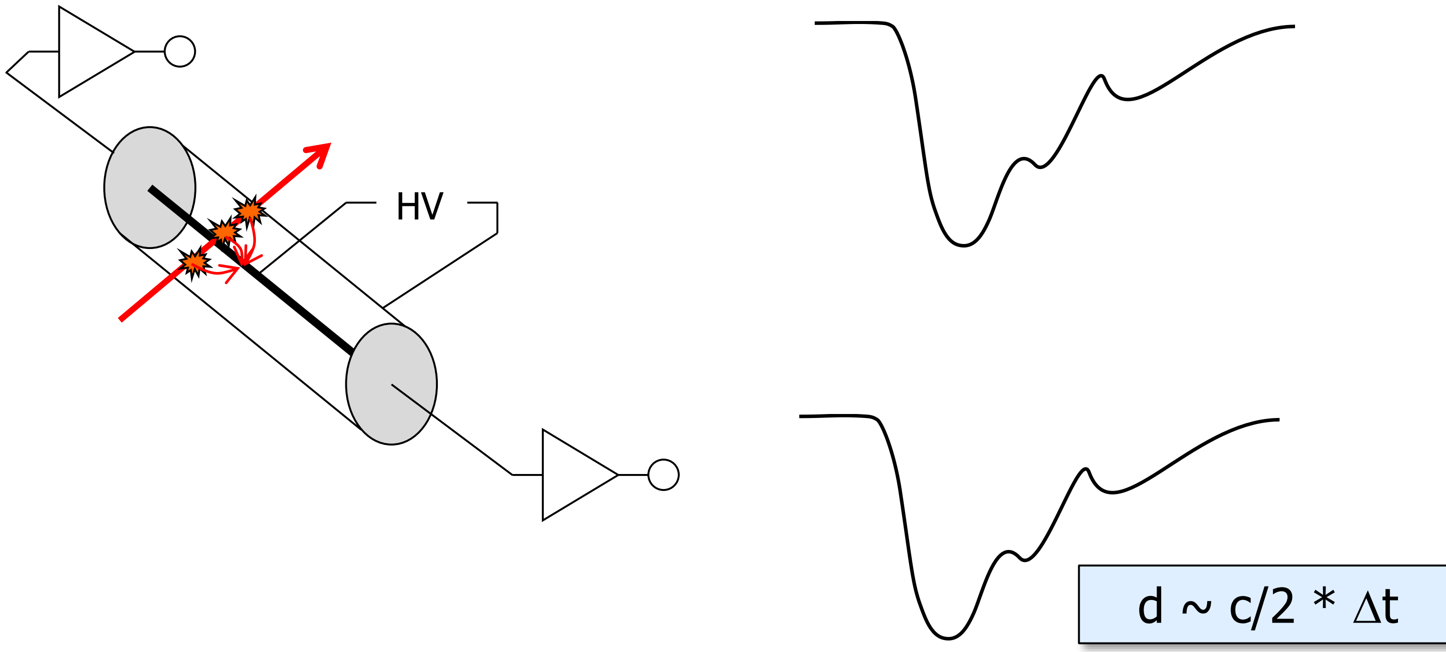
Assumes ideal sampling ↓

	U	Δu	f_s	f_{3db}	Δt
today:	100 mV	1 mV	2 GSPS	300 MHz	~10 ps
optimized SNR:	1 V	1 mV	2 GSPS	300 MHz	1 ps
next generation:	1 V	1 mV	10 GSPS	3 GHz	0.1 ps



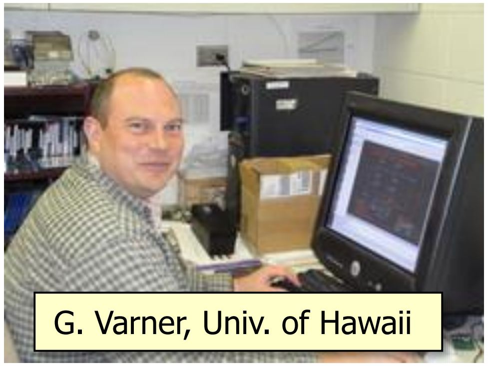
"Novel Calibration Method for Switched Capacitor Arrays Enables Time Measurements width Sub-Picosecond Resolution",
D.A. Stricker-Shaver, S. Ritt, B.J. Pichler, IEEE **TNS 61** (2014), 3607

Readout of Straw Tubes



- Readout of straw tubes or drift chambers usually with "charge sharing": 1-2 cm resolution
- Readout with fast timing: 10 ps / √10 = 3 ps → 0.5 mm
- Currently ongoing research project at PSI

Switched Capacitor Arrays for Particle Physics



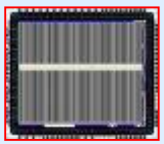
G. Varner, Univ. of Hawaii

E. Delagnes
D. Breton
CEA Saclay

H. Frisch et al., Univ. Chicago

STRAW3

LABRADOR3

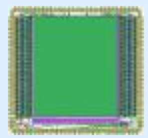


TARGET

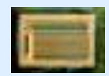
- 0.25 μm TSMC
- Many chips for different projects (Belle, Anita, IceCube …)

www.phys.hawaii.edu/~idlab/

AFTER



SAM



NECTAR0

- 0.35 μm AMS
- T2K TPC, Antares, Hess2, CTA

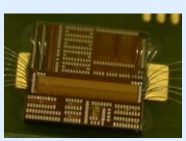
matacq.free.fr

PSEC1 - PSEC4

- 0.13 μm IBM
- Large Area Picosecond Photo-Detectors Project (LAPPD)

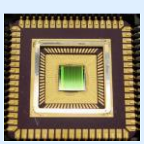
psec.uchicago.edu

DRS1



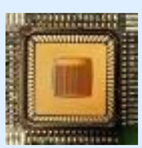
2002

DRS2



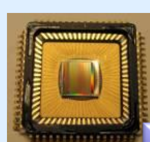
2004

DRS3



2007

DRS4



2008

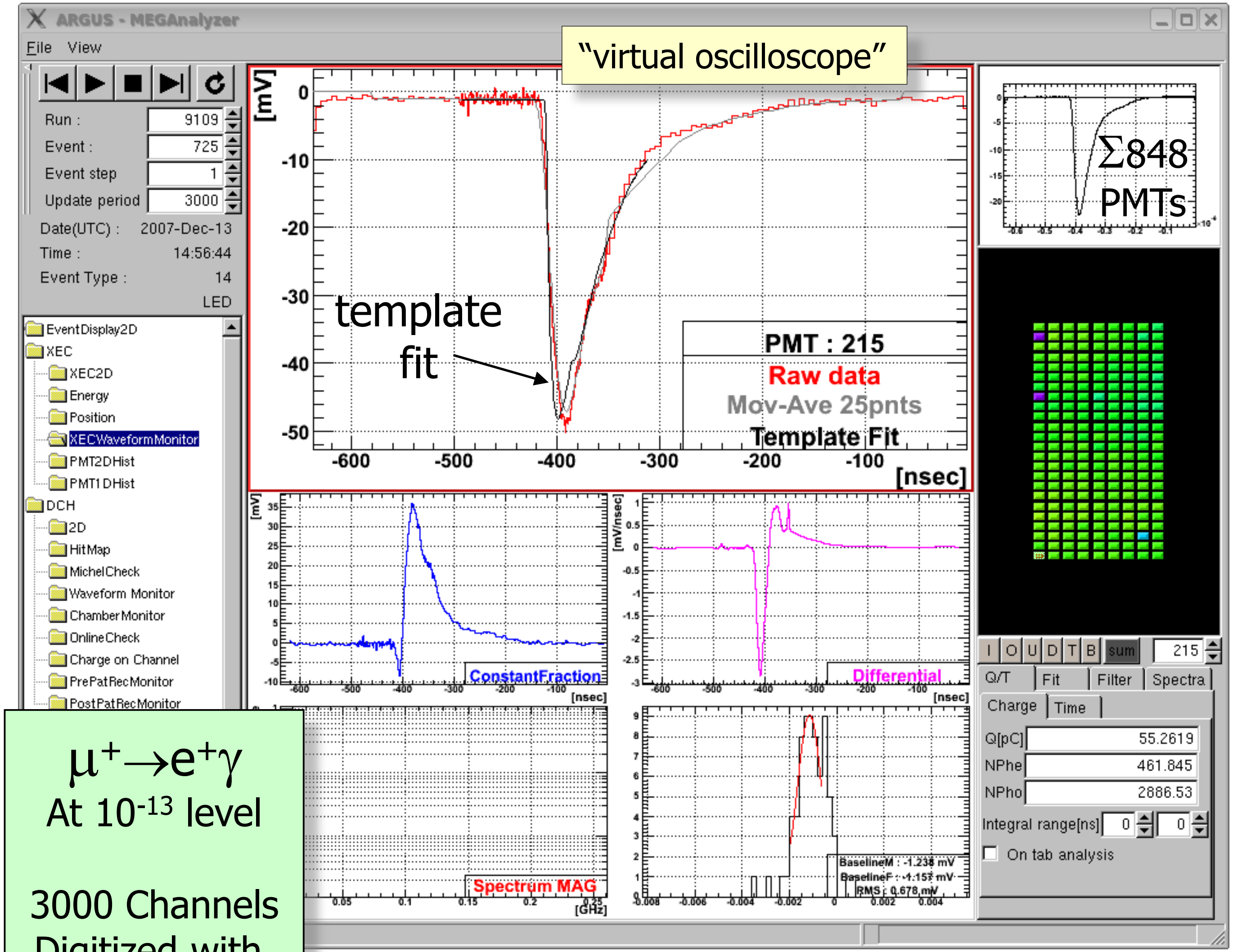
- 0.25 μm UMC
- Universal chip for many applications
- MEG experiment, MAGIC, Veritas, TOF-PET

Poster 15, 106

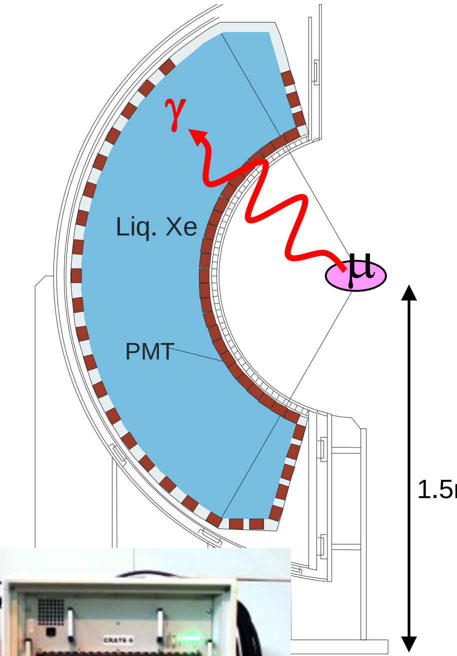
SR
R. Dinapoli
PSI, Switzerland

drs.web.psi.ch

MEG On-line waveform display



"virtual oscilloscope"



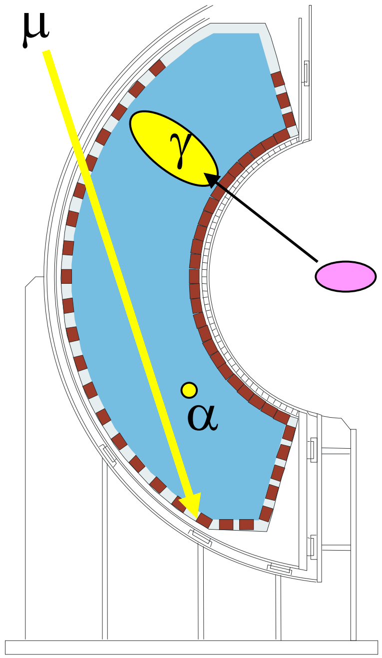
750 Oscilloscopes!

$\mu^+ \rightarrow e^+\gamma$
At 10^{-13} level

3000 Channels Digitized with **DRS4 chips** at 1.6 GSPS

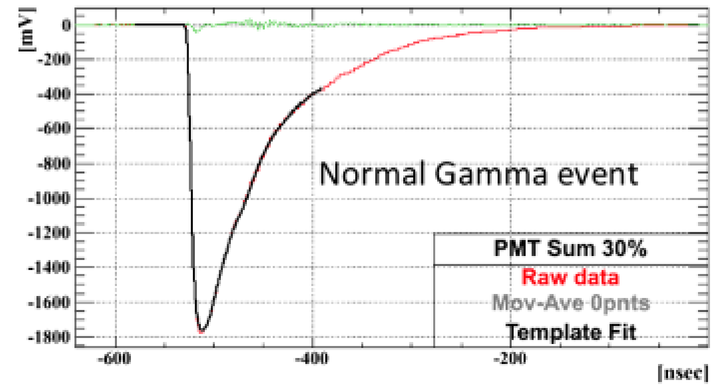
Drawback: 400 TB data/year

Pulse shape discrimination

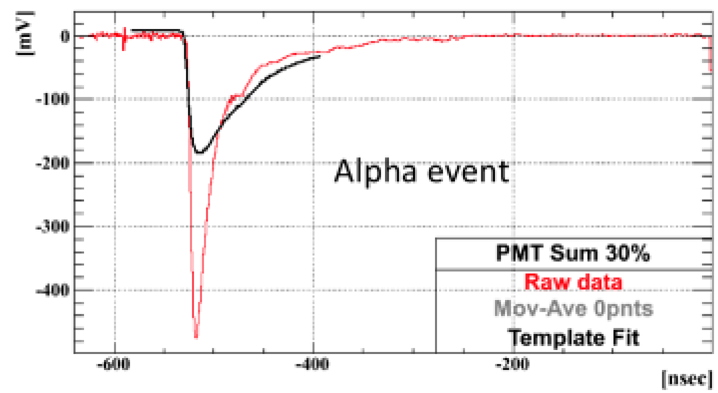


Events found and correctly processed 2 years (!) after the were acquired

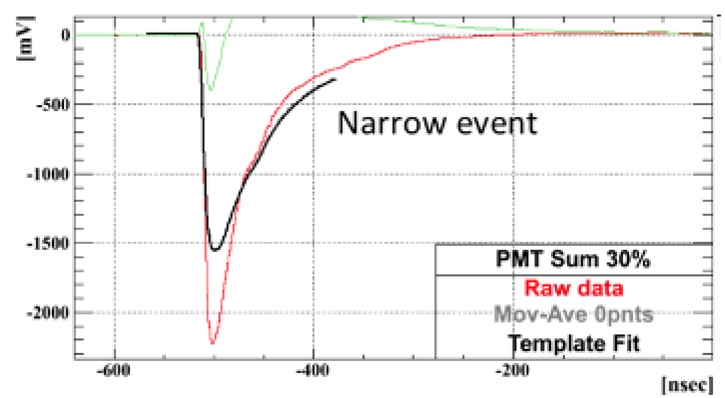
γ



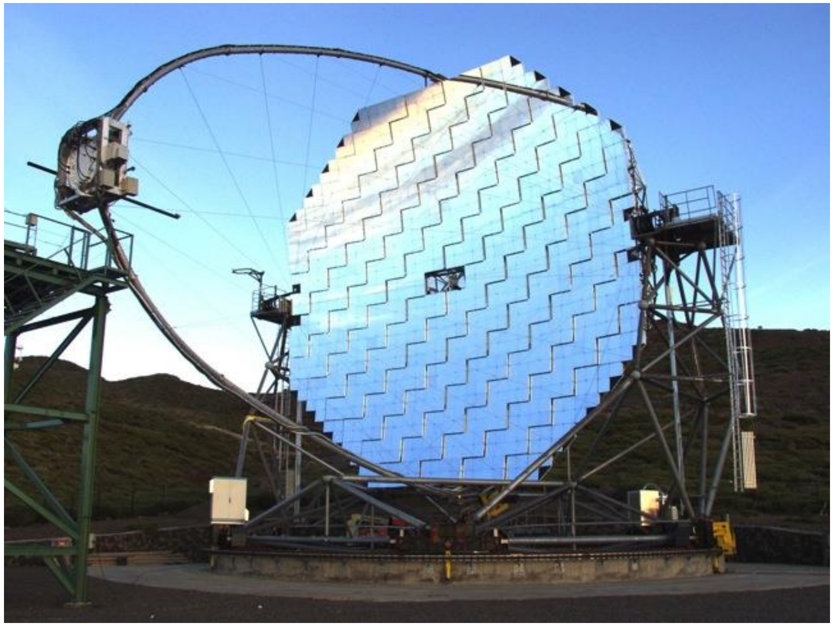
α

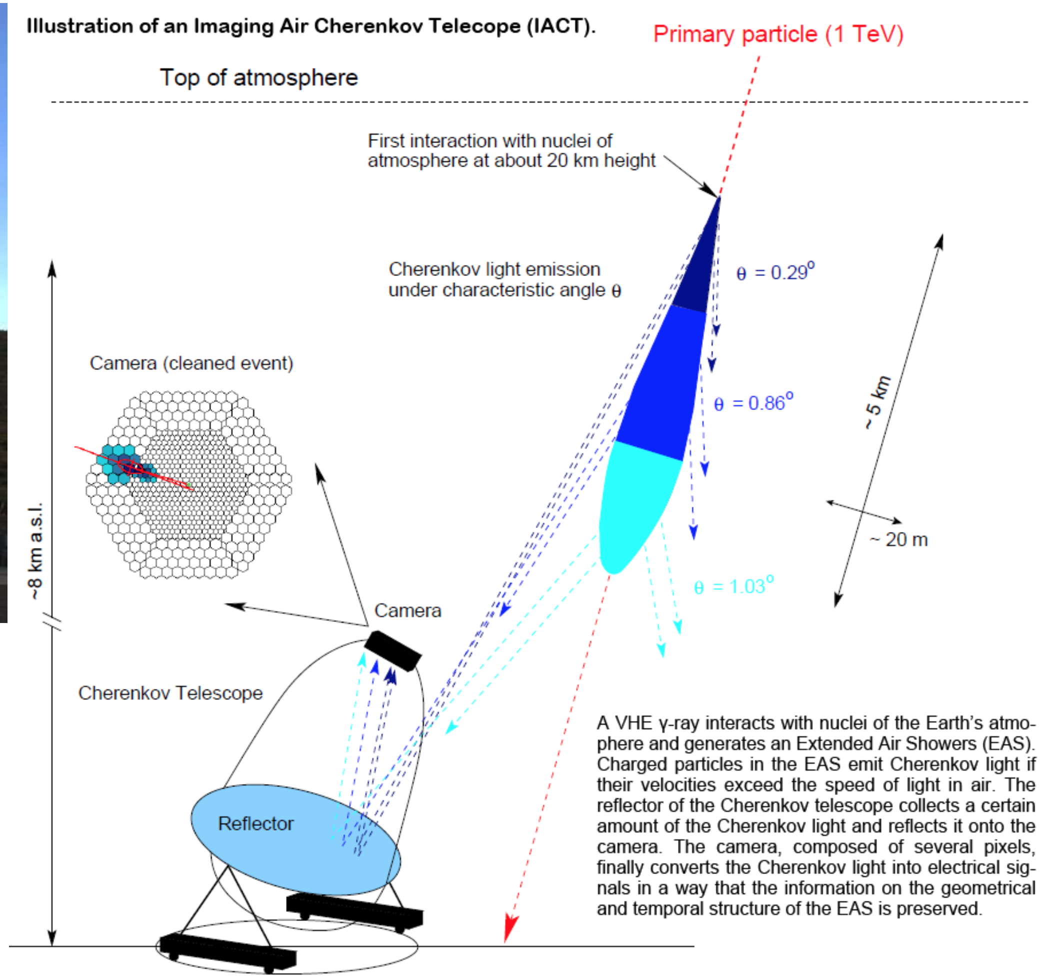


μ

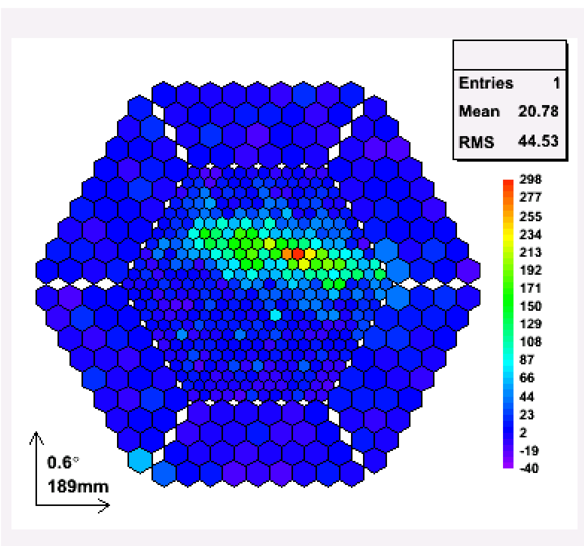


MAGIC Telescope





http://ihp-lx.ethz.ch/Stamet/magic/magicIntro.html



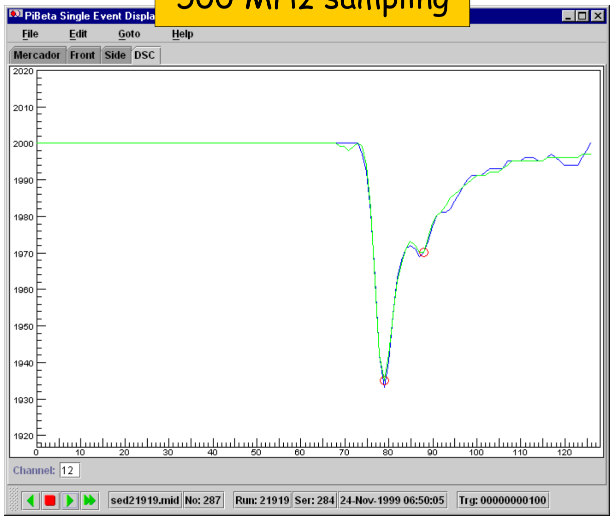
La Palma, Canary Islands, Spain, 2200 m above sea level

https://wwwmagic.mpp.mpg.de/

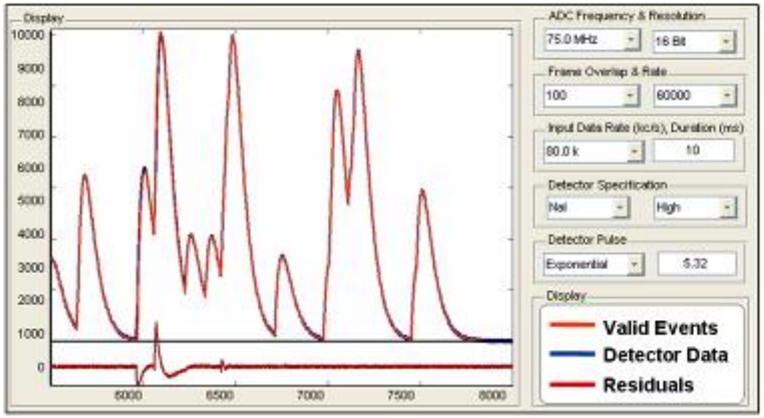
Template Fit

- Determine “standard” PMT pulse by averaging over many events → “Template”
  - Find hit in waveform
  - Shift (“TDC”) and scale (“ADC”) template to hit
  - Minimize χ^2
  - Compare fit with waveform
  - Repeat if above threshold
- Store ADC & TDC values

πβ Experiment
500 MHz sampling



• At 1,000 kc/s less than 10% of events cannot be decoded.



14 bit
60 MHz

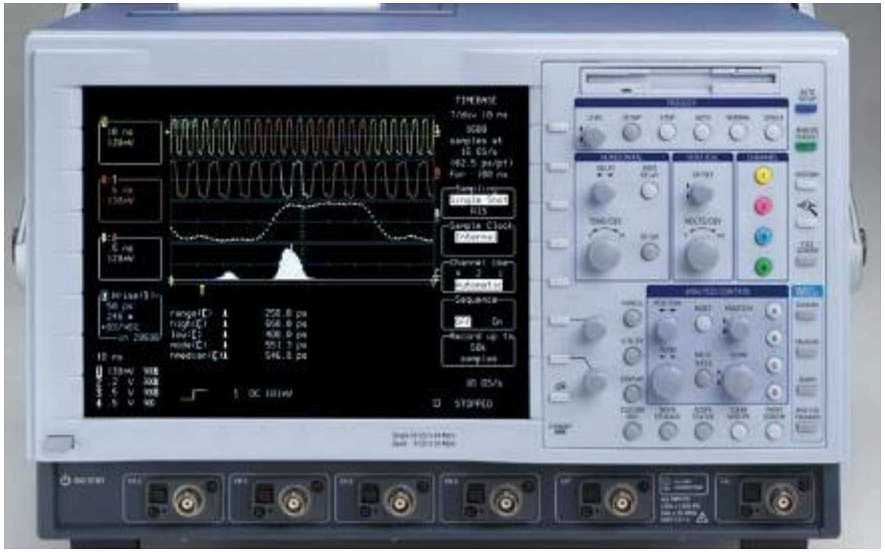
www.southerninnovation.com

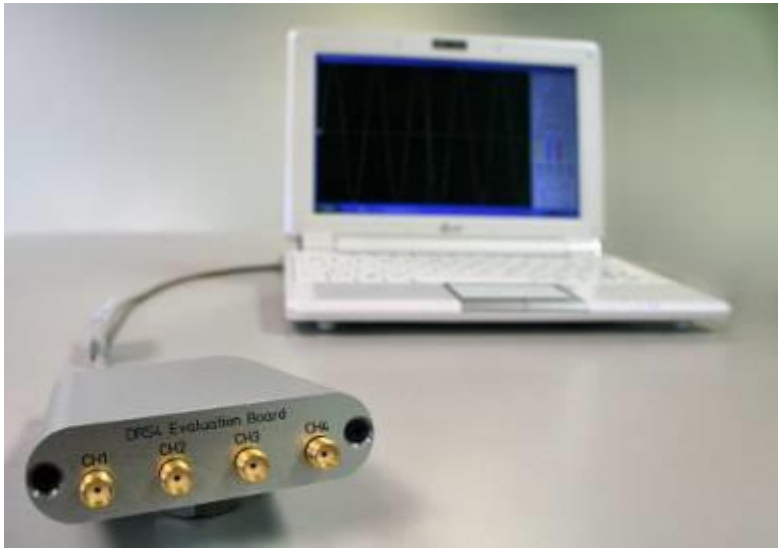
High speed USB oscilloscope

4 channels
5 GSPS
1 GHz BW
8 bit (6-7)
15 k€

→

4 channels
5 GSPS
1 GHz BW
11.5 bits
1170 €
USB Power

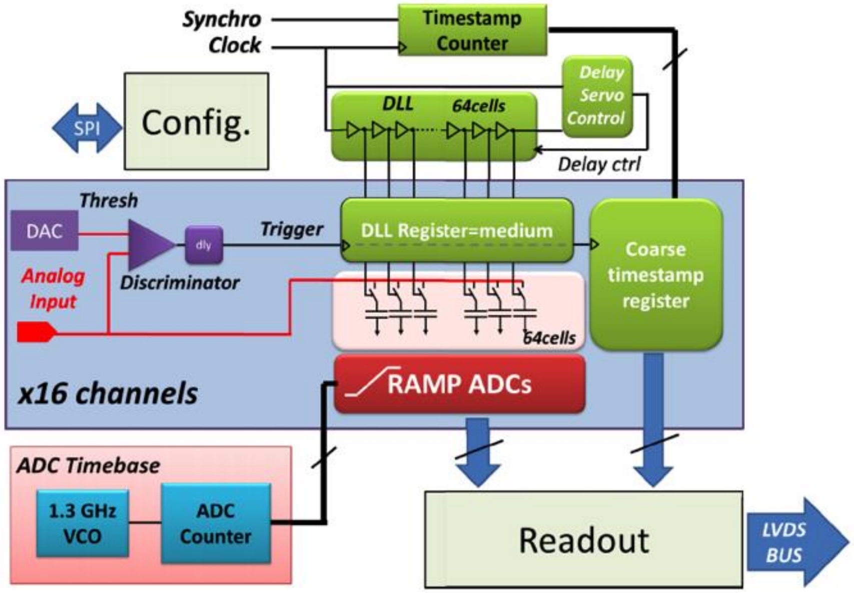




New chips

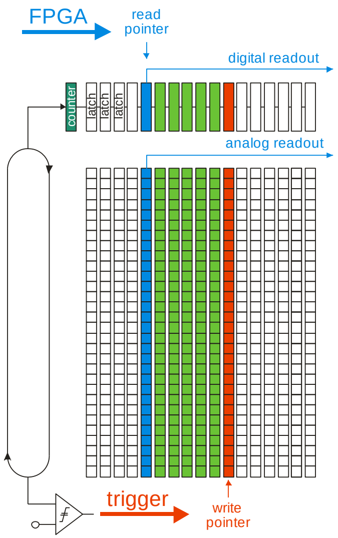
CEA/Saclay

- SAMPIC Waveform TDC
- Record short (64 bins) waveforms
- Digitize on-chip
- Data-driven read out



DRS5 (PSI, planned)

- Self-trigger writing of 128 short 32-bin segments (4096 bins total)
- Storage of 128 events
  - Accommodate long trigger latencies
  - Quasi dead time-free up to a few MHz,
  - Possibility to skip segments → second level trigger



Summary

- Digitization is a key element of all particle physics experiments
- General trend to faster digitization and waveform analysis in digital domain (embedded CPUs, FPGAs)
- This talk can only give you a glimpse
- Further information
  - H. Spieler, "Semiconductor Detector Systems", Oxford Univ. Press, 2005
  - G. Knoll, "Radiation Detection and Measurement", Wiley, 2010
  - Conferences (with short courses):
    IEEE NSS-MIC (Sydney, Australia, Nov. 2018)
    IEEE Realtime (Ho Chi Minh City, Vietnam, June 2020)
  - Become IEEE NPSS member