What is New in MicroTCA.4.1 ?

Kay Rehlich, DESY MicroTCA Technology Lab

Auxiliary Backplane

Protective Covers

AMC / RTM Application Classes

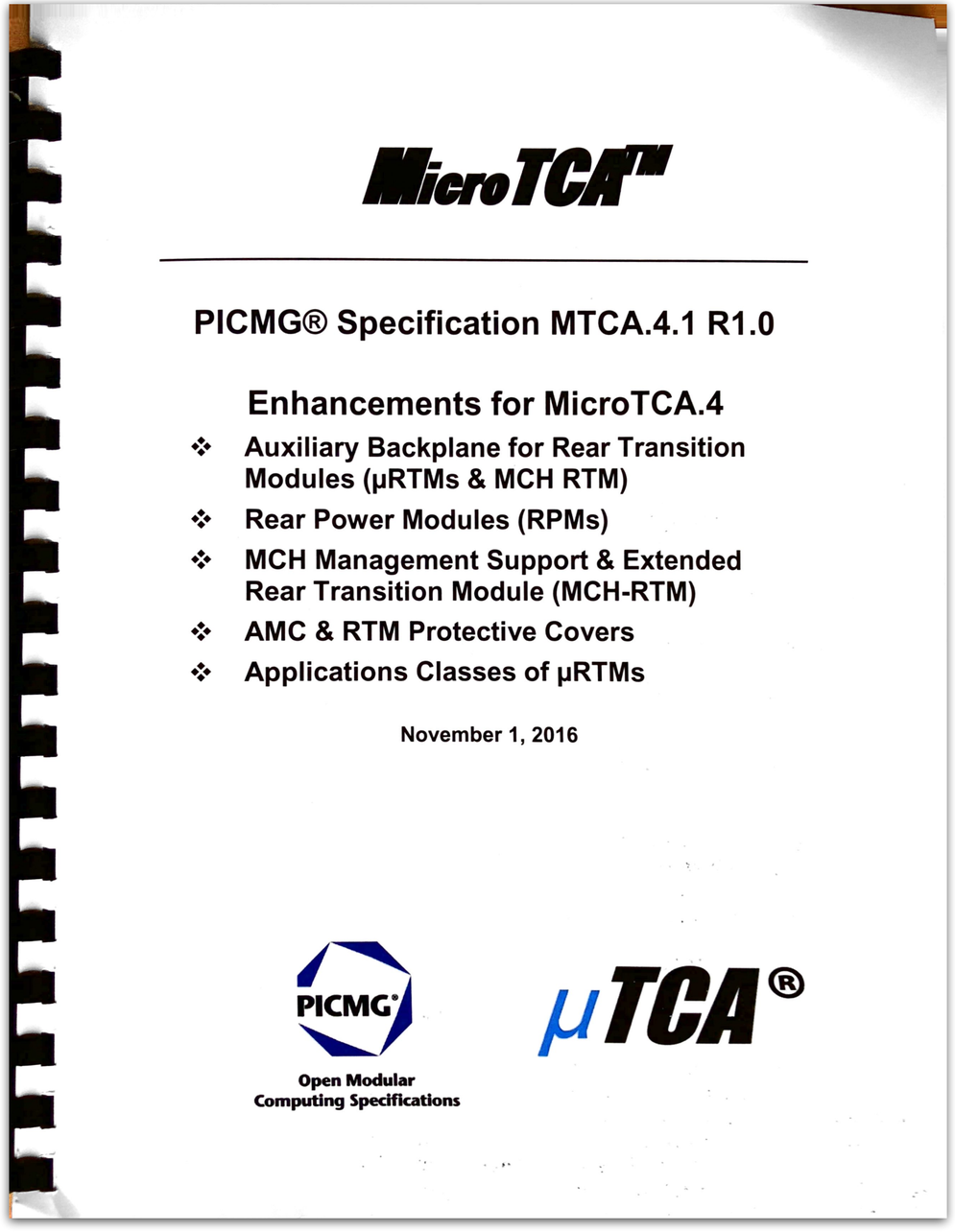
HELMHOLTZ GEMEINSCHAFT

MicroTCA TECHNOLOGY LAB

A HELMHOLTZ INNOVATION LAB

DESY

MTCA.4.1



168 Pages

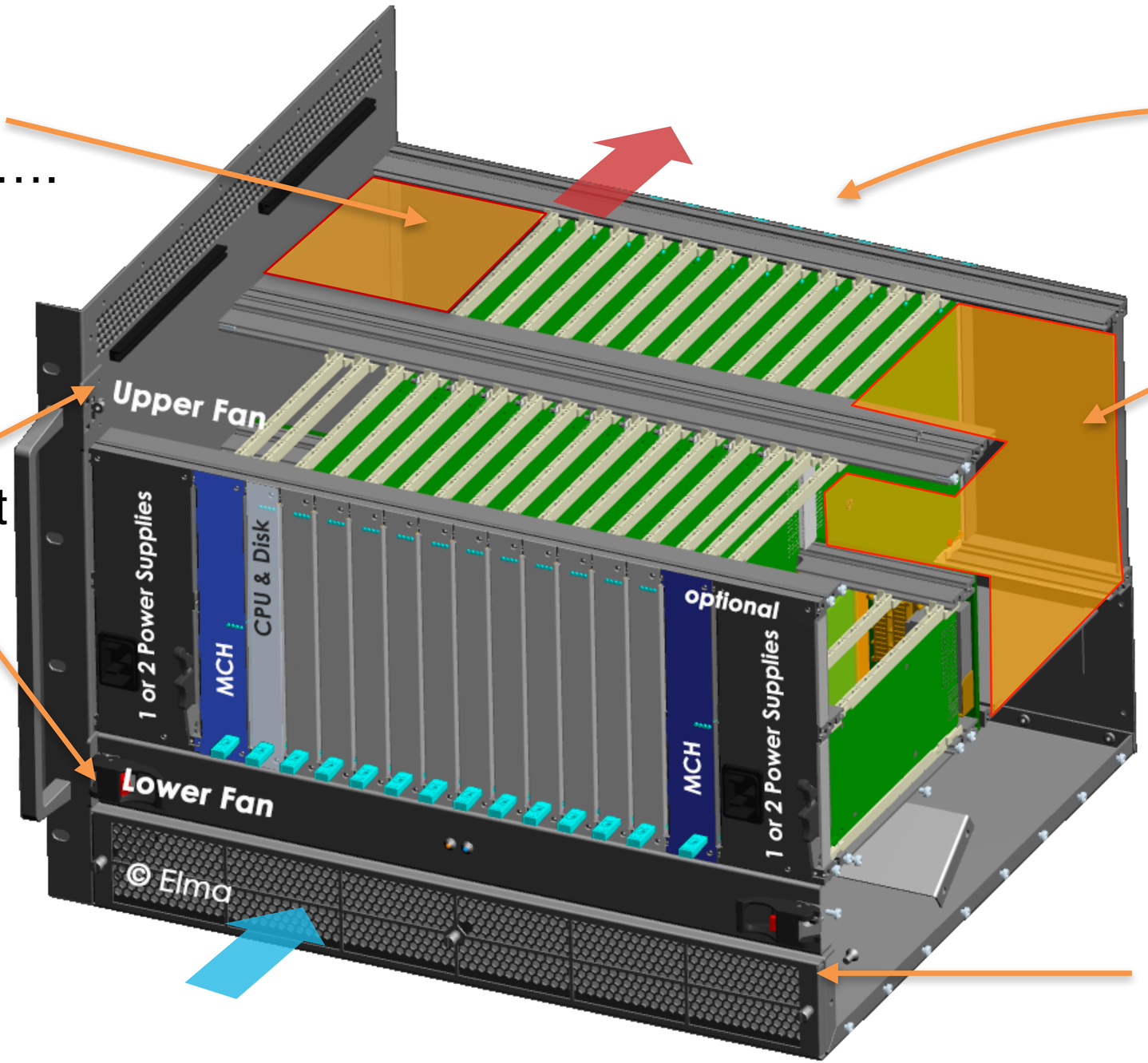
MicroTCA.4: A Modular Crate System

Space for
a CPU & ….

Most cables from rear

Space for ….

Redundant
Fans



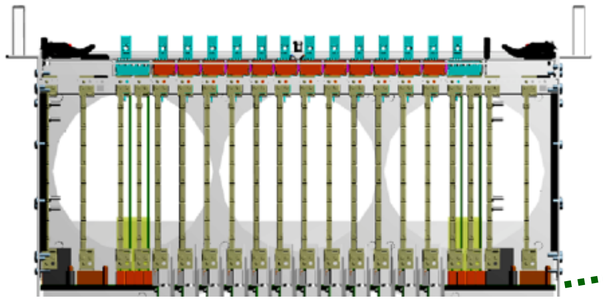
MTCA.4.1

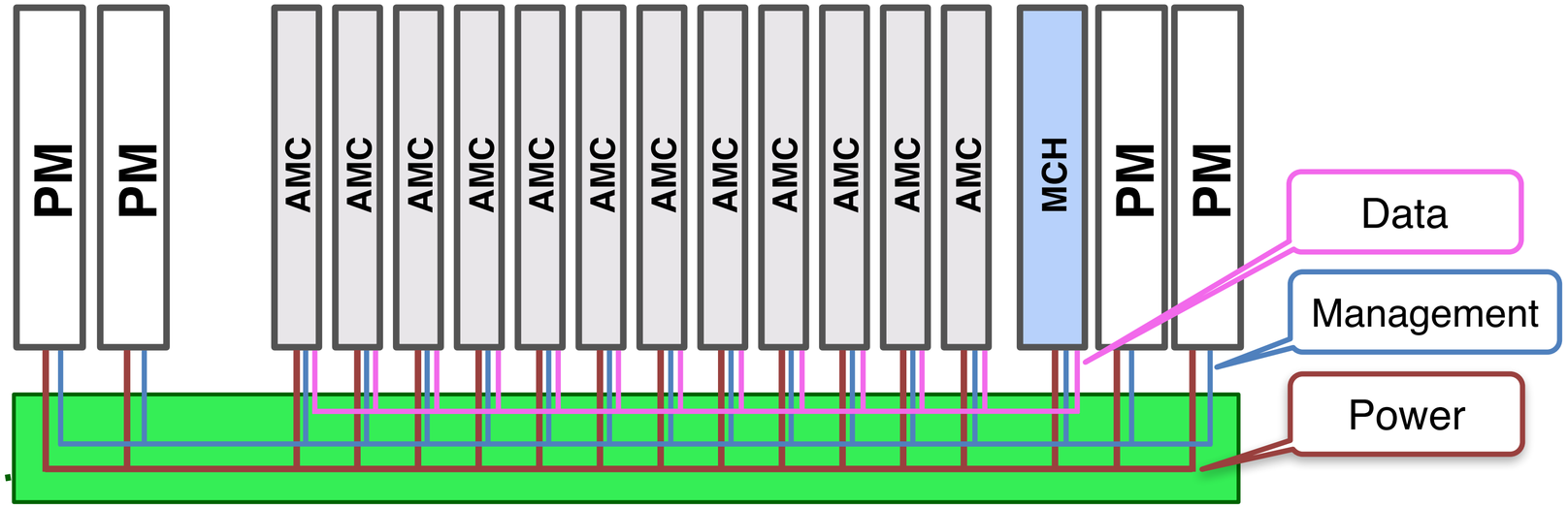
1 … 4 Power Supplies

Filter

MicroTCA Generations: **MTCA.0** MTCA.4 MTCA.4.1

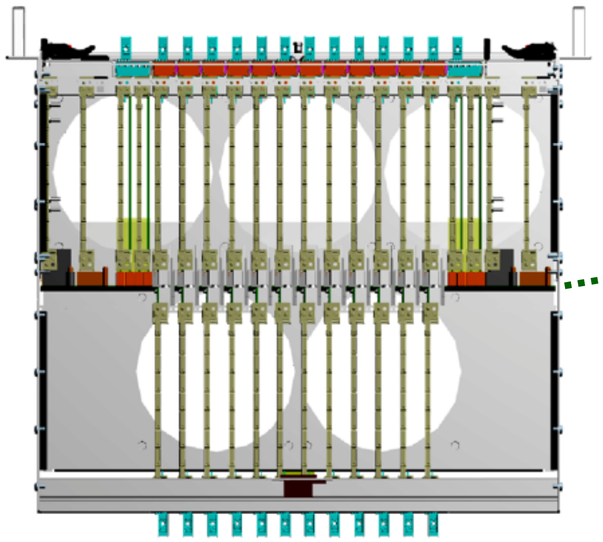
Front Side



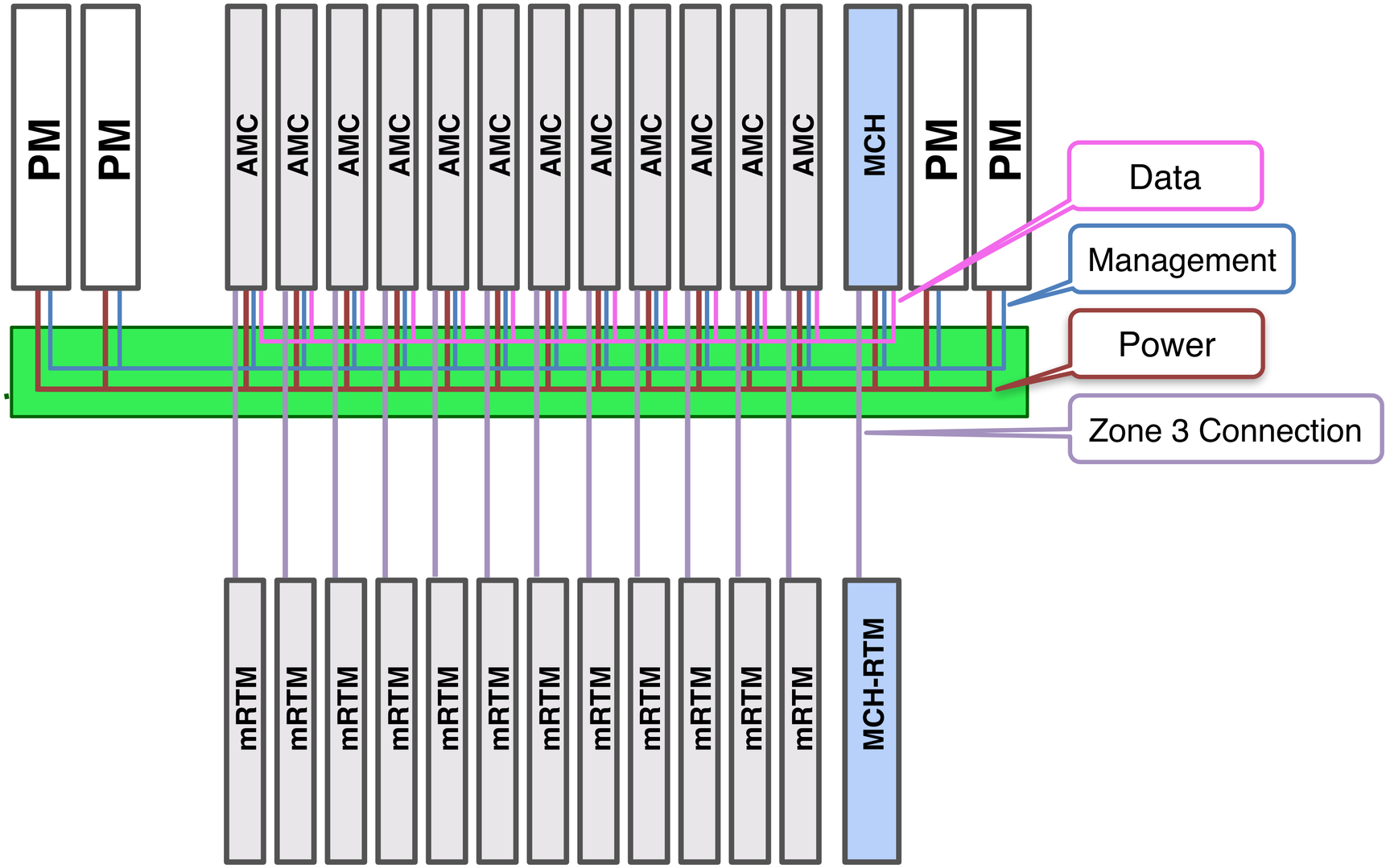


MicroTCA Generations: MTCA.0 **MTCA.4** MTCA.4.1

Front Side

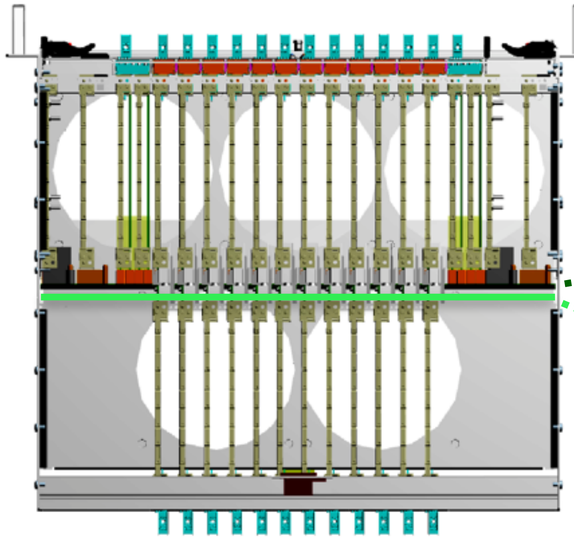


Rear Side

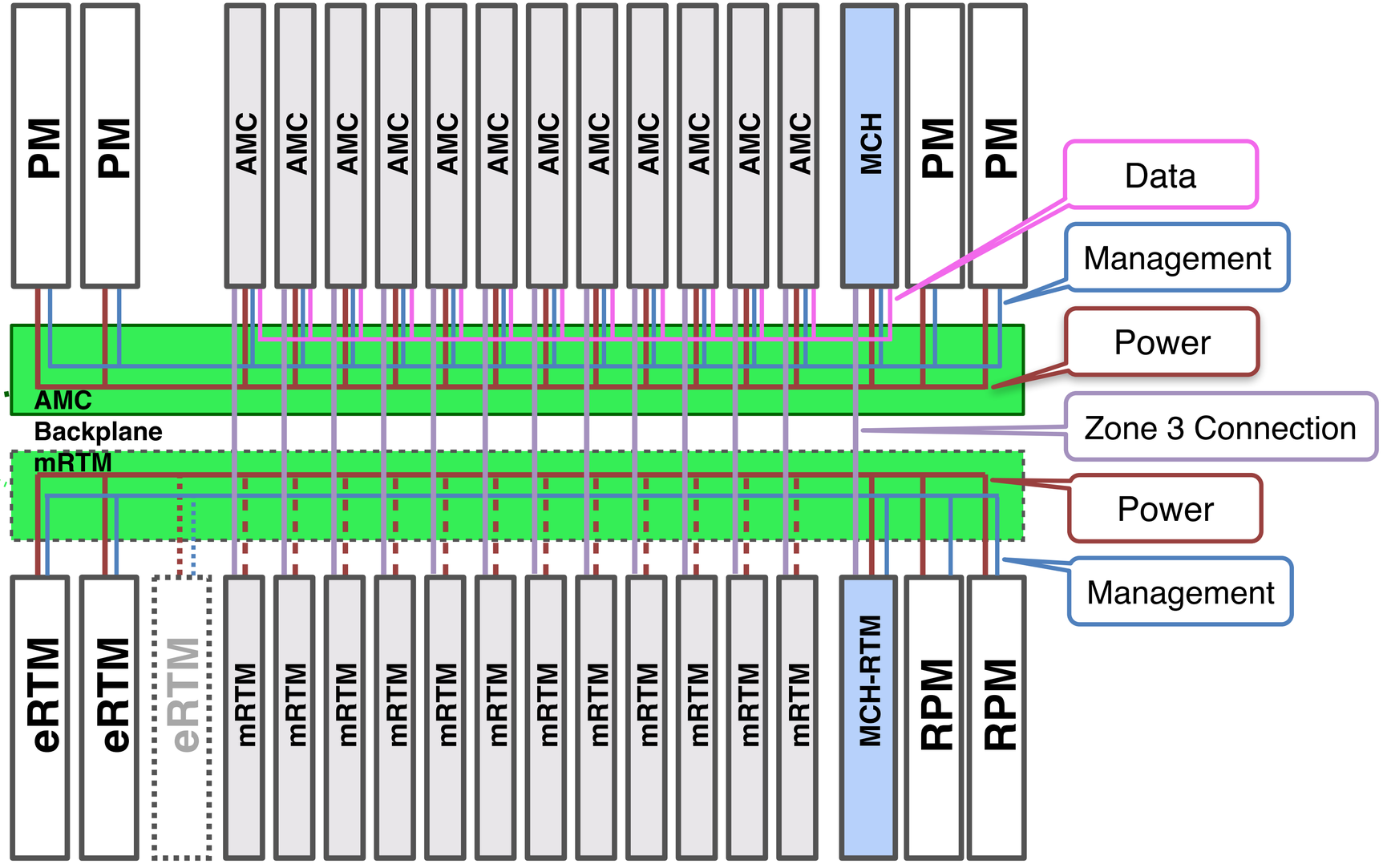


MicroTCA Generations: MTCA.0 MTCA.4 **MTCA.4.1**

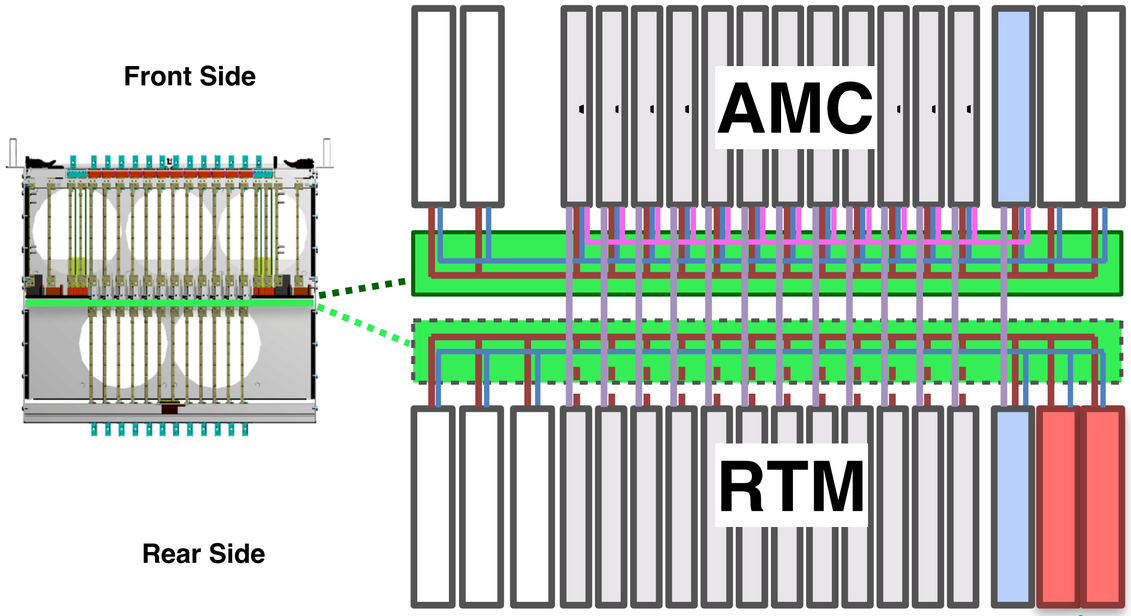
Front Side



Rear Side



MicroTCA.4.1 Rear Power Module



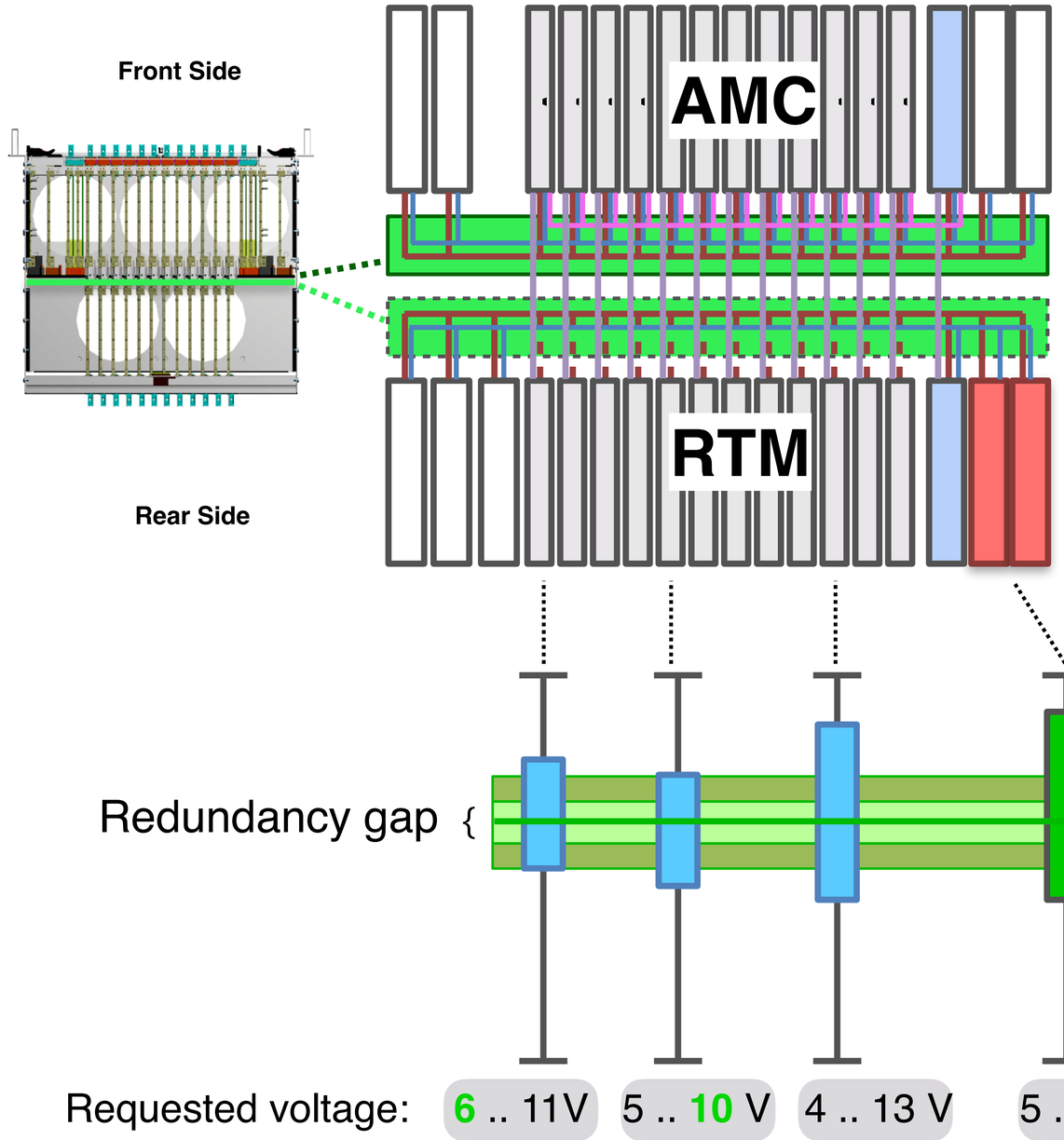
RPM: Rear Power Module

Provides:

- 3.3 V management power to eRTM
- 12 V to eRTM
- Positive variable Voltage to RTM
- Negative variable Voltage to RTM

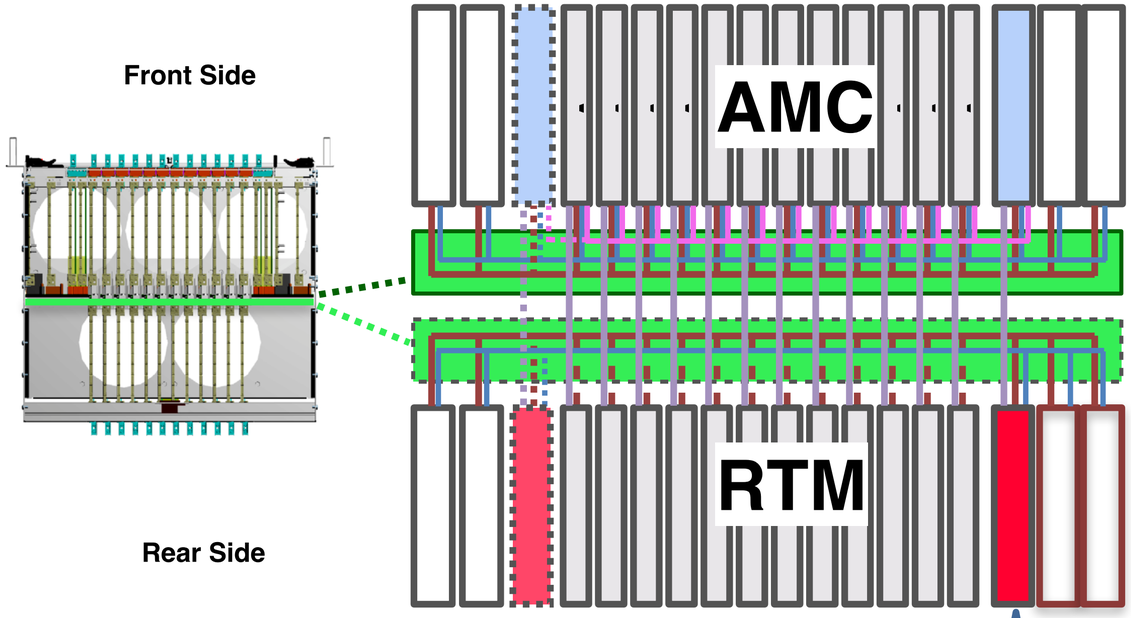
Managed by MCH via MCH-RTM

MicroTCA.4.1 Rear Power Module: Variable Voltage



Example

MicroTCA.4.1 MCH Rear Transition Module

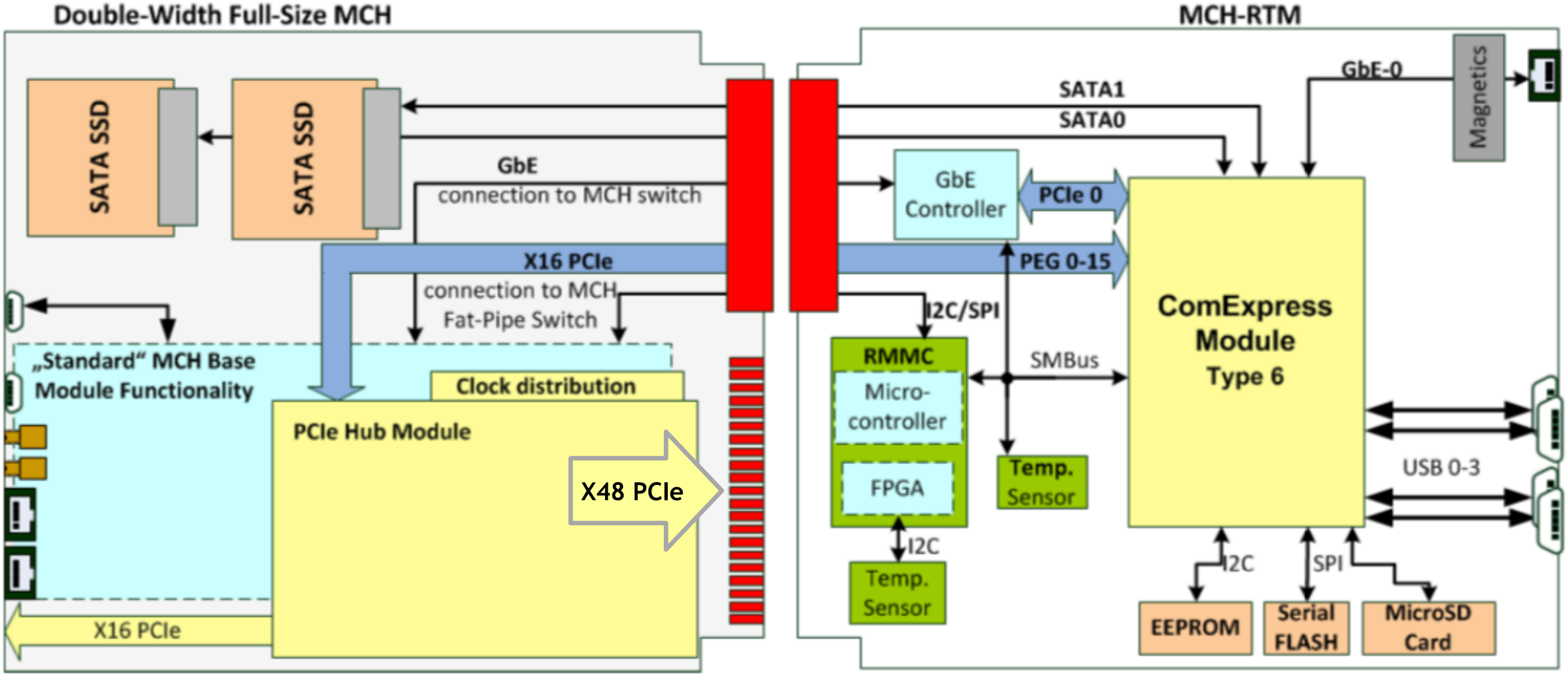


MCH-RTM: MCH Rear Transition Module

- Zone 3 plug is defined in MTCA.4.1
- The MCH is the manager, the RTM links the μRTM Backplane to the MCH
- Low power eRTMs can be powered from the MCH

MicroTCA.4.1 MCH Rear Transition Module

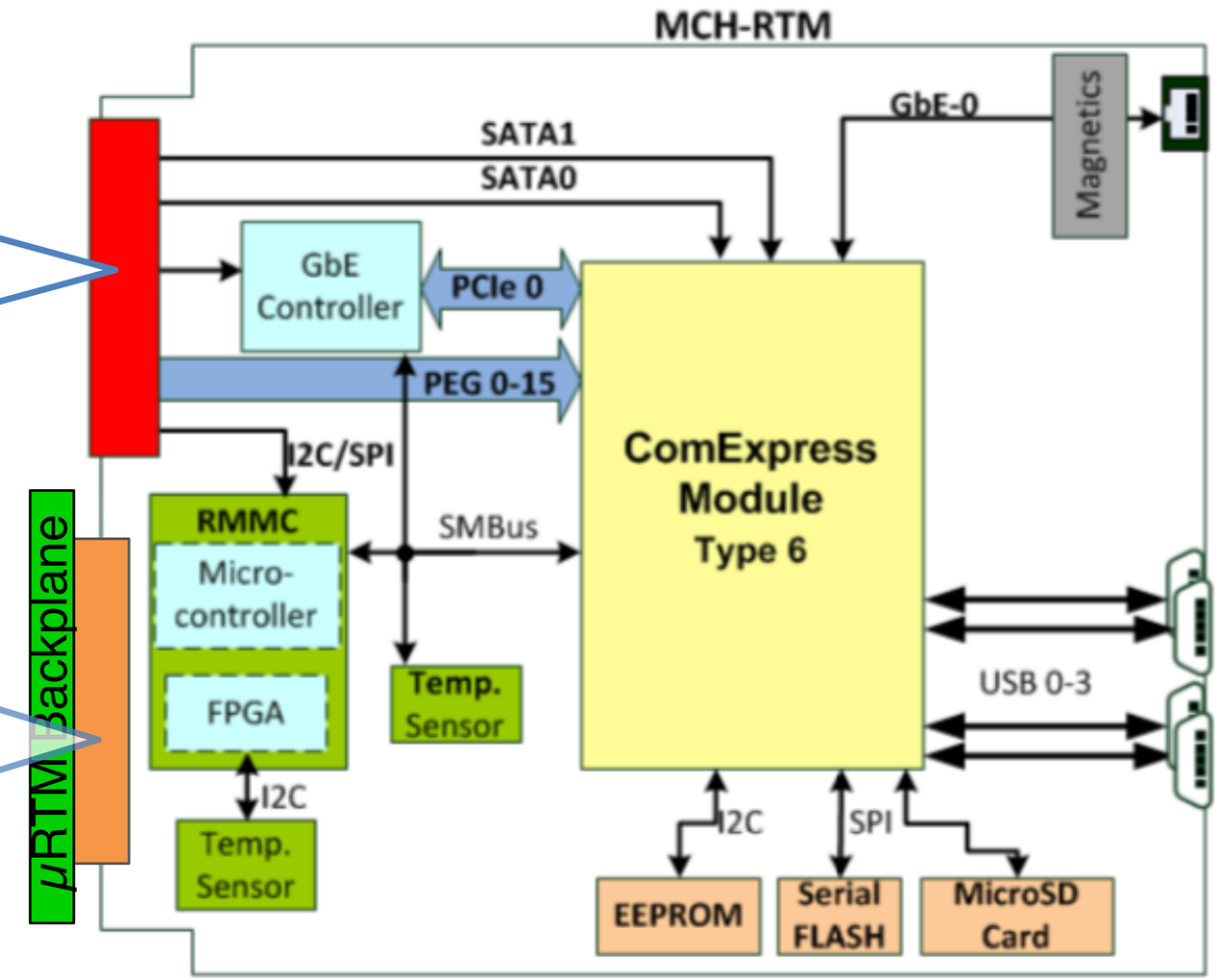
- Up to 16 additional fat-pipe for e.g. a CPU on MCH-RTM
- Management of a second μRTM backplane



MicroTCA.4.1 MCH Rear Transition Module

Zone 3 connector definition:
- 16 fat-pipe (PCIe) lanes
- 2 SATA links
- 2 Ethernet ports
- Management of rear Power Modules
- Management of rear backplane EPROM
- Management of rear eRTMs
- Management of MCH-RTM
- Power

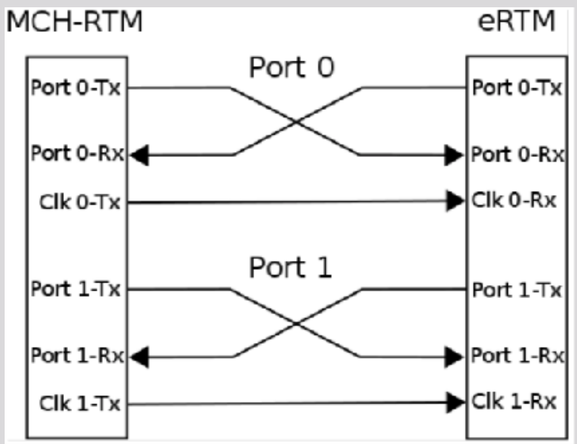
Zone 2 connector definition:
- Management of rear Power Modules
- Management of rear backplane EPROM
- Management & power for rear eRTMs
- 6 LVDS to 3 eRTMs (user defined)

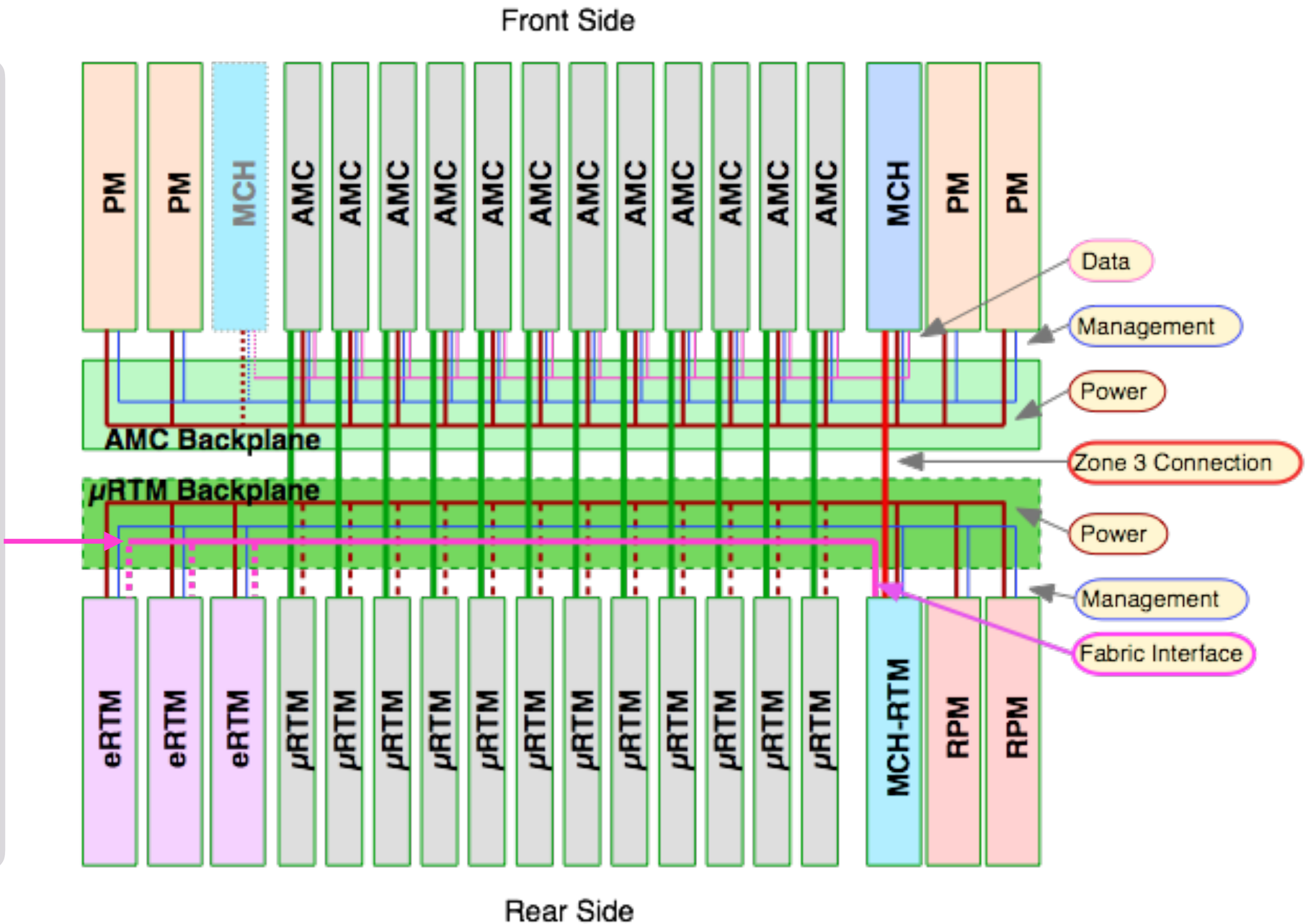


MicroTCA.4.1 MCH-RTM: 3 * 2 Fat-Pipes

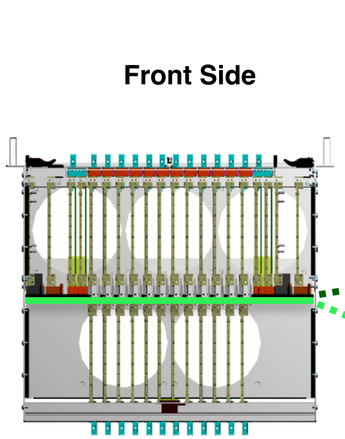
Supported Protocols:

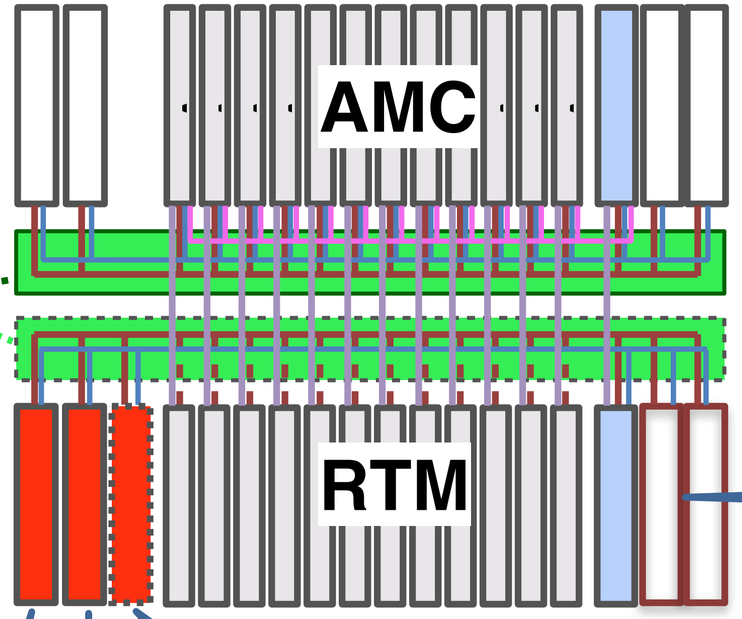
- PCI Express
- PCI Express Advanced Switching
- Ethernet 1000Base-X
- Serial RapidIO
- Serial Peripheral Interface
- Universal Asynchronous Receiver-Transmitter
- Universal Synchronous Receiver-Transmitter
- Ethernet 100Base-T





MicroTCA.4.1 Extended Rear Transition Module





1 or 2 RPM:
Power to:
- eRTM
- μRTM
- MCH-RTM

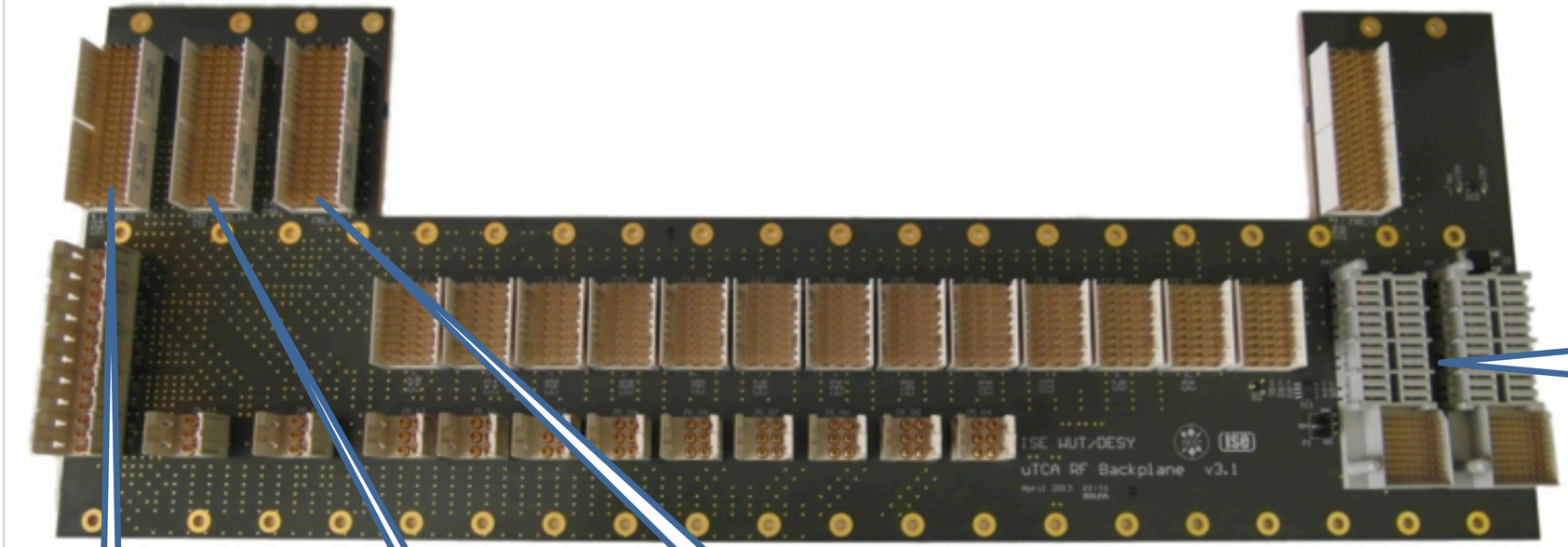
Optional

eRTM 13 or 2nd MCH-RTM:
Power from RPM

eRTM 15:
Power from MCH-RTM or RPM
Example: RF and Clock distribution

eRTM 14:
Power from RPM

Example *µ*RTM Backplane



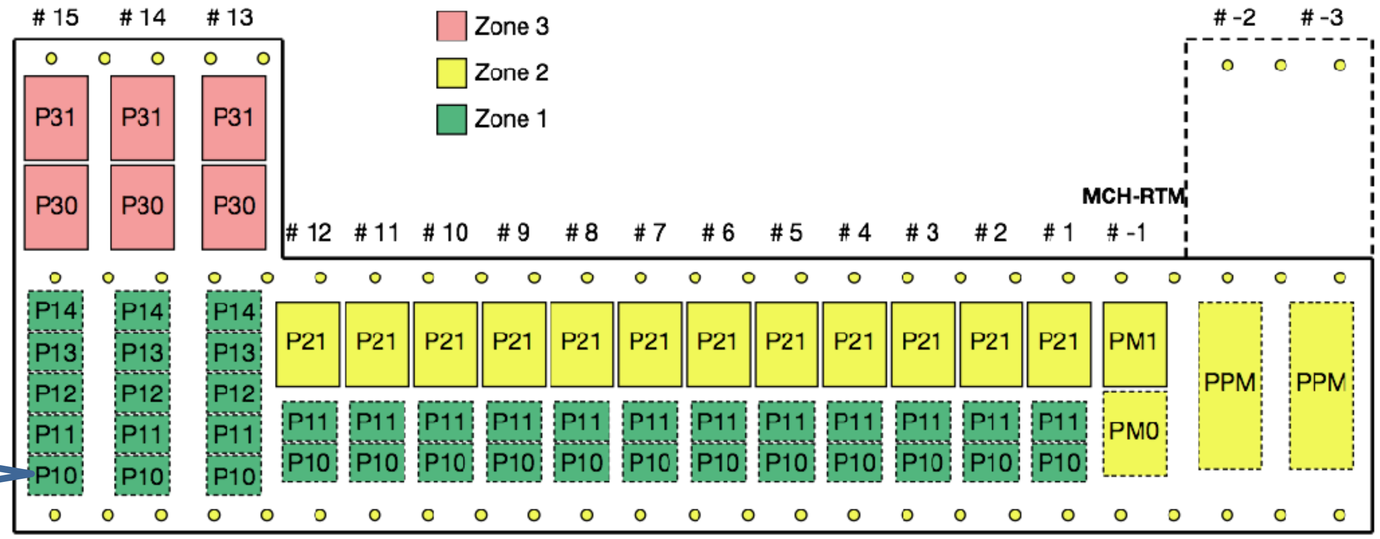
1 or 2 RPM:
Power to:
- eRTM
- *µ*RTM
- MCH-RTM

eRTM 13 or 2nd MCH-RTM:
Power from RPM

eRTM 15:
Power from MCH-RTM or RPM
Example: RF and Clock distribution

eRTM 14:
Power from RPM

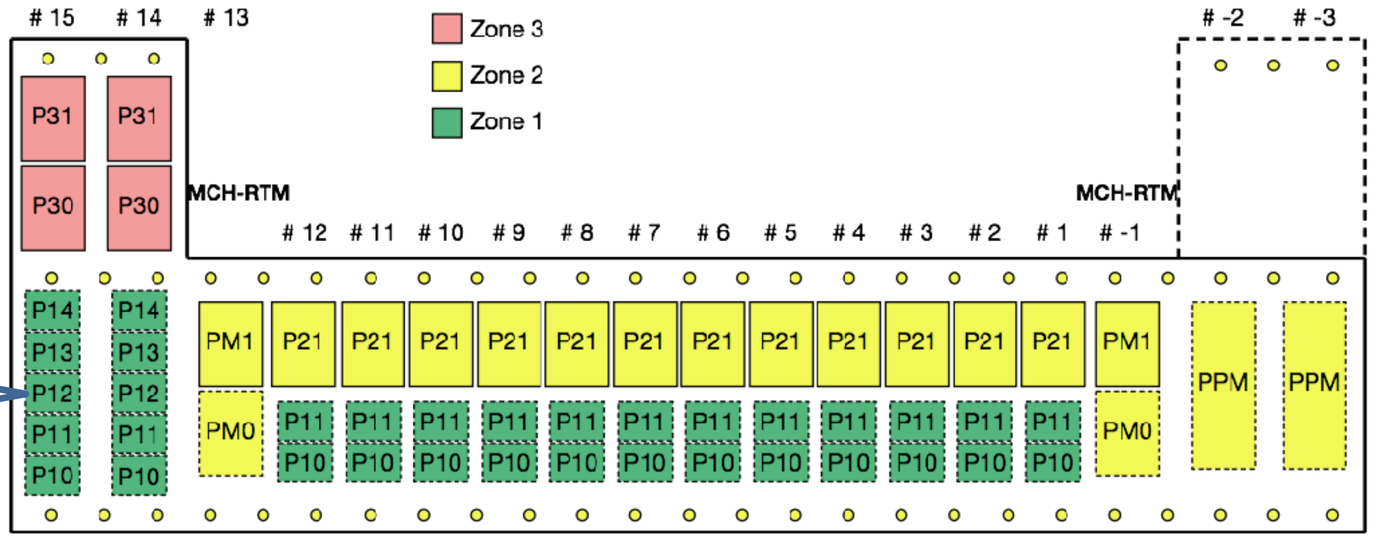
µRTM Backplane



With **one** MCH-RTM

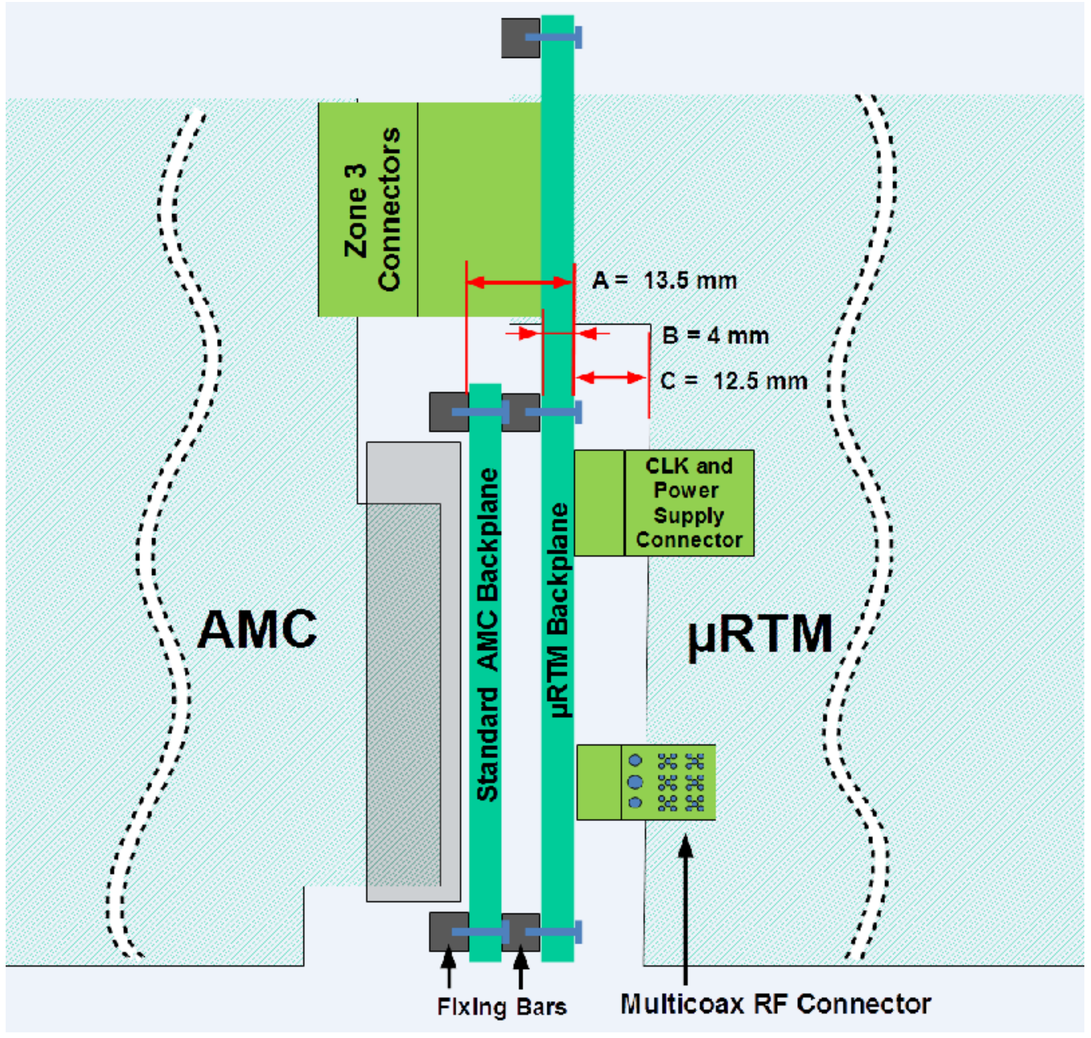
User definable plugs

Example:
Multi-Coax plugs for very low jitter RF and clock distribution



With **two** MCH-RTM

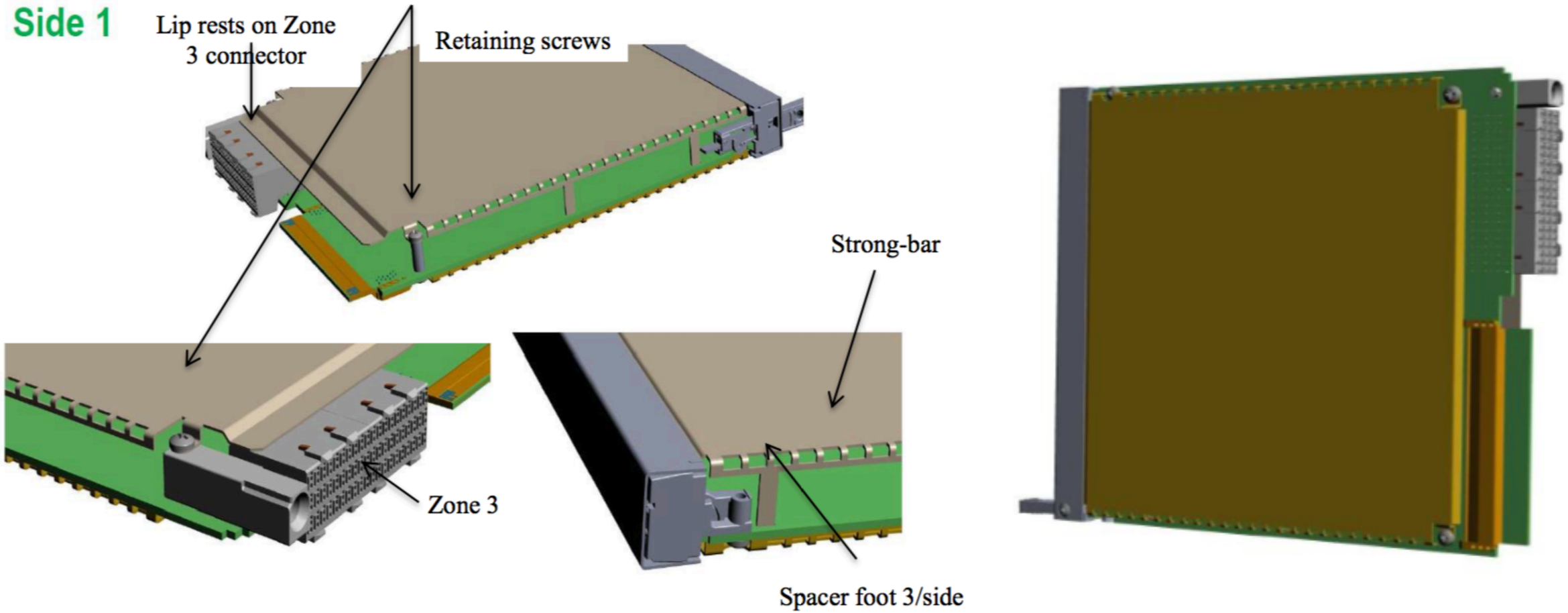
Position of the *µ*RTM Backplane



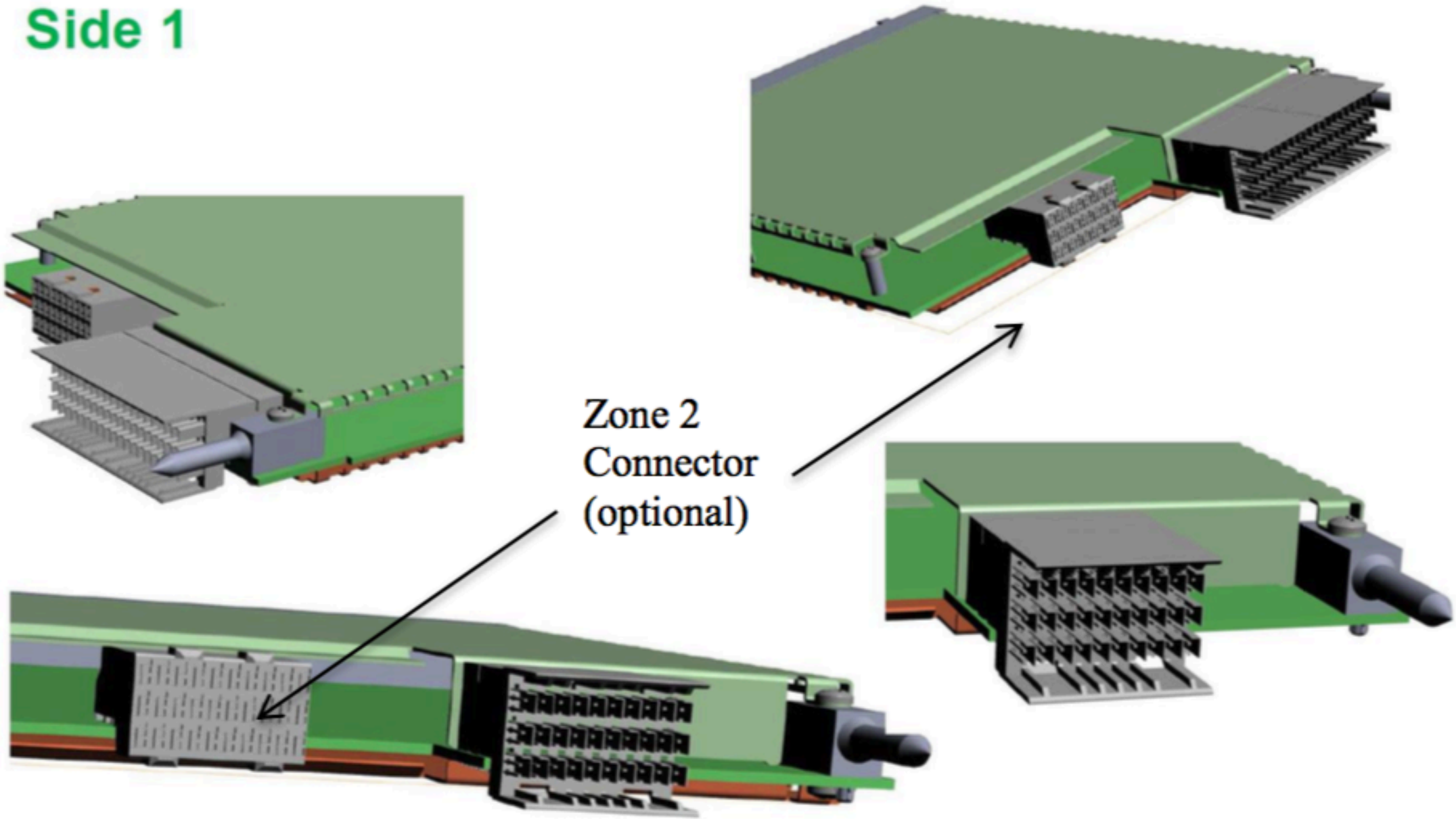
- The distance of the plugs on both backplanes are fixed
  - Independent of the backplane thickness

MicroTCA.4.1 AMC Protective Covers

- Mechanical protection of components
- A bit of shielding (grounded stainless steel with insulating foil)



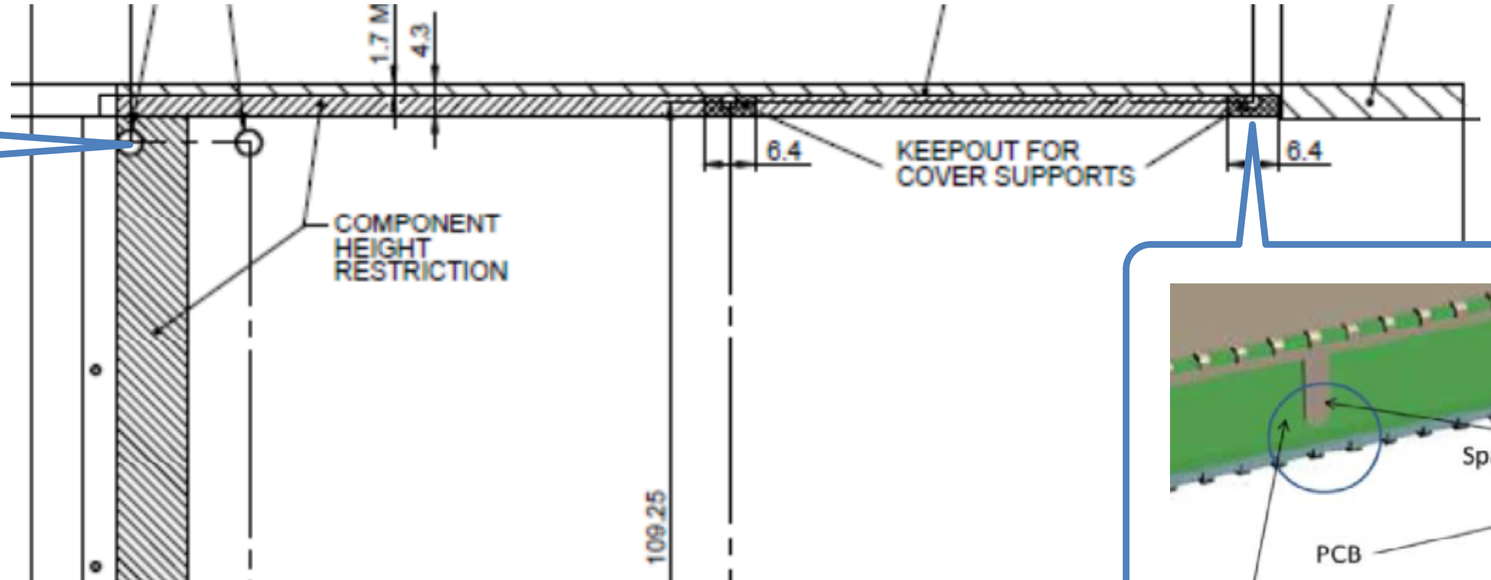
MicroTCA.4.1 RTM Protective Covers

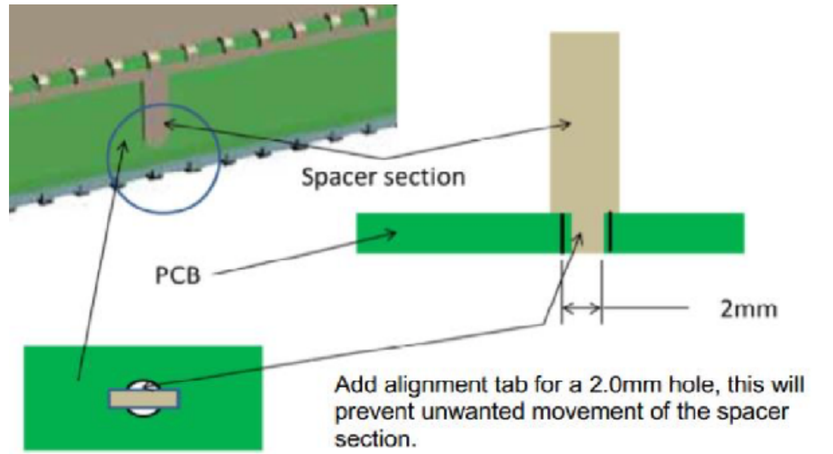


MicroTCA.4.1 AMC Protective Covers

Keying block

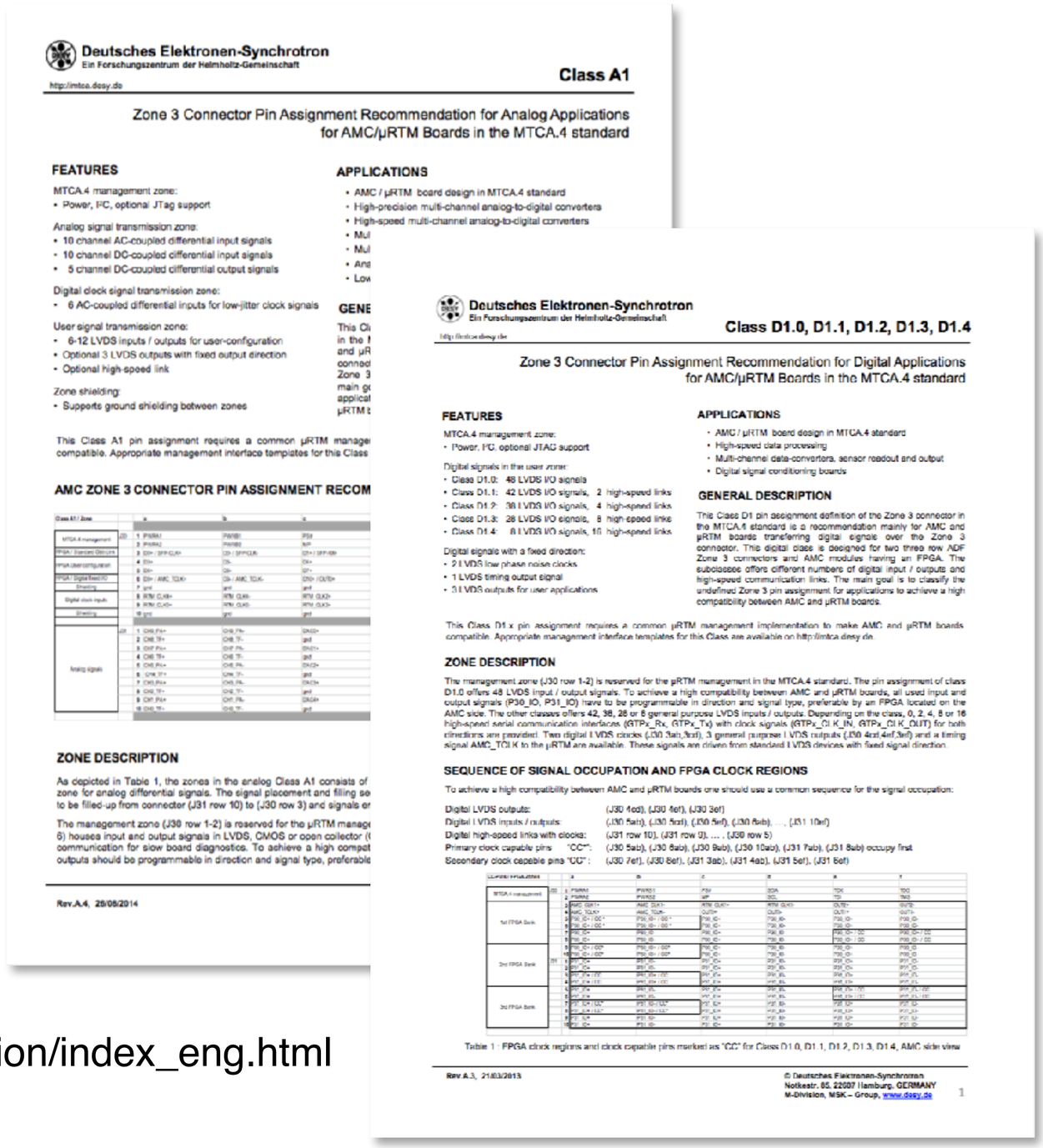
2.7Ø Thru hole for standoff with screw, connected to chassis GND





MicroTCA.4.1 Better Modularity of RTMs: Classes

- Definition of AMC / RTM compatibility by classes and sub-classes
- AMC and RTM both have FRU “Classification Records”
- One module can define compatibility with several classes
- Pin and Signal description of the Zone 3 plug
- Compatibility means: can be switched on
- Compatibility does NOT mean that all features are implemented



Deutsches Elektronen-Synchrotron
Ein Forschungszentrum der Helmholtz-Gemeinschaft
http://mtca.desy.de

Class A1

Zone 3 Connector Pin Assignment Recommendation for Analog Applications for AMC/µRTM Boards in the MTCA.4 standard

FEATURES

MTCA.4 management zone:
- Power, I²C, optional JTag support

Analog signal transmission zone:
- 10 channel AC-coupled differential input signals
- 10 channel DC-coupled differential input signals
- 5 channel DC-coupled differential output signals

Digital clock signal transmission zone:
- 6 AC-coupled differential inputs for low-jitter clock signals

User signal transmission zone:
- 6-12 LVDS inputs / outputs for user-configuration
- Optional 3 LVDS outputs with fixed output direction
- Optional high-speed link

Zone shielding:
- Supports ground shielding between zones

APPLICATIONS

- AMC / µRTM board design in MTCA.4 standard
- High-precision multi-channel analog-to-digital converters
- High-speed multi-channel analog-to-digital converters

This Class A1 pin assignment requires a common µRTM manage compatible. Appropriate management interface templates for this Class

AMC ZONE 3 CONNECTOR PIN ASSIGNMENT RECOM

ZONE DESCRIPTION

As depicted in Table 1, the zones in the analog Class A1 consists of zone for analog differential signals. The signal placement and filling se to be filled-up from connector (J31 row 10) to (J30 row 3) and signals or

The management zone (J30 row 1-2) is reserved for the µRTM manage 6) houses input and output signals in LVDS, CMOS or open collector (communication for slow board diagnostics. To achieve a high compat outputs should be programmable in direction and signal type, preferable

Rev.A.4, 25/08/2014

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http://mtca.desy.de

Class D1.0, D1.1, D1.2, D1.3, D1.4

Zone 3 Connector Pin Assignment Recommendation for Digital Applications for AMC/µRTM Boards in the MTCA.4 standard

FEATURES

MTCA.4 management zone:
- Power, I²C, optional JTAG support

Digital signals in the user zone:
- Class D1.0: 48 LVDS I/O signals
- Class D1.1: 42 LVDS I/O signals, 2 high-speed links
- Class D1.2: 36 LVDS I/O signals, 4 high-speed links
- Class D1.3: 28 LVDS I/O signals, 8 high-speed links
- Class D1.4: 8 LVDS I/O signals, 10 high-speed links

Digital signals with a fixed direction:
- 2 LVDS low phase noise clocks
- 1 LVDS timing output signal
- 3 LVDS outputs for user applications

APPLICATIONS

- AMC / µRTM board design in MTCA.4 standard
- High-speed data processing
- Multi-channel data-converters, sensor readout and output
- Digital signal conditioning boards

GENERAL DESCRIPTION

This Class D1 pin assignment definition of the Zone 3 connector in the MTCA.4 standard is a recommendation mainly for AMC and µRTM boards transferring digital signals over the Zone 3 connector. This digital class is designed for two three row ADF Zone 3 connectors and AMC modules having an FPGA. The subclasses offers different numbers of digital input / outputs and high-speed communication links. The main goal is to classify the undefined Zone 3 pin assignment for applications to achieve a high compatibility between AMC and µRTM boards.

This Class D1.x pin assignment requires a common µRTM management implementation to make AMC and µRTM boards compatible. Appropriate management interface templates for this Class are available on http://mtca.desy.de

ZONE DESCRIPTION

The management zone (J30 row 1-2) is reserved for the µRTM management in the MTCA.4 standard. The pin assignment of class D1.0 offers 48 LVDS input / output signals. To achieve a high compatibility between AMC and µRTM boards, all used input and output signals (P30_IO, P31_IO) have to be programmable in direction and signal type, preferable by an FPGA located on the AMC side. The other classes offers 42, 36, 28 or 8 general purpose LVDS inputs / outputs. Depending on the class, 0, 2, 4, 8 or 16 high-speed serial communication interfaces (GTPx_Rx, GTPx_Tx) with clock signals (GTPx_CLK_IN, GTPx_CLK_OUT) for both directions are provided. Two digital LVDS clocks (J30 3ab,3cd), 3 general purpose LVDS outputs (J30 4cd,4ef,3ef) and a timing signal AMC_TCLK to the µRTM are available. These signals are driven from standard LVDS devices with fixed signal direction.

SEQUENCE OF SIGNAL OCCUPATION AND FPGA CLOCK REGIONS

To achieve a high compatibility between AMC and µRTM boards one should use a common sequence for the signal occupation:

Digital LVDS outputs: (J30 4cd), (J30 4ef), (J30 3ef)
Digital LVDS inputs / outputs: (J30 5ab), (J30 5cd), (J30 5ef), (J30 6ab), … , (J31 10ef)
Digital high-speed links with clocks: (J31 row 10), (J31 row 0), … , (J30 row 5)
Primary clock capable pins "CC*": (J30 5ab), (J30 6ab), (J30 6ab), (J30 10ab), (J31 7ab), (J31 8ab) occupy first
Secondary clock capable pins "CC" : (J30 7ef), (J30 6ef), (J31 3ab), (J31 4ab), (J31 5ef), (J31 6ef)

Table 1 : FPGA clock regions and clock capable pins marked as "CC" for Class D1.0, D1.1, D1.2, D1.3, D1.4, AMC side view

Rev.A.3, 21/03/2013

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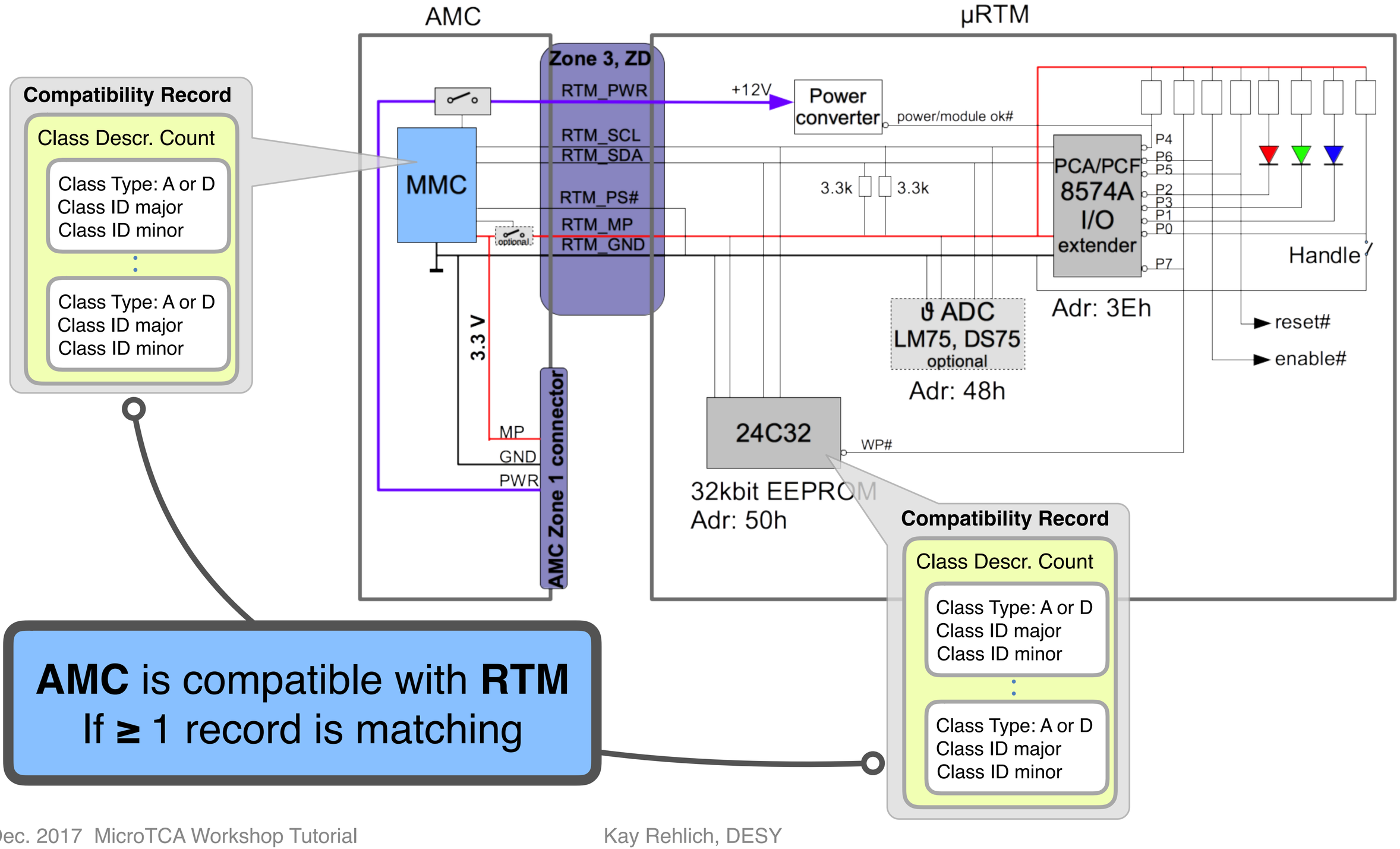
https://mtca.desy.de/resources/zone_3_recommendation/index_eng.html

MicroTCA.4.1 AMC - RTM Compatibility Check: Classes



MicroTCA.4.1 AMC - RTM: Class Definition

- Analog Class **A1**.1
  - 10 differential analog inputs, AC
  - 10 differential analog inputs, DC
  - 5 differential analog outputs, DC
  - Clocks: 6 input, AC
  - 9 differential digital IO
  - 2 high speed links optional
- Analog Class **A2**.1
  - 32 differential analog inputs, DC
  - 4 differential analog outputs, DC
  - Clocks: 2 input (AC), 1 output (LVDS)
  - 6 differential digital IO (LVDS)

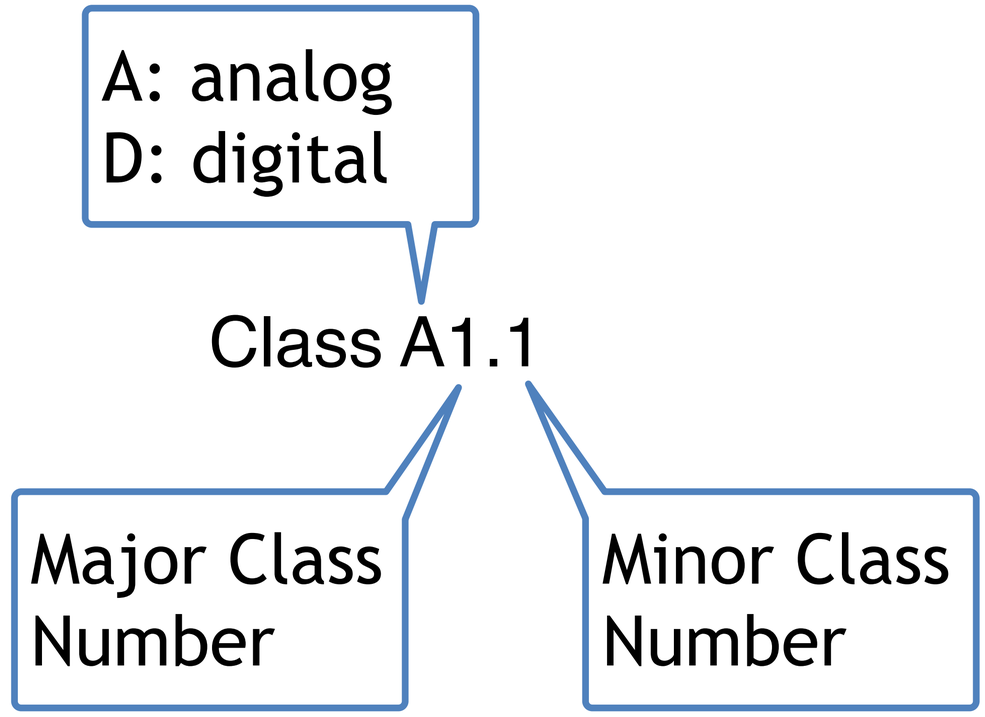


Table 6-9: Zone 3 Classification Descriptor Bytes

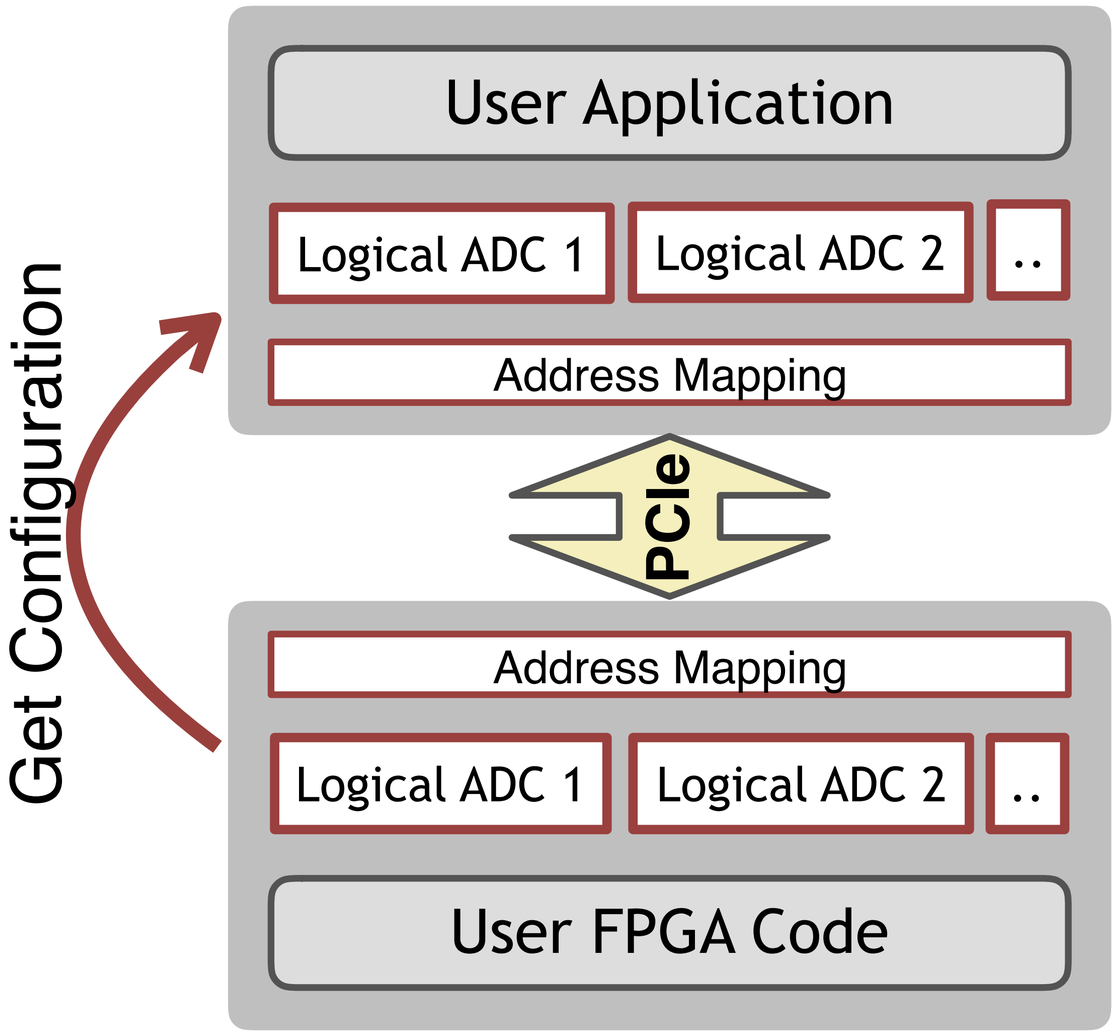
Offset	Length	Field Description
12+m*3	1	Class Type: 0h = Analogue (A) 1h = Digital (D) 3h-FFh = Reserved
13+m*3	1	Class Identifier major number
14+m*3	1	Class Identifier minor number

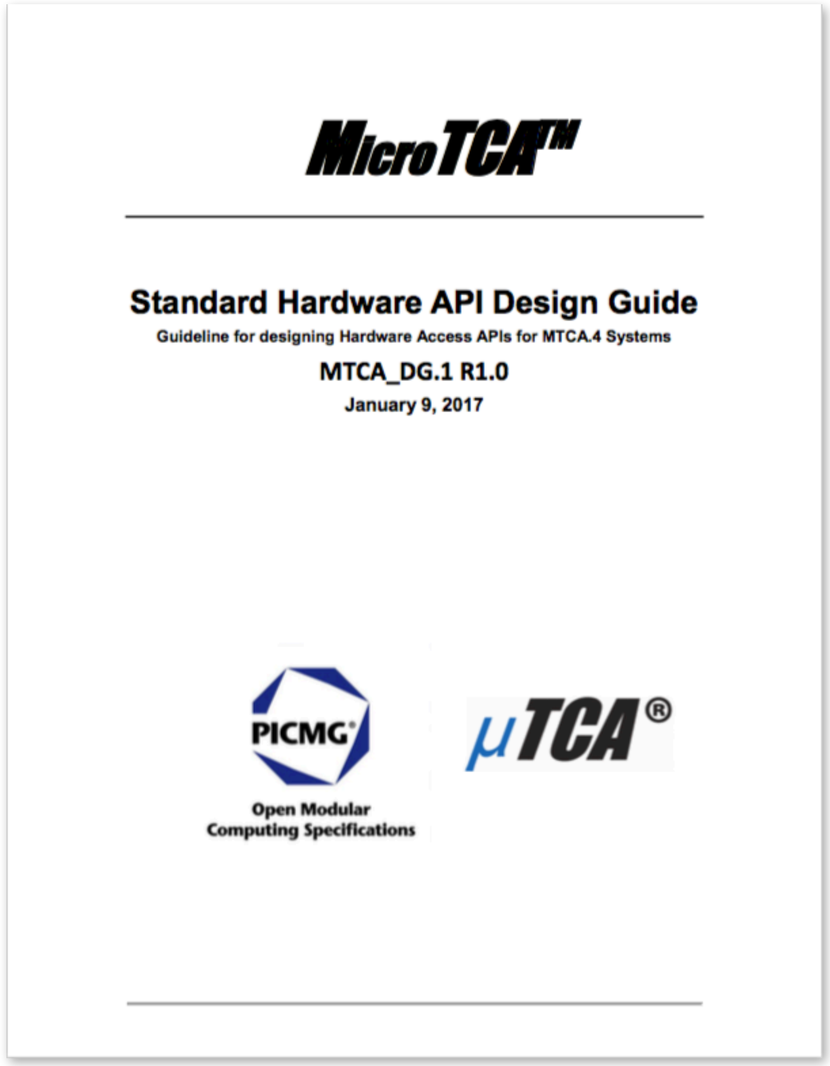
Summary

- **MicroTCA.4.1**
  - ✓ First standard of a rear backplane with full management
  - ✓ Allows very compact and modular designs
  - ✓ Class concept for a modular AMC/RTM compatibility

SHAPI

Standard Hardware API Design Guide




MicroTCA™

Standard Hardware API Design Guide

Guideline for designing Hardware Access APIs for MTCA.4 Systems

MTCA_DG.1 R1.0

January 9, 2017

PICMG® Open Modular Computing Specifications

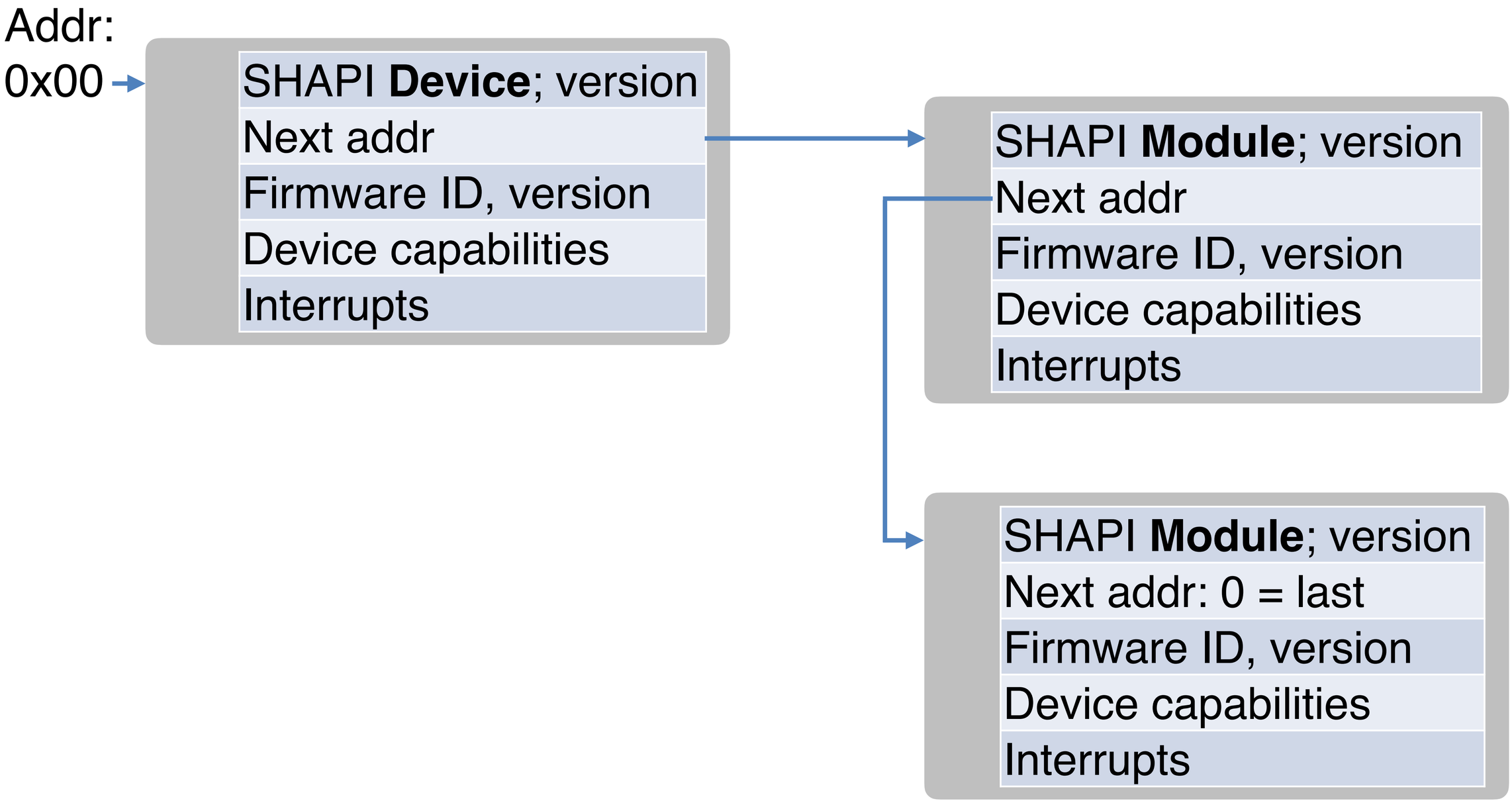
µTCA®

https://www.picmg.org/wp-content/uploads/PICMG_MTCA_DG_1-Standard_Hardware_API_Design_Guide_RELEASED-2017-01-09-002.pdf

SHAPI

- Self-describing communication: CPU <-> FPGA
  - Decoupling of application programs from FPGA code
  - No address mapping file required
  - Re-usable FPGA and application modules
- One **Device** header describes the FPGA and board hardware
  - Provides the main interrupt registers (vectored interrupt preferred)
  - Links to the first module of the FPGA
- **Module** headers are describing the function blocks (e.g. ADCs, DACs, …)
  - A module has a standard part (ID, capabilities, …)
    and a function specific part
- DMA is implemented by a special **DMA Module**

SHAPI: FPGA Device is Composed of Module



SHAPI: Standard Device Identification

31 16	15 0	Addr	R/W
Magic = 0X5348	SHAPI Version	0x00	ro
First Module Address		0x04	ro
Hardware ID	HW Vendor ID	0x08	ro
Device FW ID	Device Vendor ID	0x0C	ro
Firmware Version		0x10	ro
Firmware Timestamp		0x14	ro
Firmware Name		0x18 0x1C 0x20	ro
Device Capabilities		0x24	ro
Device Status		0x28	ro
Device Control		0x2C	rw
Interrupt Mask		0x30	rw
Interrupt Flag		0x34	ro
Interrupt Active		0x38	ro
Scratch Registers		0x3C	rw

Standard **Device** Identification & Control

Capabilities:
- Full reset available
- Soft reset available
- Has RTM detection
- Endianness available

Status:
- Doing Full reset routine
- Doing Soft reset routine
- RTM present

Control:
- Do Full reset
- Do Soft reset
- Use big-endian format

SHAPI: Device Interrupt Registers

31 16	15 0	Addr	R/W
Magic = 0X5348	SHAPI Version	0x00	ro
First Module Address		0x04	ro
Hardware ID	HW Vendor ID	0x08	ro
Device FW ID	Device Vendor ID	0x0C	ro
Firmware Version		0x10	ro
Firmware Timestamp		0x14	ro
Firmware Name		0x18 0x1C 0x20	ro
Device Capabilities		0x24	ro
Device Status		0x28	ro
Device Control		0x2C	rw
Interrupt Mask		0x30	rw
Interrupt Flag		0x34	ro
Interrupt Active		0x38	ro
Scratch Registers		0x3C	rw

Standard **Device** Identification & Control

Interrupt Mask:
- 32 bits
- 1 = interrupt **enabled** for the device assigned to this bit

Interrupt Flag:
- 32 bits
- 1 = interrupt was **raised**
- **Is masked**

Interrupt Active:
- 32 bits
- 1 = interrupt was **raised**
- **Is not masked**

SHAPI: Standard Module Identification

31 16	15 0	Addr	R/W
Magic = 0X534D	0x0100	0x00	ro
Next Module Address		0x04	ro
Firmware ID	Vendor ID	0x08	ro
Module Version		0x0C	ro
Module Name: std_dma		0x10, 0x14	ro
Module Capabilities		0x18	ro
Module Status		0x1C	ro
Module Control		0x20	rw
Interrupt ID		0x24	ro
Interrupt Flag Clear		0x28	rw
Interrupt Mask		0x2C	rw
Interrupt Flag		0x30	ro
Interrupt Active		0x34	ro
N Module Specific Registers		0x38 …	

Standard **Module** Identification & Control

Vendor ID:
- Can be used for plug-in modules

Firmware ID:
- Defines the the routine to handle this module, e.g. a certain ADC type

Version:
- Major (SW compatibility), minor, patch

Capabilities, Status, Control:
- Full or soft reset (available, status, ctrl)
- RTM required
- Single or multiple interrupts

Interrupts:
- ID: defines which device level interrupts can be raised by this module (one bit)
- Clear, Mask, Flag, Active:
  to reset, enable, IRQ & Mask, IRQ

SHAPI: DMA Standard Module

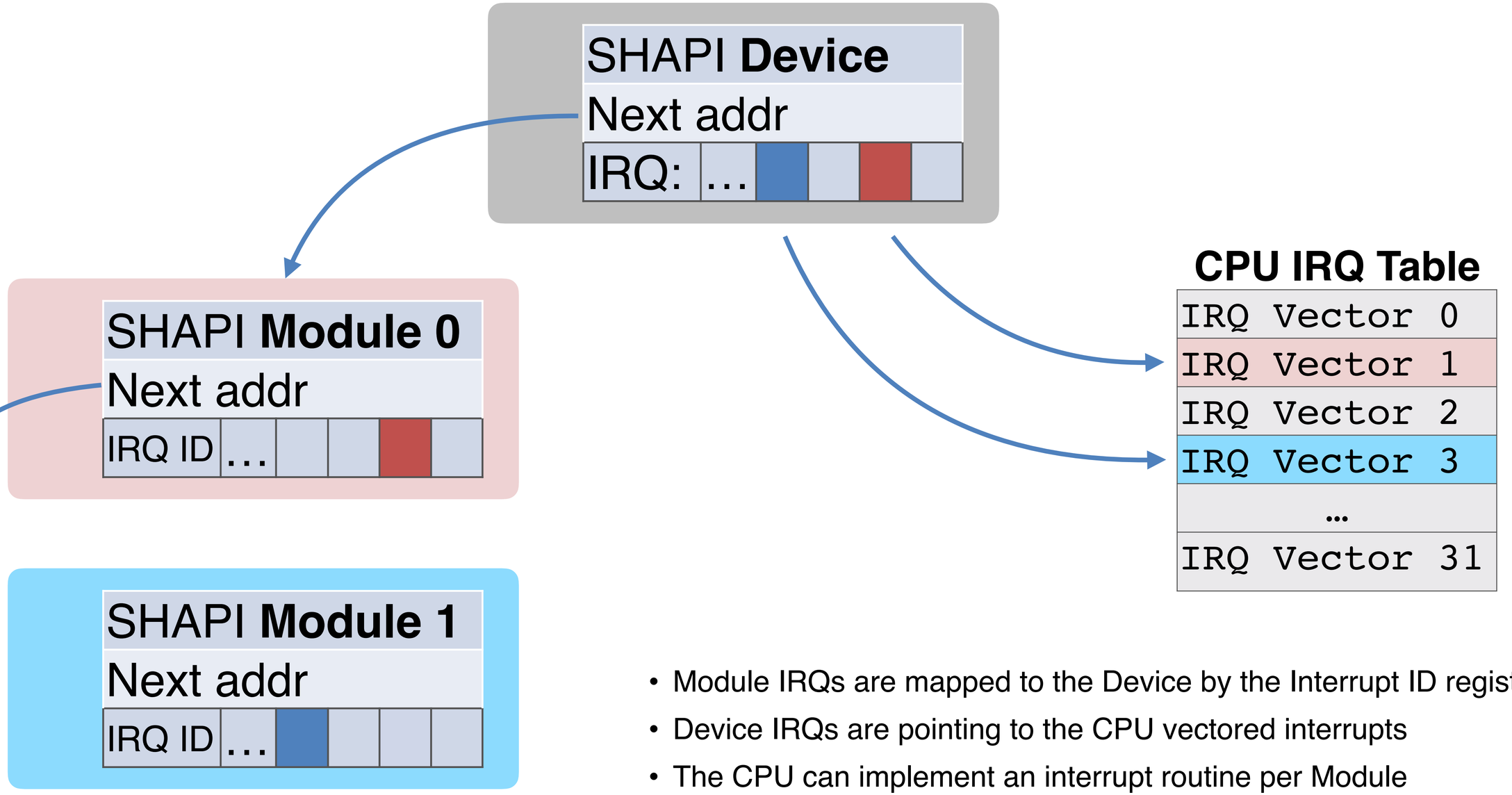
31 16	15 0	Addr	R/W
0X534D	0x0100	0x00	ro
Next Module Address		0x04	ro
Firmware ID = 1	Vendor ID = 0	0x08	ro
Module Version		0x0C	ro
Module Name: std_dma		0x10, 0x14	ro
Module Capabilities		0x18	ro
Module Status		0x1C	ro
Module Control		0x20	rw
Interrupt ID		0x24	ro
Interrupt Flag Clear		0x28	rw
Interrupt Mask		0x2C	rw
Interrupt Flag		0x30	ro
Interrupt Active		0x34	ro
DMA Capabilities		0x38	ro
DMA Status		0x3C	ro
DMA Control		0x40	rw
From Device Destination		0x44, 0x48	rw
From Device Source		0x4C, 0x50	rw
From Device Data Size		0x54	rw
From Device Data Transmitted		0x58	ro
To Device Destination		0x5C, 0x60	rw
To Device Source		0x64,0x68	rw
To Device Data Size		0x6C	rw
To Device Data Transmitted		0x70	ro

Vendor ID = 0
Firmware ID = 1
Defines a DMA Module

DMA Capabilities:
- Simultaneous read/write transfer
- RTM required
- Single or multiple interrupts
- To device DMA supported
- From device DMA supported
- Endianness data swap supported

DMA:
- Destination Address (e.g. CPU)
- Source Address (e.g. board memory)
- Requested bytes to be transferred
- Bytes transferred in last DMA

SHAPI: Interrupts



- Module IRQs are mapped to the Device by the Interrupt ID register
- Device IRQs are pointing to the CPU vectored interrupts
- The CPU can implement an interrupt routine per Module

SHAPI & Linux Driver Repository

- GitHub as an open repository to exchange MicroTCA code
  - Linux driver: hot-swap and universal
  - SHAPI driver coming soon
  - SHAPI FPGA test project coming soon

https://github.com/MicroTCA