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Design and development of the DAQ and Timing Hub for CMS Phase-2

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The CMS Detector will undergo a major upgrade for the Phase-2 of the LHC physics program, which will start around 2026. The detector will be read out at a rate of 750 kHz by some 50k high-speed optical links, for an average event size of 7.5 MB. In the baseline architecture for the Phase-2 DAQ, the optical links from detector front-ends are aggregated in detector-dependent ATCA based back-end boards.
A DAQ and Timing Hub (DTH) aggregates data streams from multiple back-end boards over point-to-point links. The DTH combines these streams to feed high speed commercial 100 Gb/s optical links, forming the data-to-surface (D2S) network. It provides buffering for time decoupling and transmission using a reliable high-level protocol, such as TCP/IP. The D2S links carry the data to surface, connecting the DTH output via standard network to I/O servers for the event building. The DTH is also distributing trigger accept and timing signals, as well as trigger control codes for calibration and synchronisation to the back-end electronics, from where they are redistributed to the front-ends.
This paper presents the system level functionality and performance requirements of the DTH. The DTH will have a modular design, where a fully equipped board has a 1.2 Tb/s DAQ bandwidth. The first step of the DTH development roadmap (P1) is currently under design. The goals and design of the P1 will be described. Results from implementation on Ultrascale development kits and a custom add-on board with serial HMC memories will be presented.

Minioral

No

Description

Timing Hub

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