

# Development of MicroTCA.4 based remote DAQ system for KSTAR Tokamak

giilkwon@nfri.re.kr
Giil Kwon



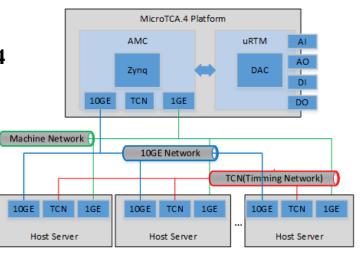
# Development of MicroTCA.4 based remote DAQ system for KSTAR Tokamak

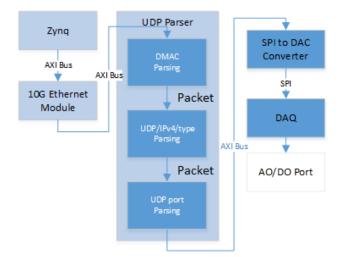


- To standardize and simplify the control system at KSTAR, we develop 10G Ethernet based remote DAQ system(SDN-Parser).
- Host and the DAQ module can be separated and multiple hosts can be connected to the DAQ module.
- This system consist of homemade case, power, MicroTCA.4 AMC(Advanced Mezzanine Cards) board and RTM(Rear Transition Module) board.









- The module takes 2.7usec to receive the input, process it, and output it.
- The system can generate
  - 8 channel AO signal at 2kHz
    - 4 channel AO signal at 5kHz
    - 1 channel AO signal at 10kHz
    - Each packet payload size is 36byte (48bytes header).
    - Each packet contain one channel signal.



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#### Development of MicroTCA.4 based remote DAQ system for KSTAR Tokamak



Control team, National Fusion Research Institute (NFRI), Daejeon, Rep. of Korea b Seedcore Ltd., Daejeon, Rep. of Korea

Abstract- To standardize and simplify the control system at Korea Superconducting Tokamak Advanced Research (KSTAR), we develop 10G Ethernet based remote DAQ system. By separating the DAQ system and the host, the structure of the control system can be made more flexible. We have developed a DAQ module with a 10G Ethernet interface based on a MicroTCA.4 system designed to control devices in real time on a remote server via 10GE. To connect proposed device and host, we use real time network based on UDP multicast atop 10GbE cut-through packet switching infrastructure. This system is implemented using Zynq based MicroTCA.4 board, matched RTM board that has analogue input/output interface and power supply system. By using remote DAQ system, multiple host server can subscribe the DAQ data without additional computational cost in real time. This system was or apprect to control rucing system at the lower to know the lower transfer of the lower transf

#### 1.Introduction

- To standardize and simplify the control system at Korea Superconducting Tokamak Advanced Research (KSTAR), we develop 10G Ethernet based remote DAQ system(SDN-Parser).
- Some KSTAR devices require only a small number of highspeed(>1kHz) AI channels and AO channels (Such as Fueling system, Neutral Beam Injection system).
- The use of DAQ equipment with MicroTCA4 crates in such equipment is not suitable in terms of cost or complexity.
- By separating the DAQ system and the host, the structure of the control system can be made Figl. Basic Concept and Architecture of System
- more flexible. - Host and the DAO module can be separated and multiple hosts can be connected
- To connect proposed device and host, we use ITER Synchronized Data Network(SD)

#### 3. FPGA Logic Design

- This module parse UDP packet from 10GE module and transmit this data to D Q module to generate analogue output.
  - Currently, Logics for AI/DI module i





Computer

SDN

PARSER

Oscilloscope

SDN Packe

AO signa

#### 4. Software for Real Time System

5. Experiment

- Host server uses Tool for Advanced Control (TAC) engine to implement real time application that control the SDN-Parser by publishing SDN packet.
  - A new TAC engine was based on C++ standard run on Linux.
  - It is a multithreaded core engine program for execution of real time application.

#### 2. Hardware Design

- This system consist of homemade case, power, MicroTCA.4 AMC(Advance Mezzanine Cards) board and RTM(Rear Transition Module) board.
- This system is implemented using Zynq based MicroTCA.4 AMC board, matche RTM board that has analogue input/output interface and pan less power suppl
  - AMC: KSTAR Multifunction Control Unit(KMCU, KZ30) is a Zynq based AM board that was developed from KSTAR.

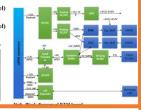


- AI: 2 channels ADC (18bit resolution, 1MSPS/channel)

- AO · Schannels DAC
- (16bit resolution, 1MSPS/channel) DI: 8channels (TTS Input)



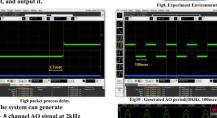
Conclusions



· To calculate latency of SDN-Parser, we construct the

SDN-Parser get packet from computer via 10GE. When SDN-Parser get packet, the module emits DO signal to Oscilloscope

- After parsing the packet from computer, the module generate AO signal
- We compare these two signal time to calculate latency
- The module takes 2.7usec to receive the input, process
- it, and output it.



- The system can generate
- 4 channel AO signal at 5kHz 1 channel AO signal at 10kHz
- Each packet payload size is 36byte
- (48bytes header). Each packet contain one channel signal.
- We will do more test with multi host server.
- We will change the packet to have more Fig11 Captured 4 waves that generated from SDN-P see

- We has develop 10G Ethernet based remote DAQ system(SDN-Par er) to standardize and simplify the control system at KSTAR. This system consist of homemade case, power, MicroTCA.4 AMC to and DTM ho
- · The FPGA module parse UDP packet from 10GE module and transmit this data to DAQ module to generate analogue output.
- · SDN Parser process delay is 2.6usec. and it can generate 8 channel AO signal at 2kHz(1 channel 10kHz). · We will do more test with multi host server.

#### 국가핵융합연구소

## H/W Design

### Experiment Result



Introduction

H/W Design