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## Application of FPGA Acceleration in ADC Performance Calibration

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In recent years, high speed and high resolution analog-to-digital converter (ADC) is widely employed in many physical experiments, especially in high precision time and charge measurement. The rapid increasing amount of digitized data demands faster computing. FPGA acceleration has an attracting prospect in data process for its stream process and parallel process feature. In this paper, an ADC performance calibration application based on FPGA acceleration is described. FPGA reads the ADC digitized data stream from PC memory, process and then write processed data back to the PC memory. PCIE bus is applied to increase the data transfer speed, and floating point algorithm is applied to improve the accuracy. The test result shows that FPGA acceleration can reduce the processing time of the ADC performance calibration compared with traditional method of C-based CPU processing. This frame of PCIE-based FPGA acceleration method can be applied in analysis and simulation in the future physical experiment for large ADC array, such as CCD camera and waveform digitization readout electronics calibration.

### Minioral

Yes

### Description

ADC calibration Algo

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