
Contribution ID: **405** Type: **Oral presentation**

# Configurable and Expandable High Speed Trigger Supervisor for Imaging Data Acquisition System.

*Thursday 14 June 2018 12:00 (20 minutes)*

The FPGA based Trigger Supervisor for the JLab Imaging Data Acquisition (DAQ) system provides a high speed connection for a number of data acquisition (DAQ) instruments. An example of a DAQ instrument is the JLab Ethernet 250 MHz 16 channel Flash Analog to Digital Converter (EFADC16) which is the basis of a recently submitted JLab patent application. The Trigger Supervisor is composed of a novel arrangement of hardware and software structures to arrive at a high performance DAQ system. It can accommodate a system of a single DAQ instrument to a complex system composed of many DAQ instruments. Each individual instrument of the complex system can be located up to hundreds of feet apart. The functionality and operation of the Trigger Supervisor are both fully programmable. The DAQ system can be seamlessly expanded to accommodate more DAQ instruments as required. The cost is directly proportional to the complexity of the system.

## Minioral

No

## Description

Trigger supervisor

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**Session Classification:** Imaging and detectors