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FPGA code for the data acquisition and real-time processing prototype of the ITER Radial Neutron Camera

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Motivation

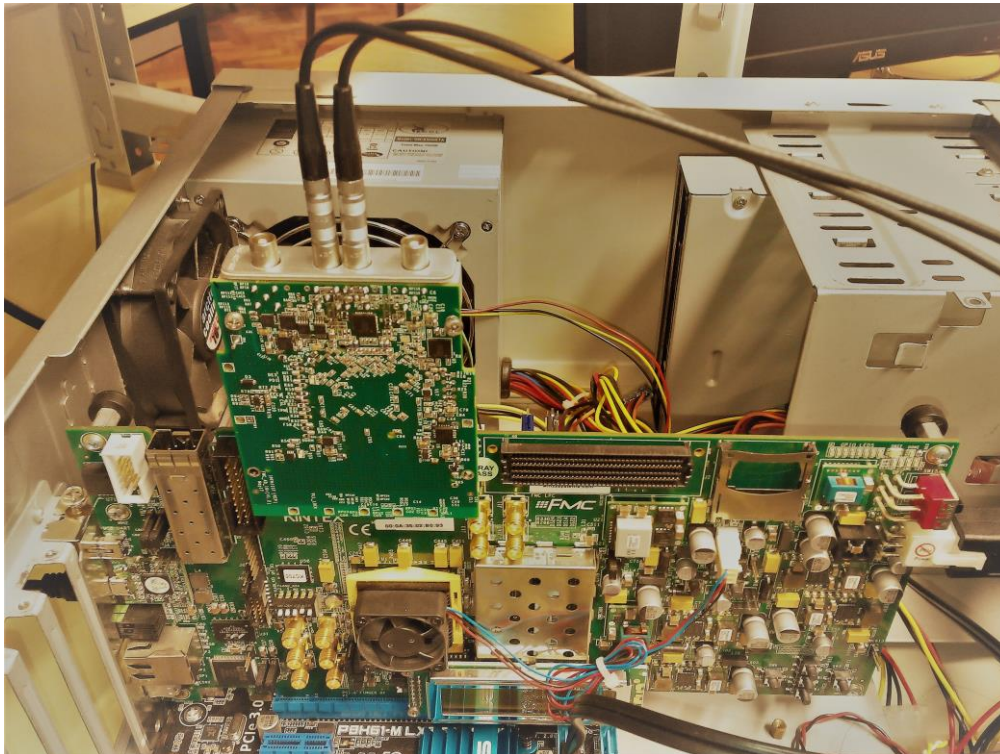
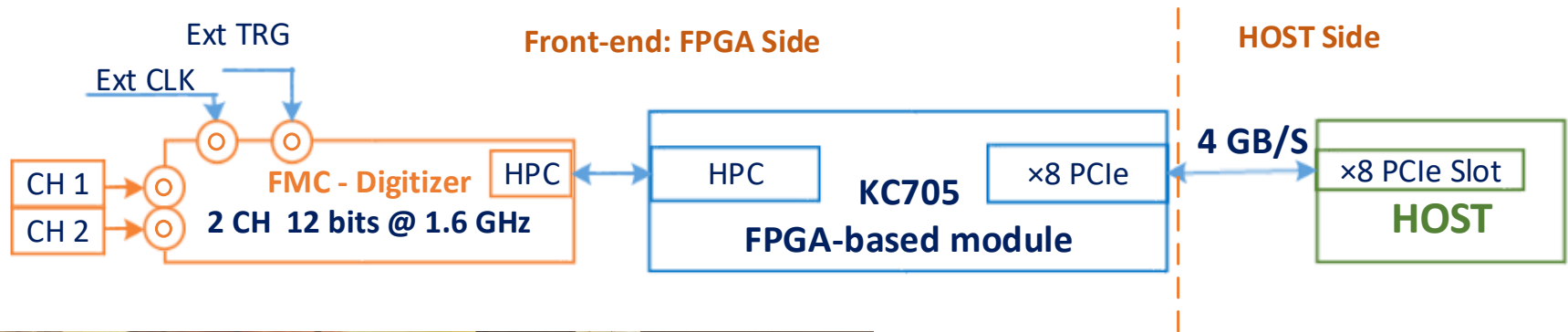
ITER Radial Neutron Camera (RNC) diagnostic main goal: measure in Real-Time (RT) the plasma neutron emissivity profile at high peak count rates for a time duration up to 500 s.

Unprecedented **high performance conditions expected** → set of **activities** selected, focused on the **development of high priority prototypes**, capable to deliver **answers** to critical issues **before the final RNC design**.

FPGA code for the front-end electronics prototype aims to **acquire, process and store in RT the neutron and gamma pulses** from the detectors located in collimated LOS viewing a plasma poloidal section.

IPFN task: design, development and testing of the common data-path and dedicated FPGA-side algorithms for RNC front end electronics prototype.

RNC Front End Electronics Prototype



Host PC:

Intel(R) Core(TM) i7-5930K CPU @ 3.50GHz;

Scientific Linux 7;

kernel: 3.10-rt

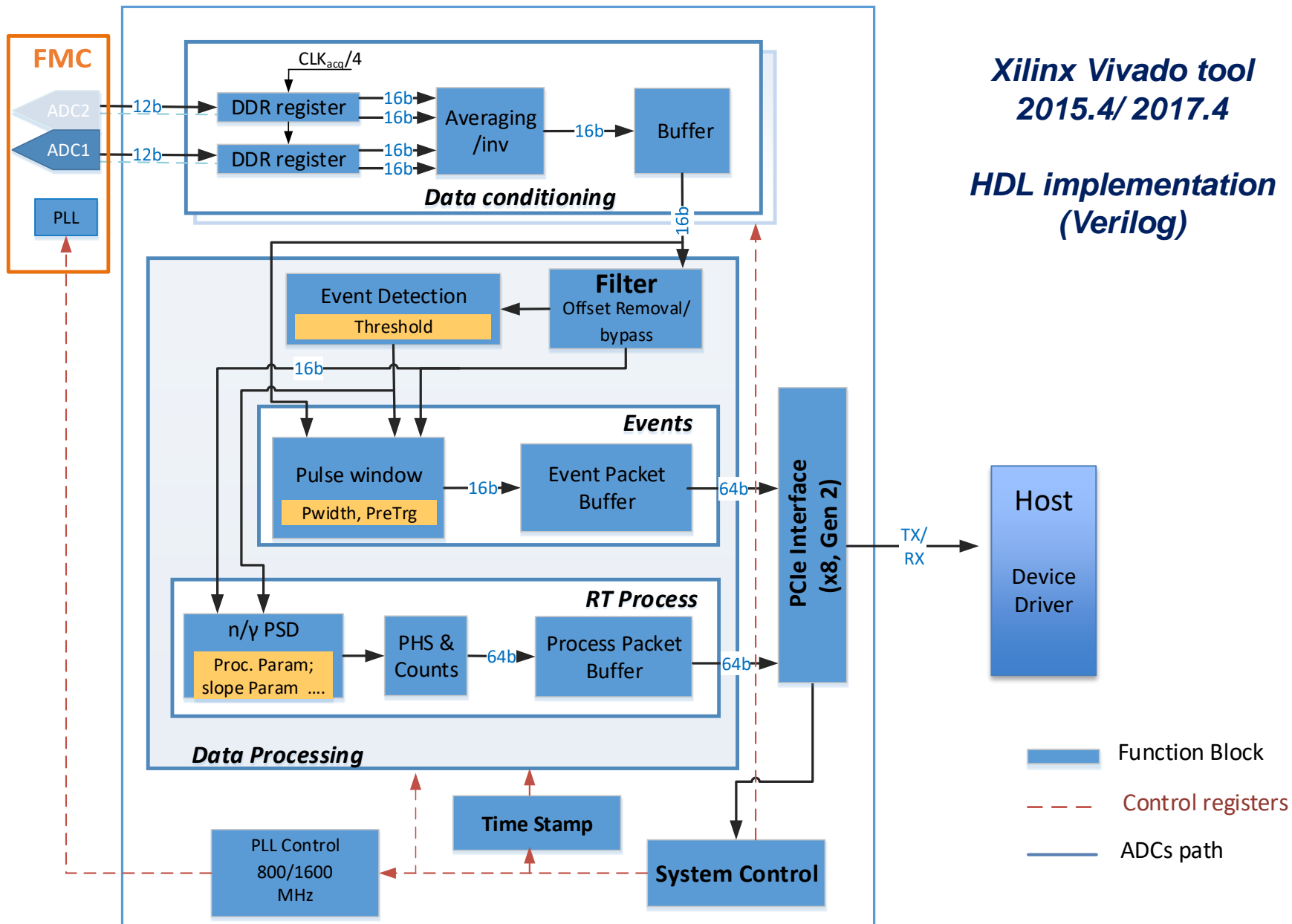
Digitizer:

Xilinx evaluation board (**KC705**);
FPGA Mezzanine Card (**FMC-AD2-1600**) with 2 digitizer channels of 12-bit resolution @ 1600 MHz.

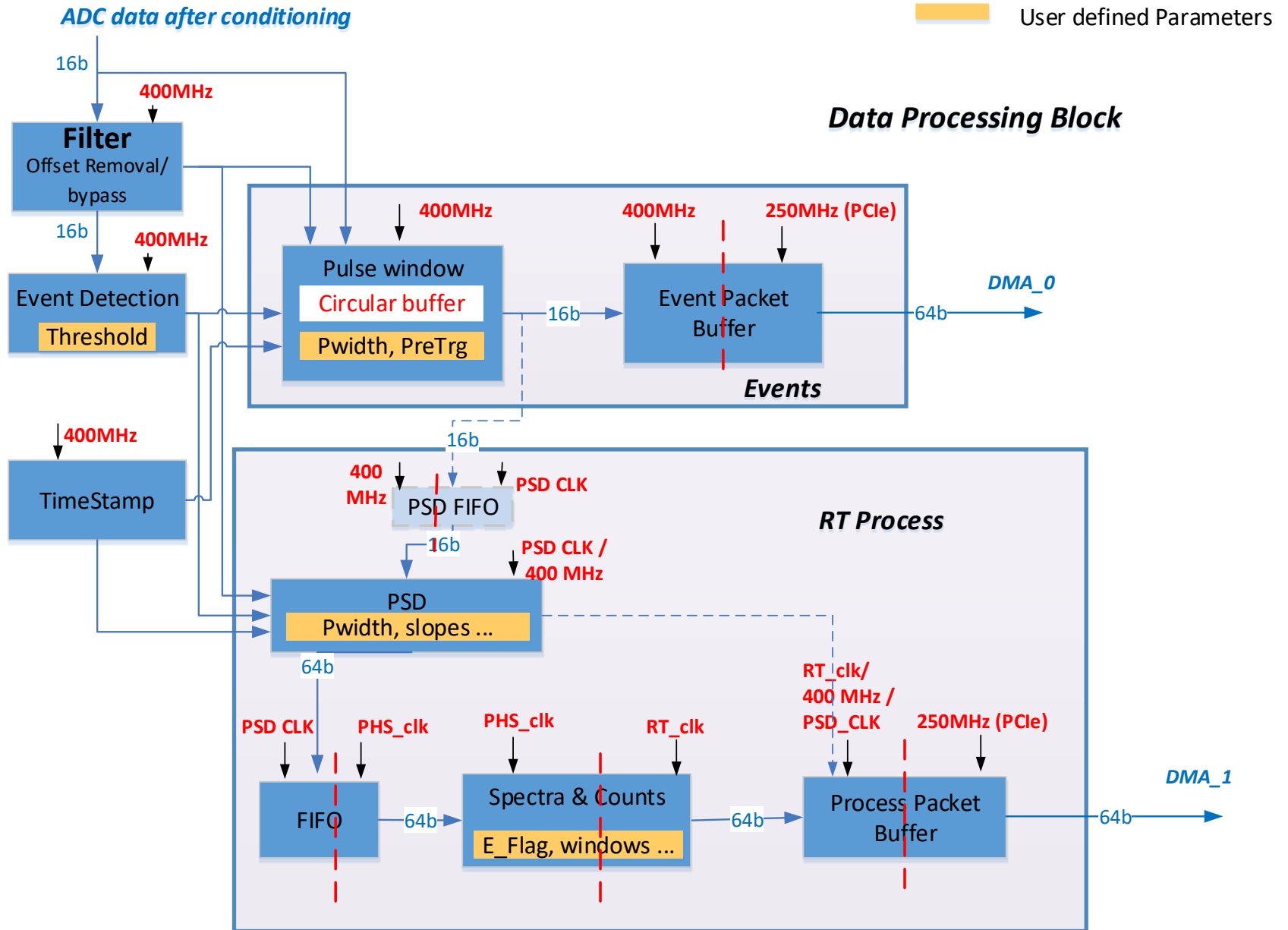
RNC FPGA CODE

*Xilinx Vivado tool
2015.4/ 2017.4*

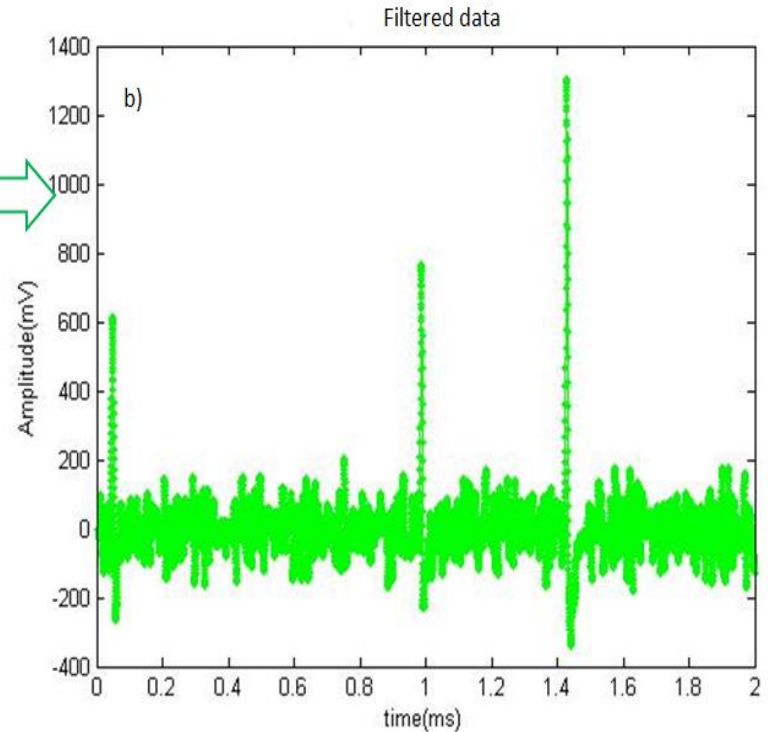
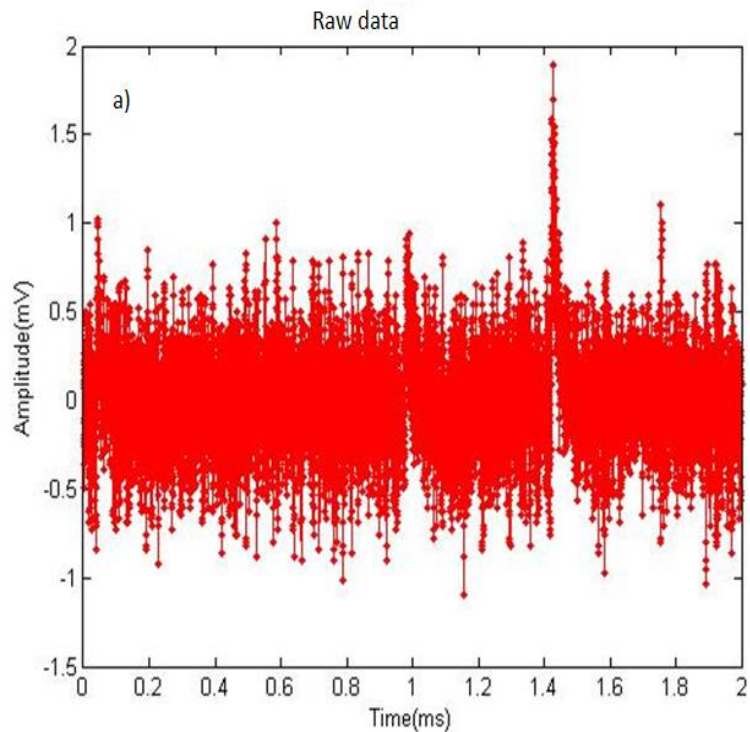
*HDL implementation
(Verilog)*



Data Processing

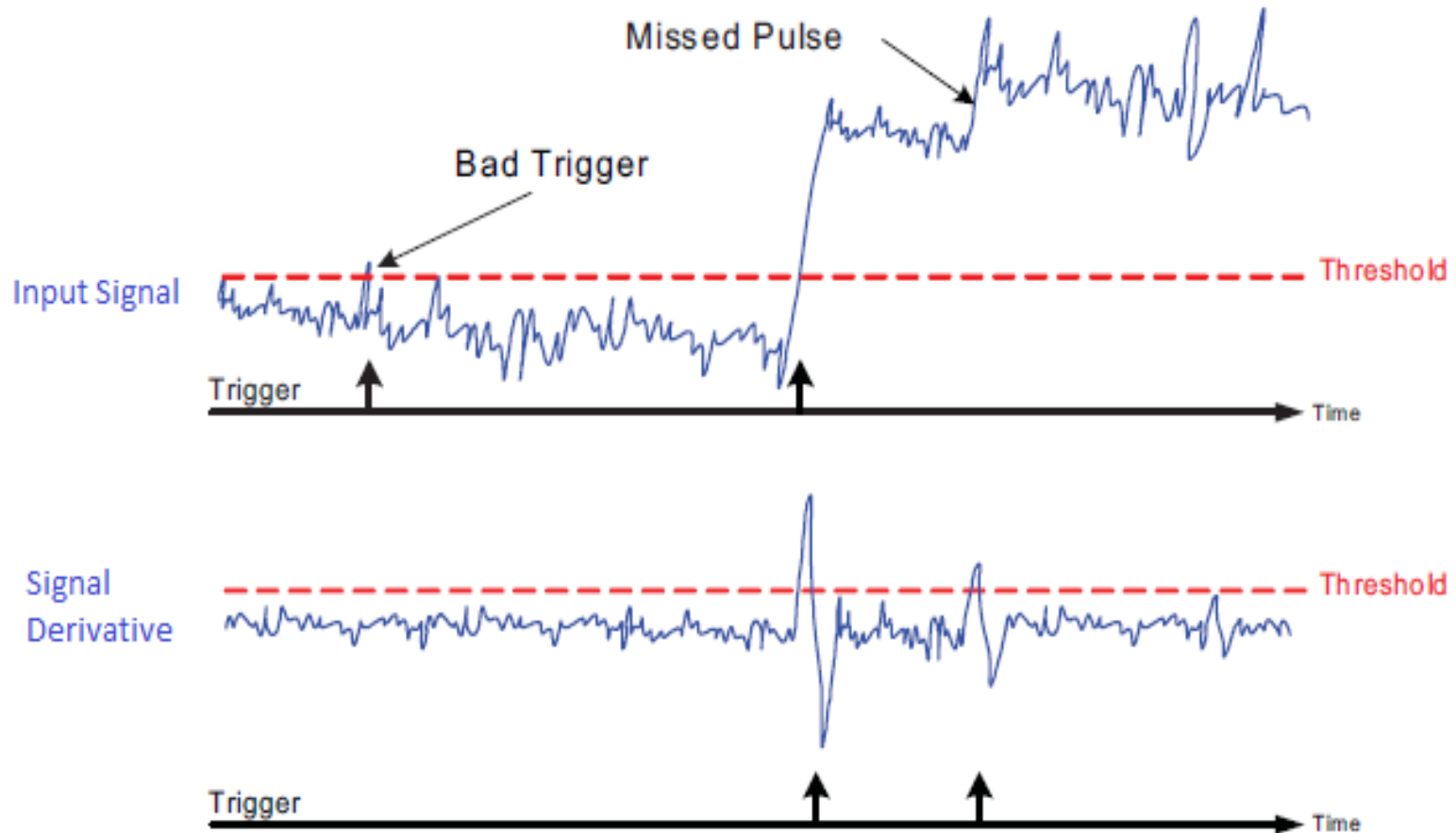


Data Processing – Filter / Bypass



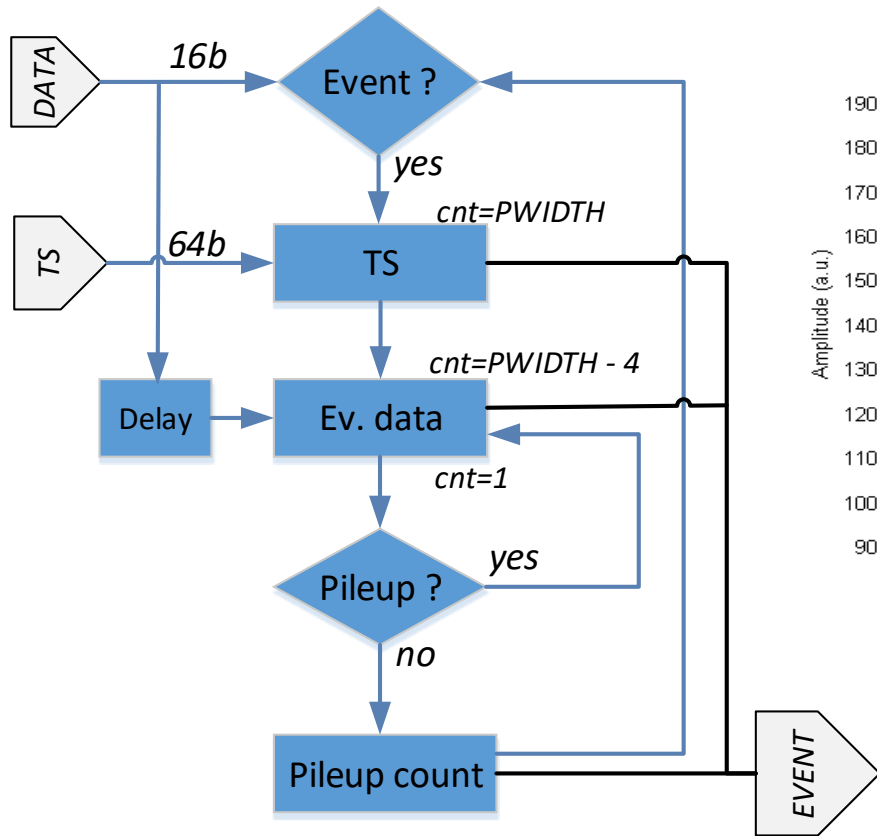
Digital Trapezoidal based Shaper (DTS) -> improvements in SNR; baseline restoring capabilities...

Data Processing – Event detection

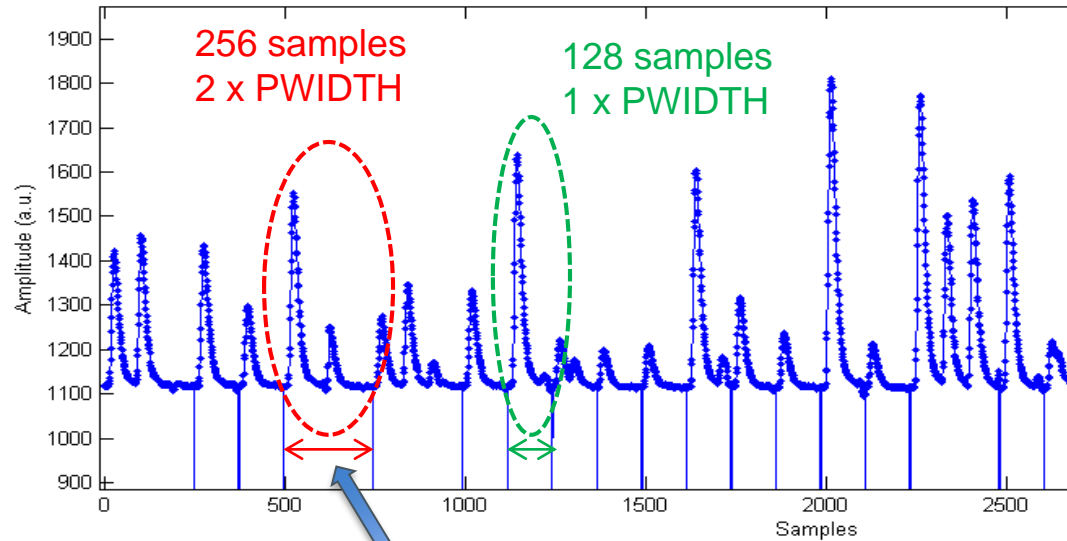


* *Digital Pulse Processing in Nuclear Physics*, CAEN, WP2081, Rev. 3, 2011

Data Processing – Events Storage (1/2)

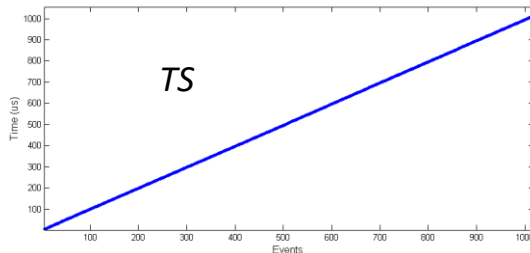


cnt – decreasing counter



Event = n x PWIDTH

Synthetic input signal with several superimposed pulses (128 samples; PTRG 16 samples; THR. Level)



RT Processing – PSD (1/2)

Implementation based on **DTS**¹:

- The FPGA n/γ **PSD code** receives data from filter module (**DTS filtered data**);
- PSD determined by the **relation factor** between the **maximum (peak) of filtered pulses** and its **integration value – charge integration (CI)**

Q - word 1 [63:0]								
63							0	
reserved		TimeStamp						
Q - word 2 [63:0]								
63	56	24	31	21	18	15	12	0
rsv	CI		rsv	PU	N/γ/L	rsv	Peak	

Other PSD methods might be feasible to implement^{2,3}

¹R.C.Pereira, Neutron/Gamma discrimination code based on trapezoidal filter, Fusion Engineering and Design (submitted)

² M. Riva, et al., Fusion Eng. Des. 86, pp. 1191–1195, 2011;

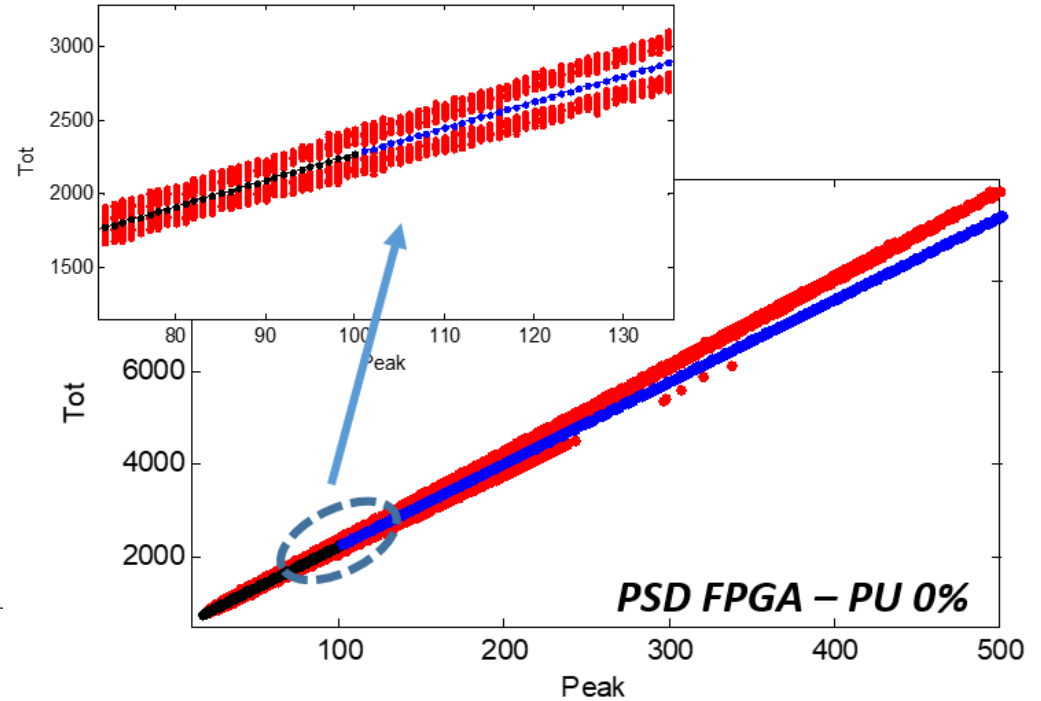
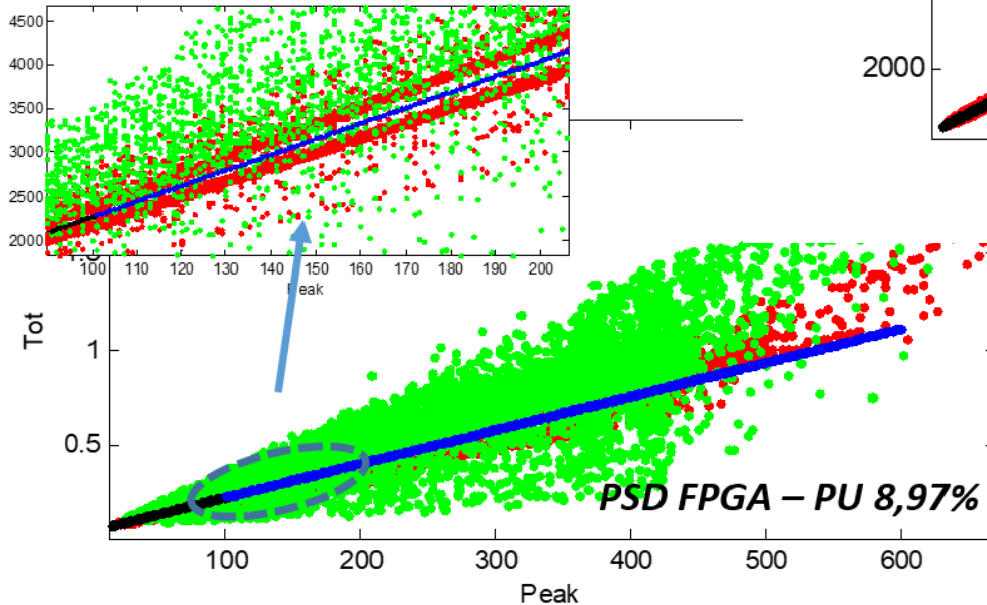
³ Vahid Esmaeili-sani, et. al., Nuclear Inst. Methods in Physics Res. A, vol 694, pp. 113-118, 2012

RT Processing – PSD (2/2)

Processed data from PSD @ FPGA

Setup:

- **Synthetic data** based on theoretical particle shape of two combined CAEN channels
- **Ch. 1 – gamma; Ch. 2 - neutron**

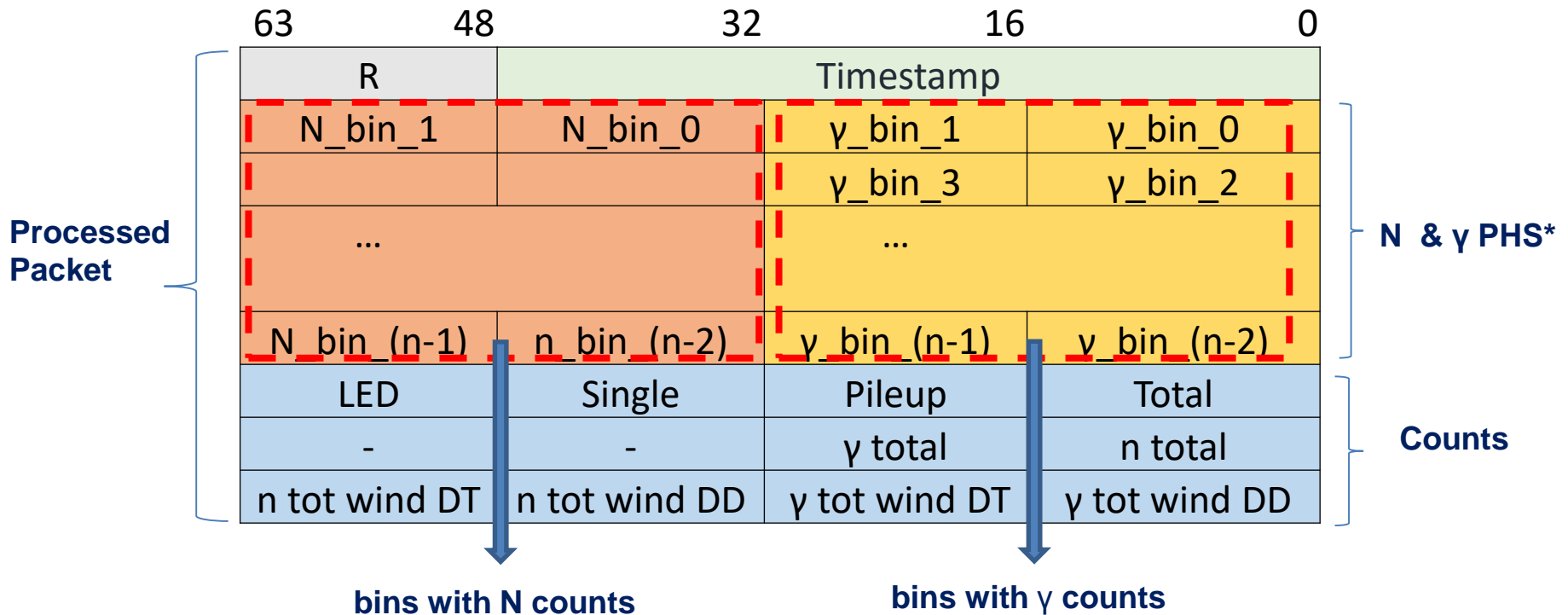


- *PU detected @ FPGA*
- *n/γ PSD from FPGA*
- *Low sep. slope*
- *High sep. slope*

Poisson distribution (~ 10 % of pileup) applied to in each channel

RT Processing – PHS (1/2)

Packet with neutron (N) & gamma (γ) Pulse Height Spectra (PHS) + Counts, to be sent periodically to host :



*n – total spectra bins***

* no-calibrated spectra

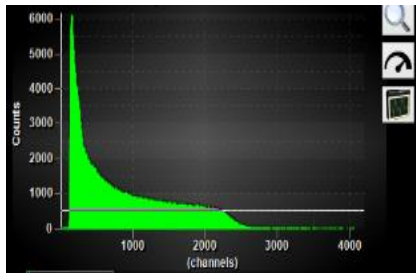
**power of 2 (512, 1024, 2048 ...)

RT Processing – PHS (2/2)

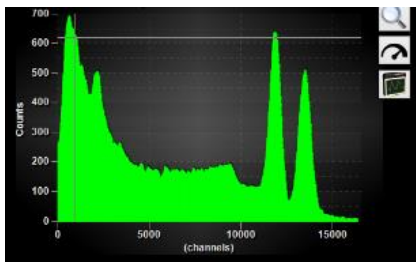
Setup:

- 100 ms acquisition of **two CAEN channels**
- **500kev/s each channel**

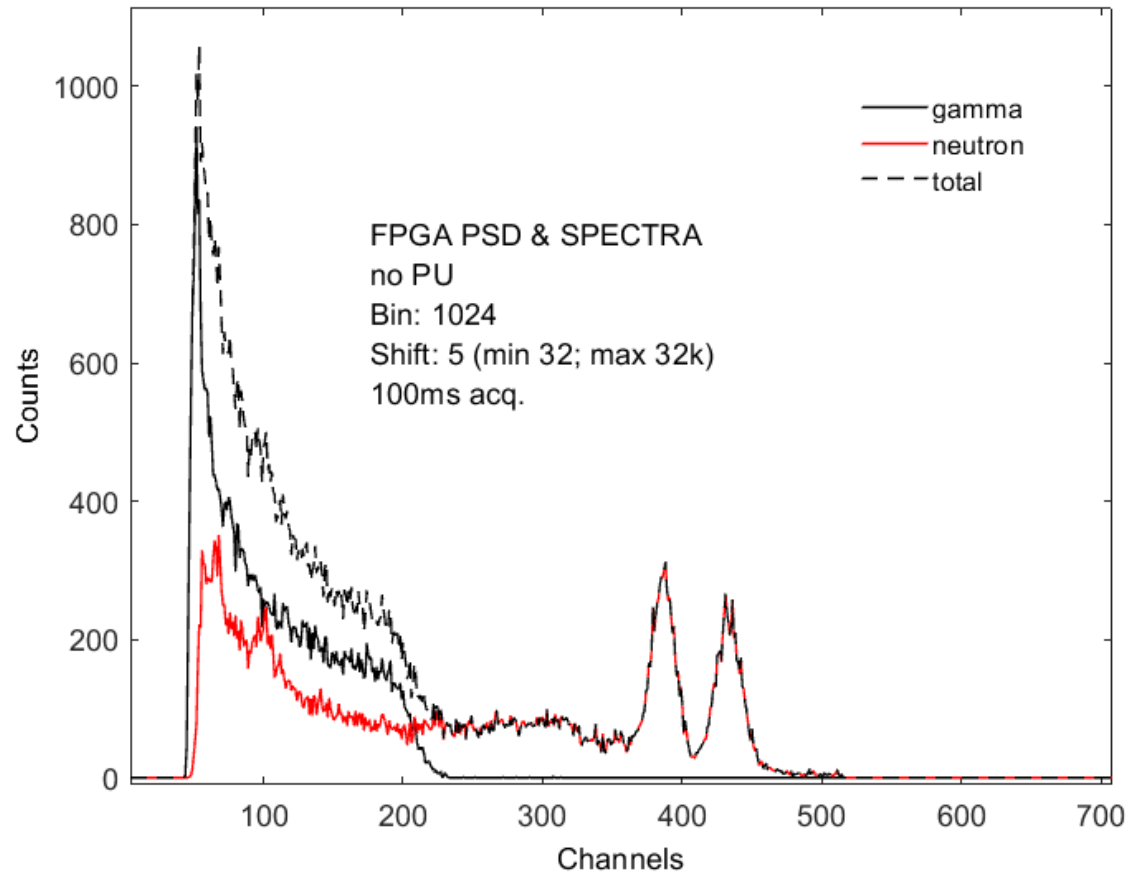
FPGA neutron/gamma PHS



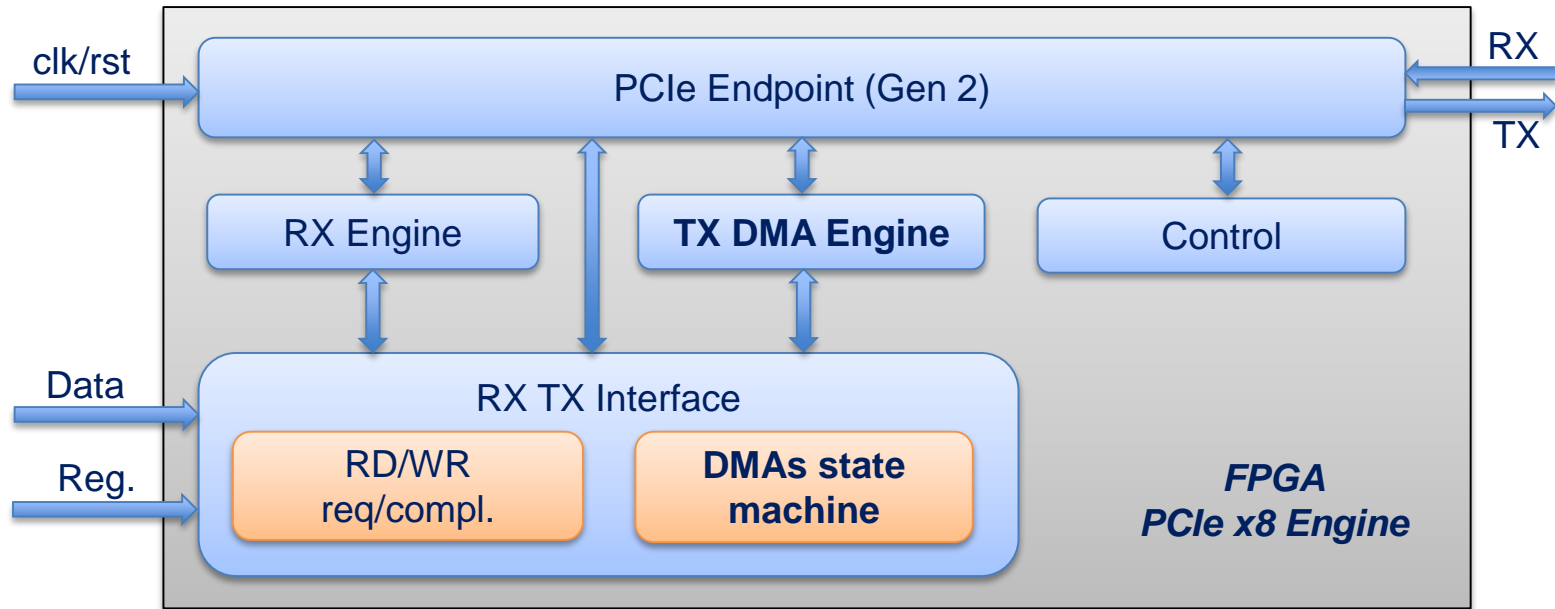
Ch1: gamma shaped pulses



Ch2: neutron shaped pulses



Data Transfer to Host

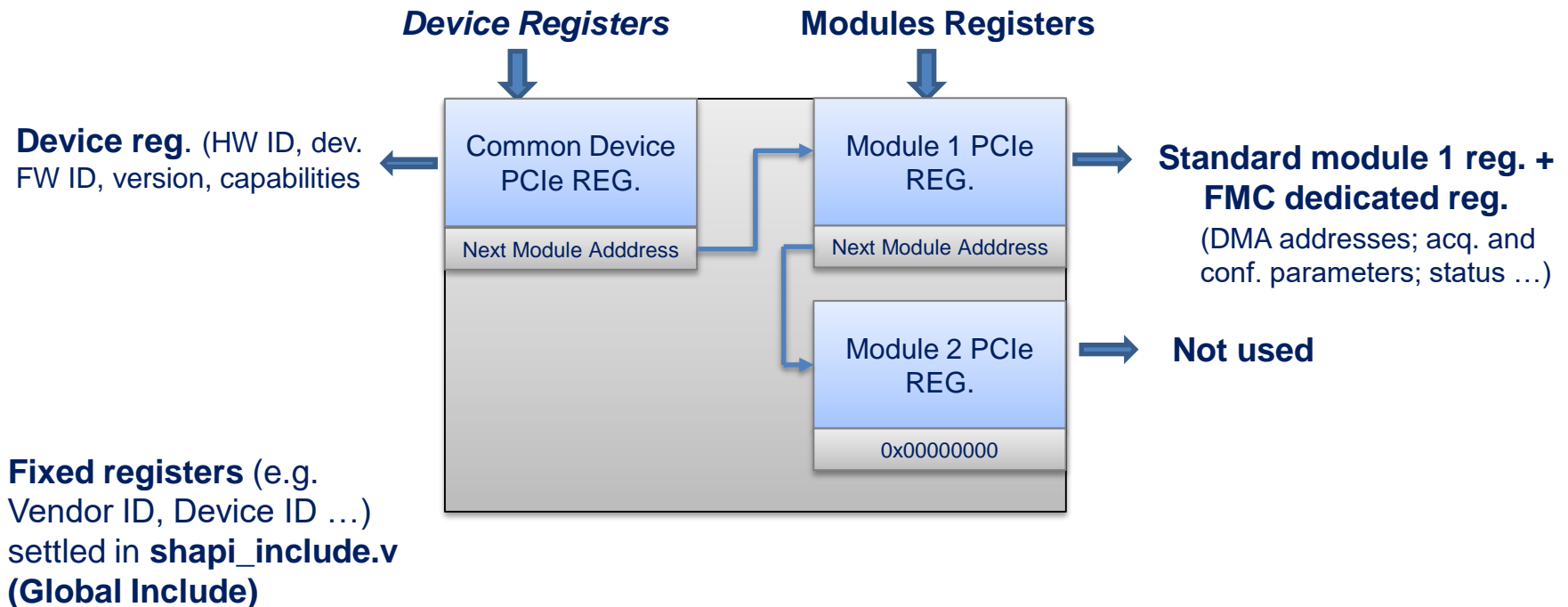


- ❑ Negotiates **data-paths between RX, TX and other FPGA** blocks;
- ❑ DMAs management and completion to requests **state machine**
- ❑ **3 DMAs** available - two DMAs for data transfer; 1 DMA for status reg.

System Control

- **Standard Hardware API (SHAPI)** – Guideline for designing hardware access APIs for xTCA systems, from PICMG® xTCA for Physics

➤ *Synchronization tasks between the board and the host done through **shared configuration registers**, located in the **host shared memory PCIe configuration space (BAR)***



Conclusions

- ✓ The Front End Electronics **FPGA code** designed and successfully implemented in the RNC prototype.

FPGA code **includes**:

- ❑ **Signal conditioning**;
- ❑ **RT processing** – filtering, event and pileup detection, event storage, PSD and PHA;
- ❑ **Data streaming** - two DMAs for real-time data streaming (event-based / PSD or PHS processed data); one DMA for status.

- ✓ Code tested with **synthetic data** in laboratory:
 - maximum throughput: **1600 MB/s** (maximum allowed for 2 channels @ 400 MHz – continuous acquisition);
 - **PSD relation factors** from FPGA able to **distinguish neutron /gamma** → further improvements for PU detection identified (overcome the DTS smoothing effect);
 - **PHS successfully tested** → might be difficult to operate in experiments with high fluctuation of the separation slopes.