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## Configuration Redundancy for Enhanced Reliability in SRAM-based FPGAs

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Digital off-detector electronics in trigger and data acquisition systems of High-Energy Physics experiments is often implemented by means of SRAM-based FPGAs, which make it possible to achieve reconfigurable, real-time processing and multi-gigabit serial data transfers. On-detector usage of such devices is mostly limited by their configuration sensitivity to radiation-induced upsets, which may alter the programmed routing paths and configurable elements.

In this work, we show a new technique for enhancing the usage of SRAM-based FPGAs also for on-detector applications. The proposed technique is capable of protecting the configuration pertaining to basic blocks such as look-up-tables and routing, but it can also address complex hard macros, such as high-speed IO transceivers (e.g. the Xilinx GTX). We show a demonstrator of our solution on benchmark designs, including a triple modular redundant design and a serial link (without redundancy) running at 5 Gbps, implemented in a Xilinx Kintex-7 FPGA.

We performed irradiation tests at Laboratori Nazionali del Sud (Catania, Italy) with a 62-MeV proton beam. The results show that our scrubbing technique made it possible to detect and correct all the radiation-induced upsets after a total fluence higher than  $10^{11} \text{ cm}^{-2}$ . For both the redundant benchmark design and the serial link, the correct functionality was always restored after scrubbing the corrupted configuration bits and re-setting the circuit. However, the redundant design has shown a significantly lower number of failures with respect to the serial link.

### Minioral

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### Description

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