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Study of Full Parallel RS(31,27) Encoder for a 3.2 Gbps Serial Transmitter in 0.18 um CMOS Technology

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A full parallel Reed Solomon encoder is developed for a 3.2 Gbps serial transmitter. The code structure is two interleaved RS(31,27) codes. One RS(31,27) code has 135 information bits and 20 redundancy bits. A frame has the information rate of 0.844 and provides the capability of correcting 20 bits consecutive errors. Two encoder modules work in parallel and send the encoded data to an interleave module. We tried the regular serial structure and a novel parallel structure to develop the RS encoder. The regular serial structure has a data output width of 5 bits, so it needs a 320 MHz clock to achieve the 3.2 Gbps speed requirement. The parallel structure requires acceptable more area, but only a 10 MHz clock is needed. The 3.2 Gbps serial transmitter is used for a CMOS monolithic active sensor application. This transmitter has been verified in 0.18 um CMOS Technology. A matched RS decoder is implemented on a Xilinx Kintex-7 FPGA board.

Minioral

No

Description

Data encoding

Speaker

Guangyu Zhang

Institute

USTC

Country

China

Author: ZHANG, Guangyu (University of Science and Technology of China)

Co-authors: GONG, Datao (Southern Methodist University (US)); YANG, Dongxu (University of Science and Technology of China); WANG, Jian (Univ. of Sci. & Tech. of China); Dr SUN, Quan (Southern Methodist University); LIU, Tiankuan (Southern Methodist University (US))

Presenter: ZHANG, Guangyu (University of Science and Technology of China)

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