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# I2C management based on IPbus

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CBM (Compressed Baryonic Matter) is mainly used to study QCD phase diagram of strong interactions in high and moderate temperature region. Before the next generation GBTx based CBM DAQ system is built up, the DPB (Data Processing Board) layer is used in data readout and data pre-processing, where a general FPGA FMC carrier board named AFCK is used. This paper mainly describes the management of the Inter-integrated Circuit (I2C) devices on AFCK and the FMCs it carries via IPBus, an FPGA-based slow control bus used in CBM DAQ system.

On AFCK, the connection of IPBus depends on the correct initialization of a set of I2C devices, including the I2C-bus multiplexer (choosing correct I2C bus), the clock crosspoint switch (providing the 125MHz needed by 1000BASE-X/SGMII), the serial EEPROM with a EUI-48 address (providing the AFCK MAC address). An independent initial module can execute an I2C command sequence stored in a ROM, through which the FPGA can write to/read from the I2C devices without IPBus, so that the related I2C devices are correctly initialized and the necessary preparation for the IPBus start-up is fulfilled. After the initialization, a Wishbone I2C master core is used as an IPbus slave and all other I2C devices can be configured directly via IPBus. All the design has been fully tested in the CBM DPB design.

## Minioral

Yes

## Description

IPBus

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