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New version of High Performance Compute Node for PANDA TDAQ system

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PANDA is a general purpose hadron spectrum to be installed in the high energy storage ring of the Future Anti-proton and Ion Research facility-FAIR, in Germany. Physics simulation shows that the event rate for PANDA experiment is about 20MHz, and event size from 1.5KByte to 4.5KByte per event. Considering background, the relative data rate to the TDAQ system will be as high as 200 GByte per second. xTCA frame will be appropriate scheme for PANDA TDAQ system.
New version of High Performance Compute Node is the key module for PANDA TDAQ system. Xilinx Ultrascale FPGA is used for data parallel processing. RocketIO hard core in FPGA used for high speed data transmission. DDR4 is used for mass data buffering. 10 Gigabit Ethernet is designed for data output. Gigabit Ethernet Switch is designed for AMC cards Ethernet port, ATCA Ethernet Switch, RTM Ethernet port switching, which can be used as slow control channel. Backplane of ATCA board is designed as full mesh topology for data sharing between every compute node. IPMC/MMC platform is designed following xTCA specification. New version Compute Node is finished. Latest testing result will be shown in the meeting.

Description

HP DAQ

Minioral

Yes

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