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A readout method based on 10 gigabit Ethernet for silicon pixel detector

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With the rapid development of network protocol, TCP/IP has been widely applied in various OS systems because of its advantages of high-speed network transmission and standardization. Furthermore, TCP/IP has the functions of retransmission and flow control, so it can ensure data's security and stability. In recent years, as a transmission Field-bus, it is also widely used in high-energy physics detector. This article describes a readout method using 10 gigabit network processor applied in silicon pixel detector which is a pixel detector designed for the High Energy Photon Source (HEPS) in China. The PHY layer and the MAC layer of this hardware are both instantiated in FPGA. The logic of hardware can process and read out the data of the detector, meanwhile, it wraps up data and send them to TOE (TCP Offload Engine). A kind of bus control protocol interface is also provided, which can facilitate the host computer to read and write the specific register directly through the UDP protocol. Only a piece of FPGA can complete the processing of the TCP and UDP packets. It is important for the miniaturization of the detector.

Minioral

Yes

Description

10G readout

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