Contribution ID: **436** Type: **Poster presentation**

A Design of FPGA Based Small Animal PET Real Time Digital Signal Processing and Correction Logic

Thursday 14 June 2018 15:50 (15 minutes)

Small animal positron emission tomography (PET) is a high sensitivity and resolution PET device for small animal imaging. Flexibility, high efficiency, high precision charge measurement and position calculation are major demands of a practical PET system which asks for a high-quality analog front end and a digital signal processing module. To achieve higher efficiency and compatibility of multiple data processing modes, we design the real time digital signal processing logic of the small animal PET system, which implements 32-channel signal processing in a single Xilinx Artix-7 family of FPGA and integrates several functions, including 2D raw position calculation, crystal identification, events energy filtering, flood map and energy spectrum real time histogram, etc. A technical design of the Crystal Look-up Table (CLT) is applied here to reduce logic consumption in order to achieve the high integration and the simplification of the logic design. Besides, a series of on-line corrections are also integrated for higher resolution, such as, timing-energy correction, energy calibration to 511 keV photon peak with crystal granularity, timing offset correction with crystal granularity, etc. The pipe-line logic processes the signals at 125 MHz with a 1,000,000 events/s rate. To evaluate the performance of the logic, a series of initial testing are conducted. The results indicate that the logic achieves the expectations.

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Yes

Description

DSP

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Session Classification: Poster 2

Track Classification: Real Time System Architectures and Intelligent Signal Processing