Contribution ID: **583** Type: **Poster presentation**

An FPGA-Driven Signal Generator for the Barrier Bucket System at COSY

Thursday 14 June 2018 15:50 (15 minutes)

At the Cooler Synchrotron (COSY) in Juelich a barrier bucket RF system is used to manipulate the proton beam. Such a system can compensate the energy loss in the target and allows for a mostly constant intensity most of the time. The barrier bucket signal is a short pulse like a single sine period.
To provide this signal we developed a signal generator based on a XILINX ZC706 evaluation board.

The internal ARM processor is used for the communication over ethernet. Four wave forms are stored in memory tables with a width of twelve bit and a size of 256 words each. The selected table is read out synchronously with the revolution of the COSY beam. A 16 bit parallel input provides an additional amplitude information. The memory words and this amplitude are multiplied and then fed to an attached DAC to generate the analog signal.

The challenge was the variable frequency. The revolution frequency of COSY changes from about 0.4 MHz to about 1.6 MHz. With 256 data points per resolution the DAC is fed with a frequency in the range of 115 to 404 MHz.
Our understanding was always that the core frequency of an FPGA has to be constant and that PLLs follow frequency changes only slowly.
But we showed that we can increase the frequency from 128 MHz to 400 MHz within 200 ms without the internal PLL of the FPGA losing its lock.

Minioral

Yes

Description

FPGA

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Session Classification: Poster 2

Track Classification: Real Time System Architectures and Intelligent Signal Processing