

### A PXI-based, Multi-channel Ultra-fast Data Acquisition System for Transient Pulsed Signal



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#### 1. Overview

This work presents a high speed, high resolution data acquisition system(DAS) with 1Gsps sampling rate and 12 bit resolution, mainly applying to nuclear and particle physics experiments. The system consists of one NI PXIe-1085 chassis, containing a PXIe controller card and 16 data acquisition cards at most. For every single card, the signal conditioning module incorporates one high precision Op Amps converting single-ended signals to differential signals(LVDS) with low additional noise level, and the data acquisition module combines a 12-bit folding interpolating ADC with a Xilinx Kintex-7 FPGA, implementing controls of A/D conversion and high speed data transmission through SFP interface using Aurora protocol. All these cards in the chassis can be synchronized easily using timing and triggering with PXI resources. Besides, a simple software of our system is designed to display the captured waveform signal and communicate with the host PC for remote controlling.

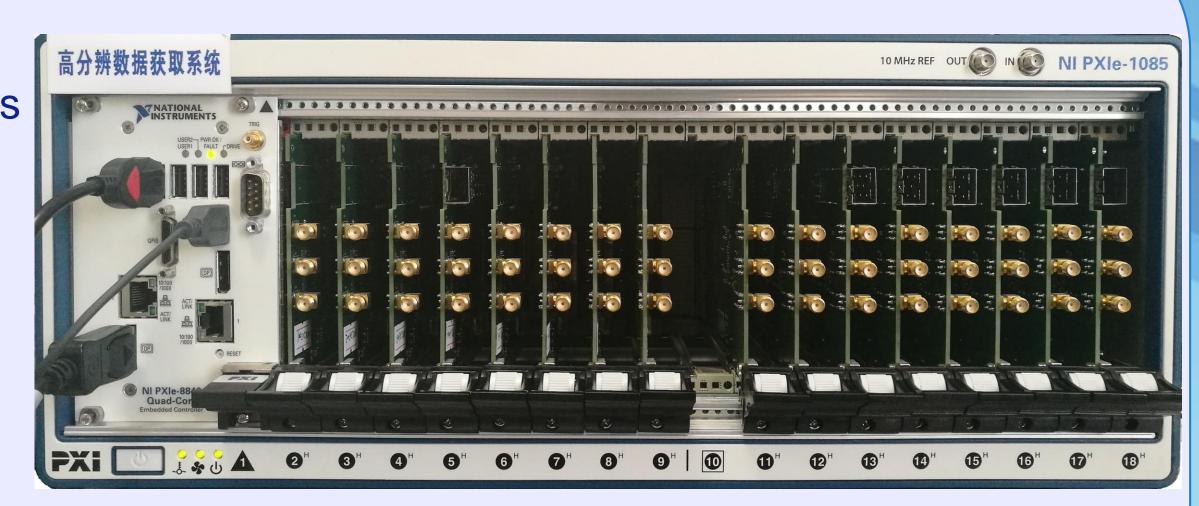


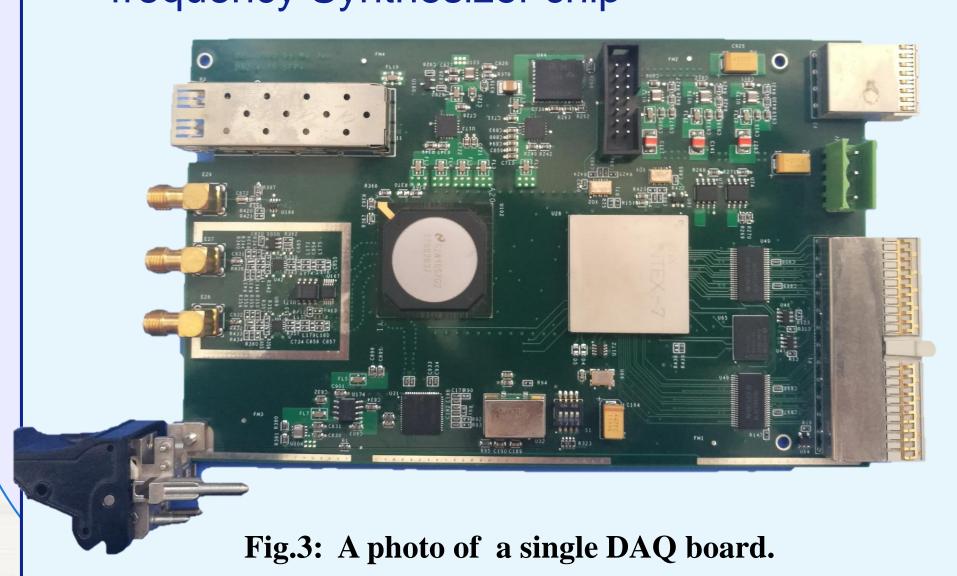
Fig.1: A photo of the PXI-based, Multi-channel Ultra-fast DAS for Transient Pulsed Signal. (Note: The NI PXIe-1085 18-slot chassis features a high-bandwidth, all-hybrid backplane to meet a wide range of high-performance test.)

#### Hardware Design

# Signal Chl Grid Generator Sept Interface Ext. Trig Impedance match Comparator Power Supply Chl Grid Generator Sept Interface Power Supply Power Supply

Fig.2: The block diagram of a single DAQ board.

- We deploy serval orders of input range to cover some hundreds of milli-voltages to hundreds of voltages.
- To improve SNR, a three-order Butterworth filter as anti-alias filter is used.
- A baseline shift module is designed for unipolar signals to fully display in the virtual oscilloscope.
- This design chooses TI's LMK04821 as the frequency Synthesizer chip



#### 2. Design and Test

## DI Serial-to-parallel DId Serial-to-parallel DCLK Clock/Trigger Data Processing PXI/SFP Interface DQ Serial-to-parallel DQd Serial-to-parallel Baseline Shift System Control

Logic and Software Design

Fig.4: Main Procedures in logic design with Xilinx FPGA.

- Serial-to-parallel: lower date rate per lane
- We use integrated Block RAM IP core to instantiate a module to assemble the captured data
- The resulting data can be transmitted to remote server through SFP connector with optic fibers using Aurora Protocol.
- After creating the VISA-based driver and developing basic communication and DMA support, our control software is built.

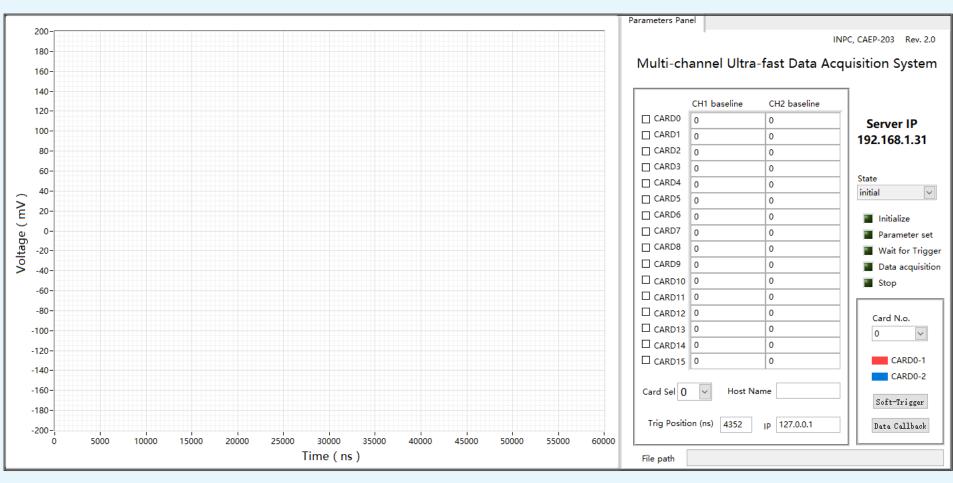


Fig.5: Interface of software designed in LabVIEW environment

#### Test Results

- Virtually oscilloscopes in a chassis.
- After calibration, primary test results show as followings

Tab.1: The primary test results of ENOB.

58.541MHz

134.337MHz

23.723MHz

**Anti-alias Filter** 

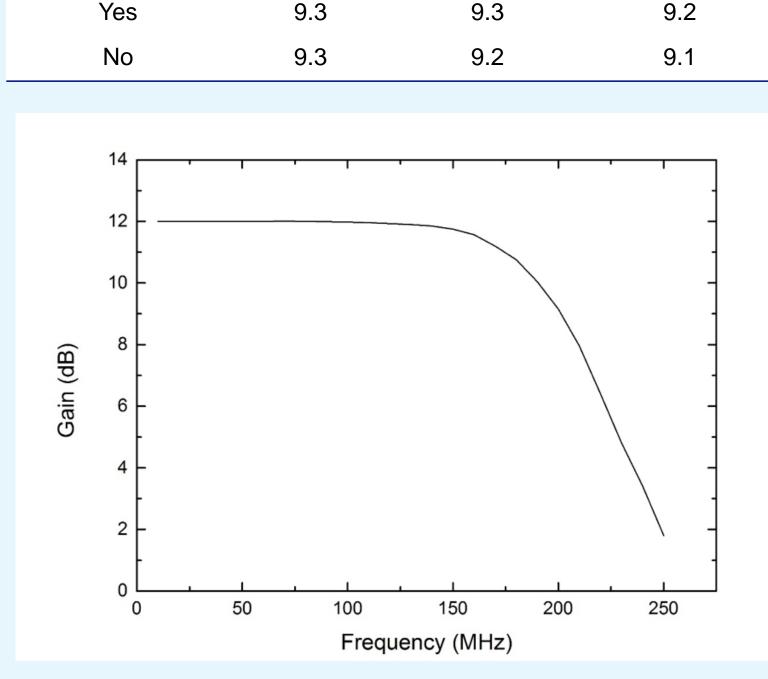


Fig.6: The typical Gain vs f plot of a single channel

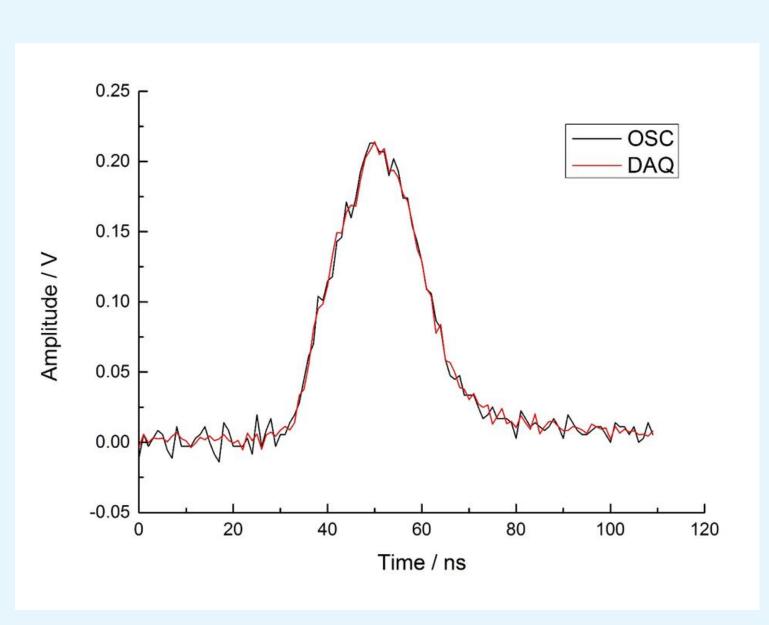


Fig.7: Typical comparison between our DAQ channel and a 12-bit 1Gsps oscilloscope channel when recording a typical transient pulsed signal.

#### 3. Summary

- ☐ The DAS can integrate 16 DAQ boards in one chassis. With great scalability, the system can be used for modern big physics experiments.
- □ Primary measurements show that the each single card in our DAS achieves an analog bandwidth of higher than 200MHz and an ENOB of more than 9 bit at 1Gsps sampling rate.
- □ Each channel has a memory depth of 65kS and the trigger position can be programmable through software interface.
- ☐ The digitized data can be either transferred through PXI 32bit/33MHz bus to the disk of the local controller or through SFP interface to the remote receiver within 1ms.
- ☐ Qualitatively speaking, more research work should be done with record and test of single transient pulsed signals.