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A 3.8ps RMS time synchronization implemented in a 20 nm FPGA

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A 3.8ps RMS time synchronization implemented in a 20nm fabrication process ultrascale kintex Field Programmable Gate Array (FPGA) is presented. The multi-channel high-speed serial transceivers (e.g., GTH) play a key role in a wide range of applications, such as the quantum key distribution systems. However, owing to the independent clock divider between the serial data clock and the parallel data clock in each GTH channel, the random skew would appear among the multi channels every time the system powers up or resets. Although the FPGA provides a phase alignment method itself, the observed jitter of ˜100ps is far from meeting the demands of extreme precision in many areas. To compensate this skew, a protocol combined of a high-precision time-to-digital converter (TDC) and a tunable phase interpolator (PI) is presented. The TDC based on the carry8 primitive is applied to measure the phase difference of each parallel clock with a bin size of ˜11ps. The embedded tunable PI in each GTH channel has a step precision of ˜3.5ps bin size and ˜0.7ps root mean square (RMS). The final time synchronization of multi channels features a RMS of ˜3.8ps, much better than the prior FPGA phase alignment method. Besides, a desirable time offset of every channel can be implemented with a closed-loop control.

Minioral

Yes

Description

time synch

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