# A *2.5 ps* RMS time synchronization for multiple high-speed transceivers in FPGA

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# Outline

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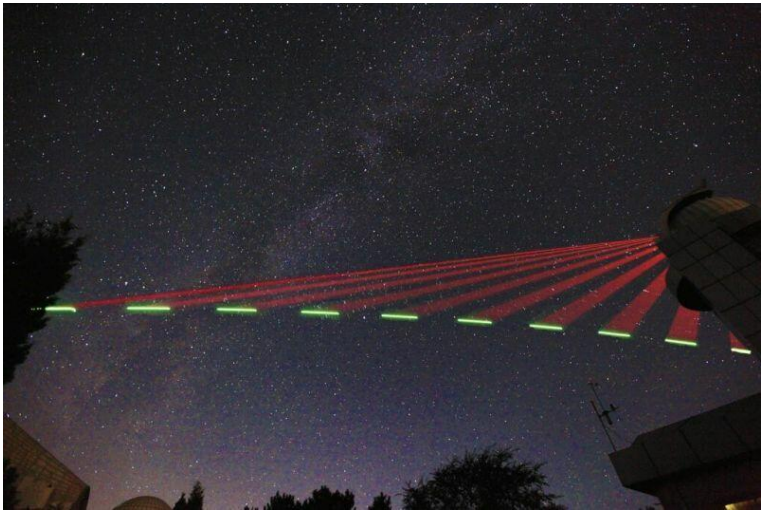
# Introduction



Quantum Key Distribution (QKD): absolute security in principle.

"mozi" satellite launching into space

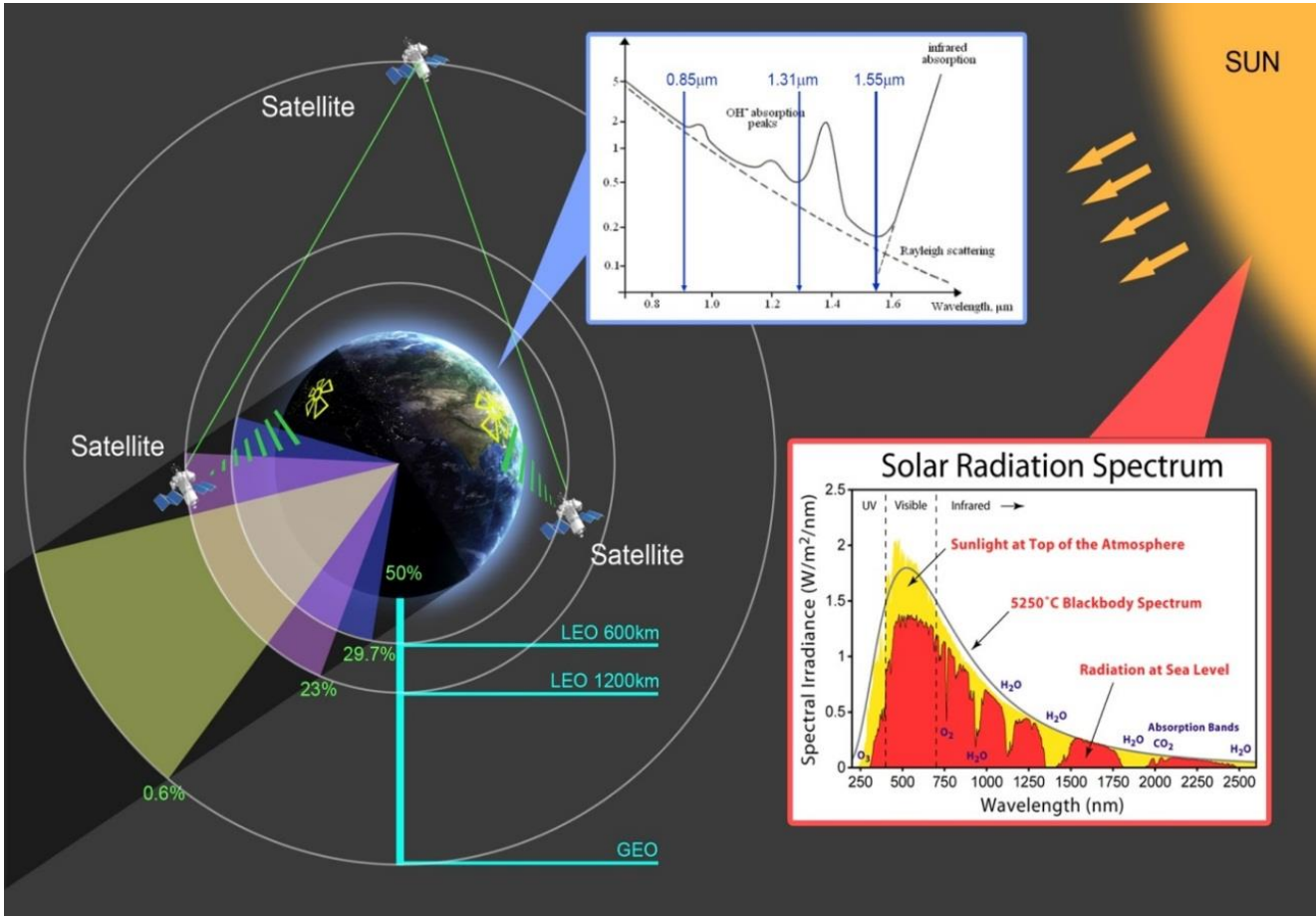


Satellite-to-ground docking experiment


- Liao, Sheng-Kai, et al. *Satellite-to-ground quantum key distribution*. Nature, 549(7670), 43–47, 2017.
- Liao, Sheng-Kai, et al. *Satellite-Relayed Intercontinental Quantum Network*. Physical Review Letters, 120(3), 30501, 2018.

# Introduction

Global QKD network.
All time.
LEO, GEO.

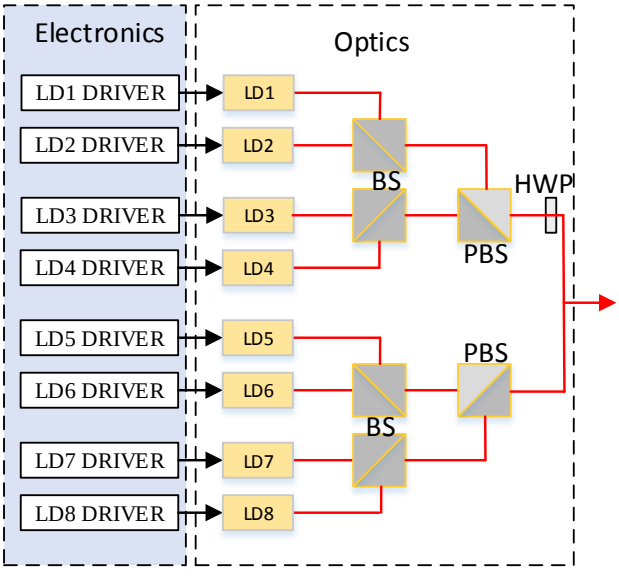


# Introduction

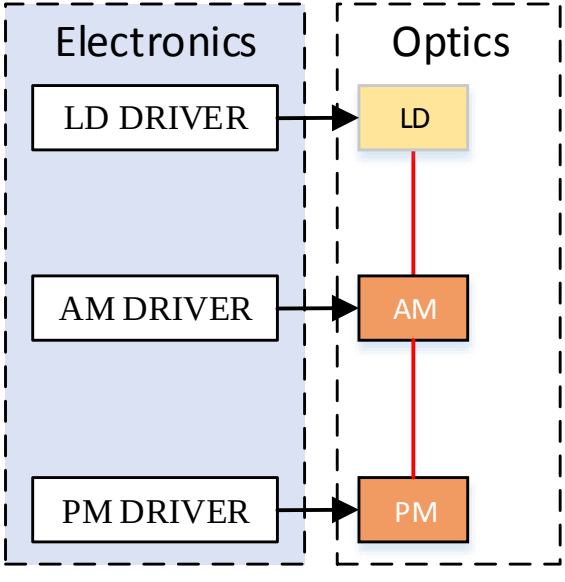


## Optical Source for QKD

Design 1: multiple lasers




Design 2: single laser with AM and PM




- Both methods need multichannel electric drivers with a deterministic phase skew.

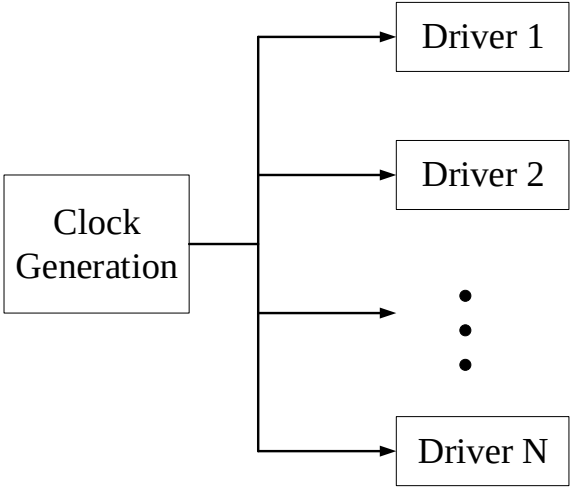
# Introduction



**Solution for multichannel electric drivers**

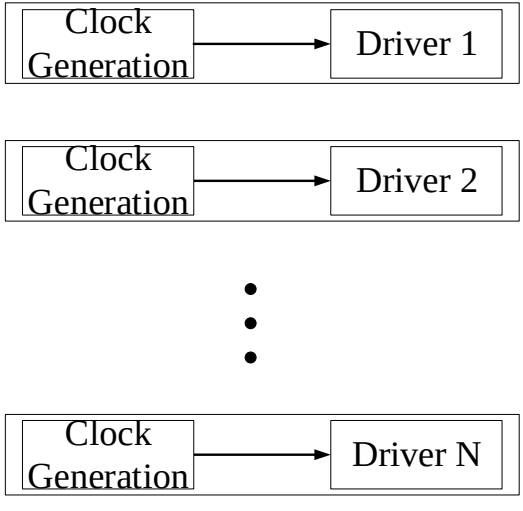
Low speed (< 100 MHz)

Parallel drivers with same clock




High speed (> 1 GHz)

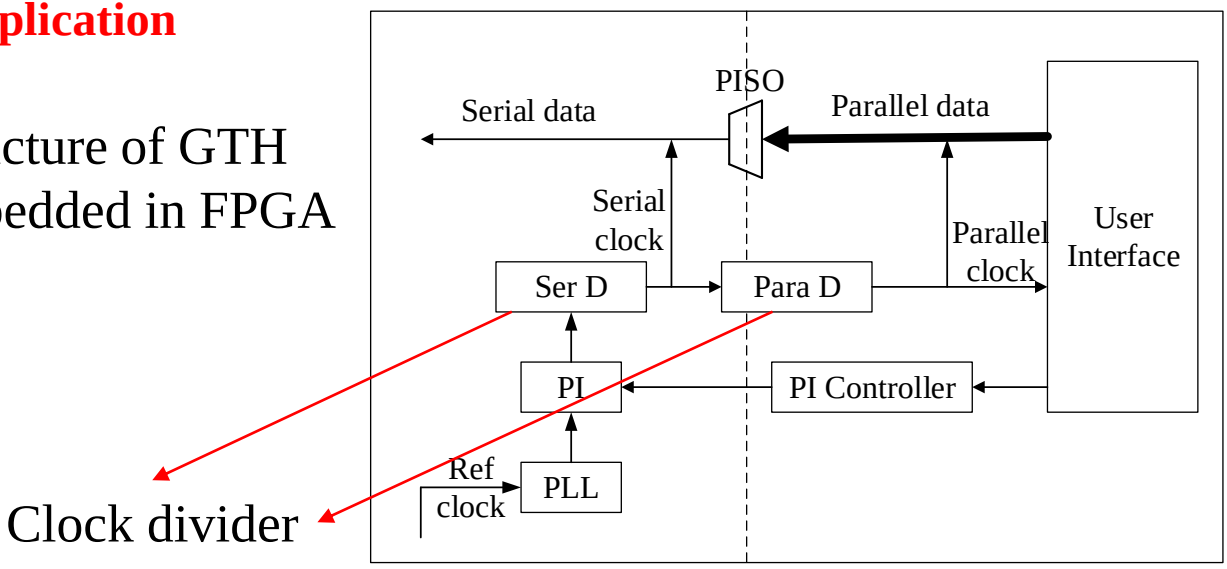
Serial drivers with independent clock



# Introduction

**High speed application**

Structure of GTH embedded in FPGA

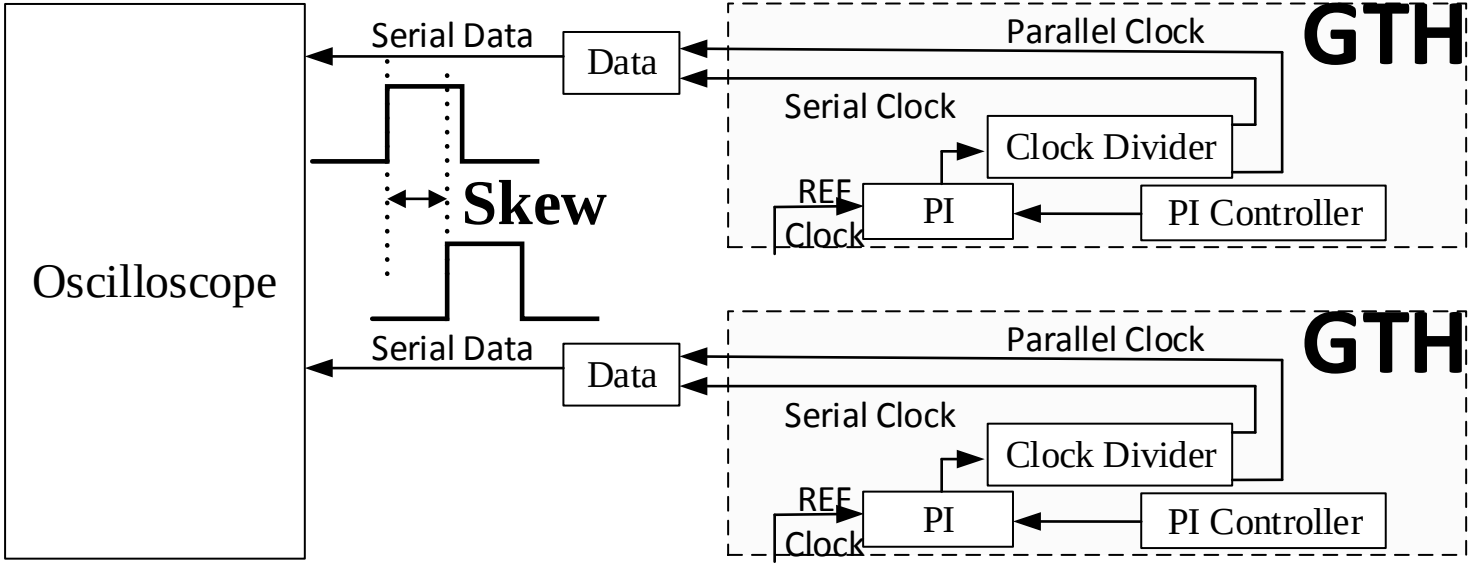



- Every time the system powers up or resets, clock dividers release at a random time.

# Introduction



**Random skew**




- When multiple channels are included, there appeal random skew among channels.

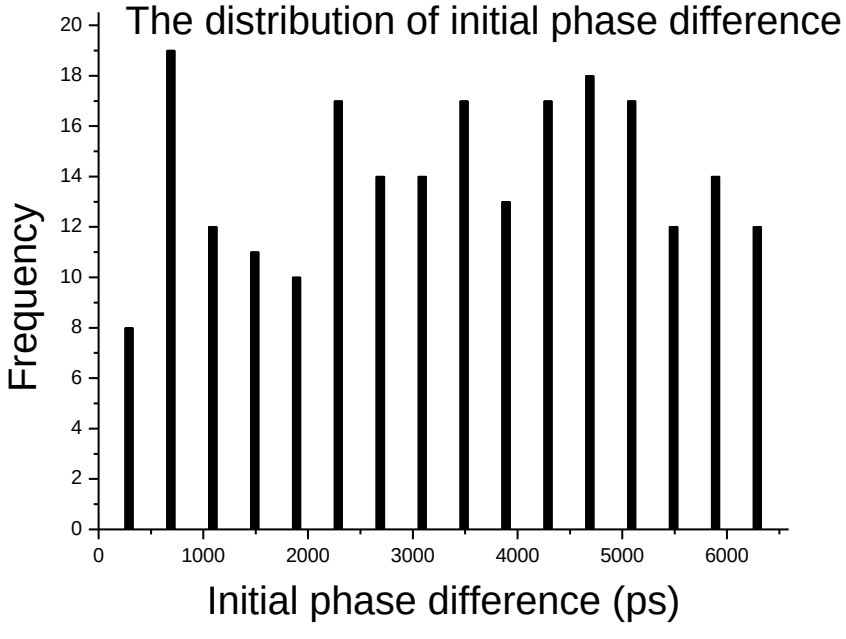
# Introduction



**Random skew test**

Conditions:

- GTH run at rate 2.5 Gbps,
- PLL output period 400 ps,
- Parallel data width 16,
- Parallel period 6.4 ns,
- System powers up or resets for 225 times.




Results:

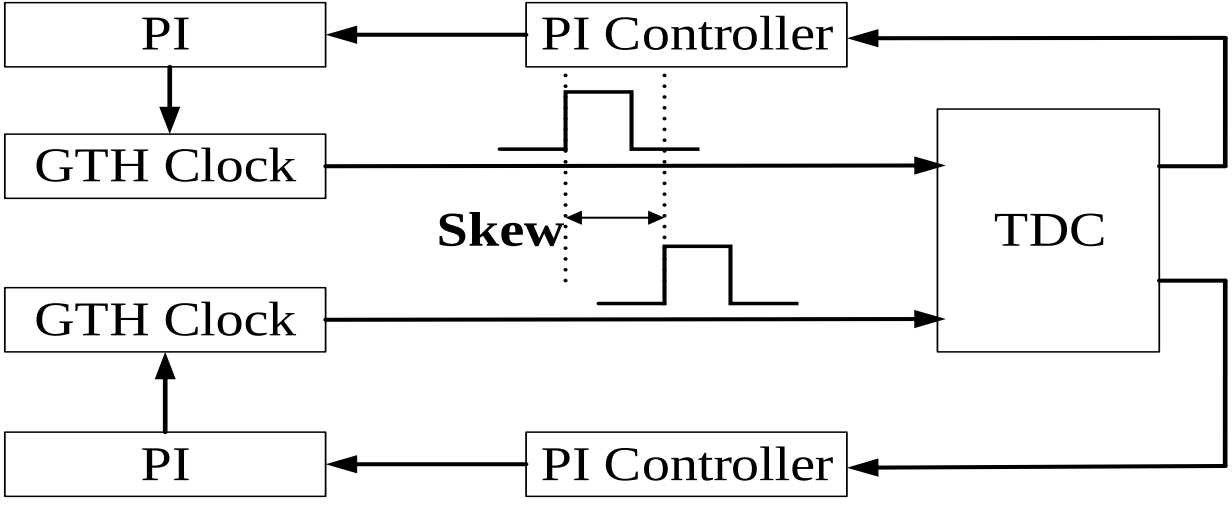
The skew conforms to a random distribution, it is the integral multiple of 400 ps.

# Introduction



How to solve the intrachannel random skew?

- Self-phase alignment: 22 ps RMS precision, the maximum is 100 ps.
- Another approach




- TDC measured the intrachannel skew.
- PI tuned the GTH's clock phase.

# Outline

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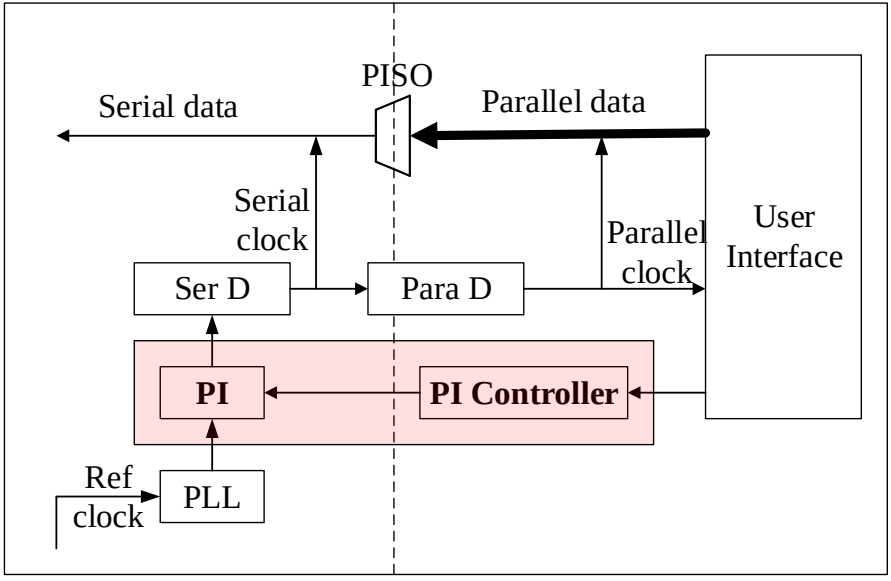
# PI Controller



PI embedded in GTH,
Tuning the clock phase of PLL output,




PI tuned step size

$$\mathrm{STEP}_{(\mathrm{UI})} = \frac{W_{pi}[3:0]}{64 * D_{txout}}$$

- $W_{pi}$: ranging from 1 to 15,
- 1 represent the minimal step size.
- $D_{txout}$ : Serial divider.

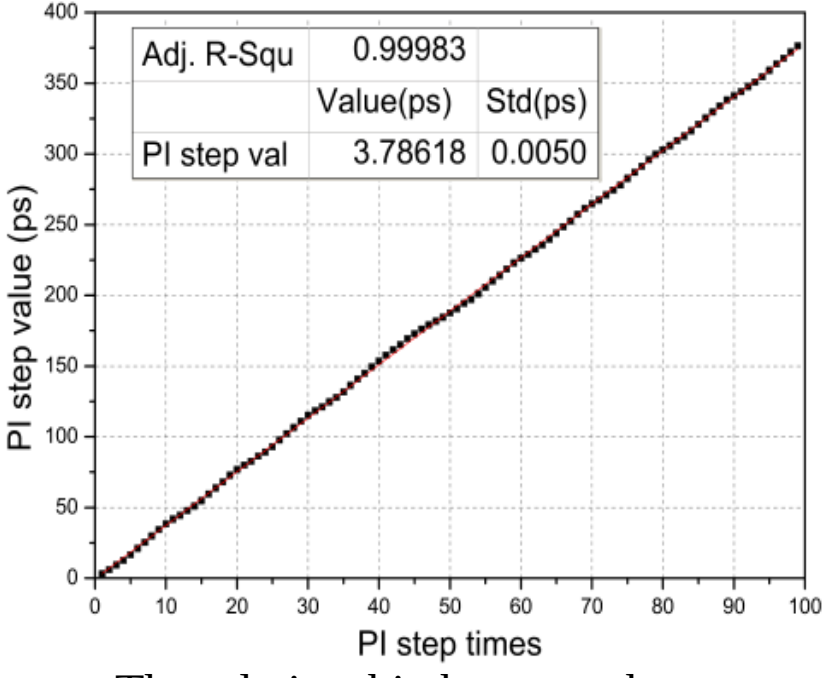
- The UI is 400 ps, $D_{txout}$ is 2, so the theoretical minimal step size is 3.125 ps.

# PI Controller



A test for the precision of PI adjustment

- Good linear
- Adj. R-Square equals 0.99983
- The slope is 3.79 ps



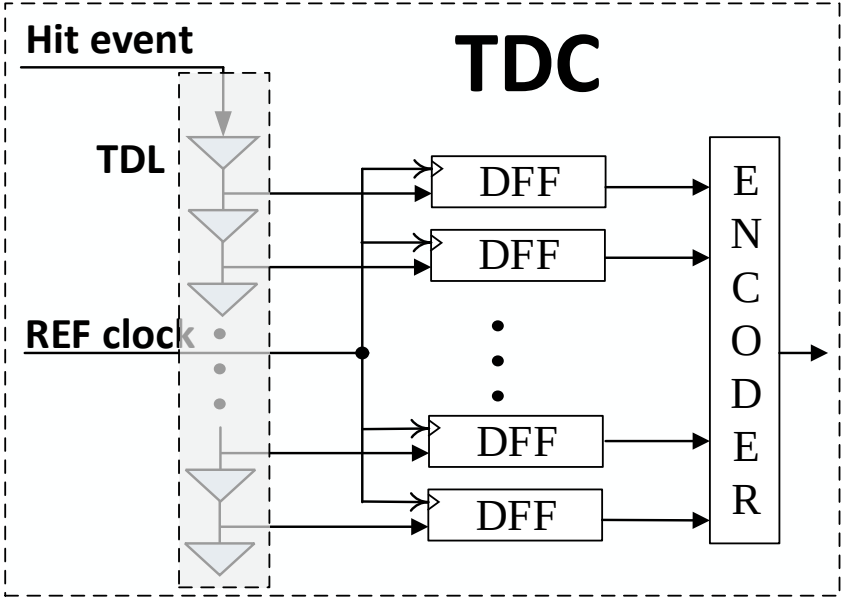

The relationship between the step value and the tuned times.

3.79 ps tunable precision is enough for the system running at rate 2.5Gbps.

# Outline

## Time delay line TDC

- Hit event: hit signal needing to measure,
- REF Clock: the system clock,
- TDL: time delay line,
- Encoder: turn the temperature code to bin code,

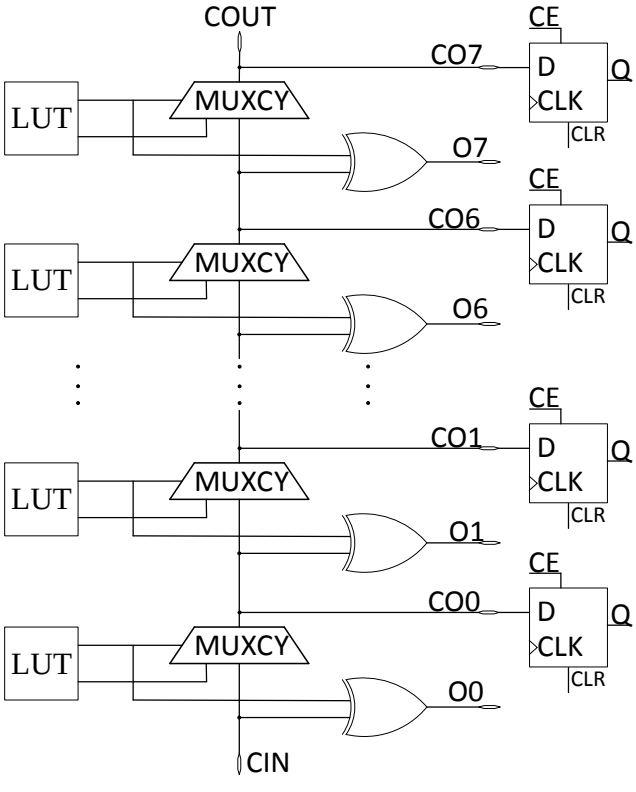



Sketch map of Time-interval TDC

Q. Shen *et al.*, *IEEE Trans. Nucl. Sci.*, vol. 62, no. 3, pp. 947–954, 2015.
Y. Wang and C. Liu, IEEE Trans. Nucl. Sci., vol. 63, no. 5, pp. 2632–2638, 2016.

## Constructing TDL with carry chain.

- UltraScale Kintex KU040,
- Carry8: **8 carry-out bits**, 8 data bits. 16 delay units at most.



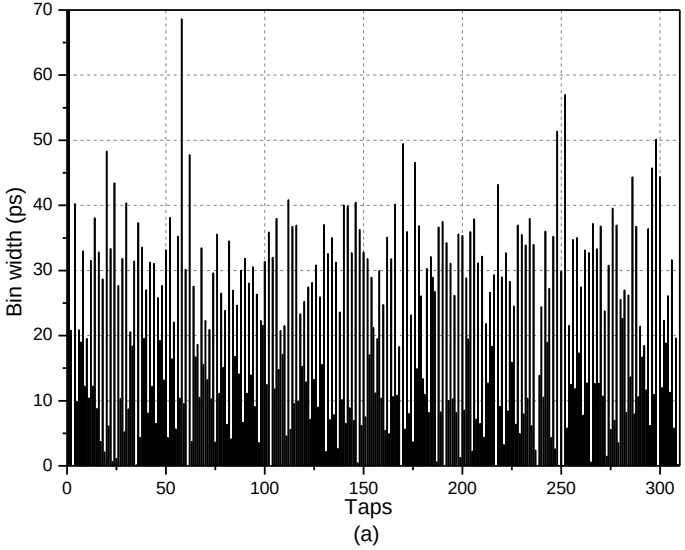

Define parameter M represent divided factor of Carry8.

## Tests of performance of TDC

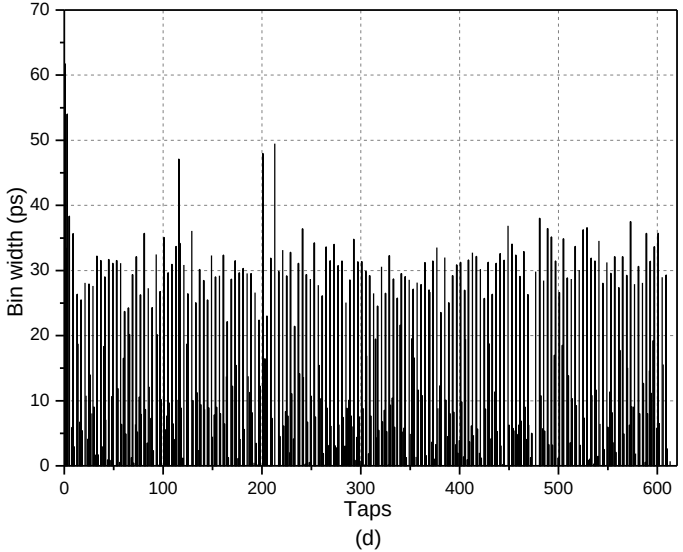
- The system clock period is 6.4 ns.
- The number of taps with M=2 is 309.
- The number of taps with M=4 is 613.

The bin size distribution

M=2, LSB = 20.4 ps

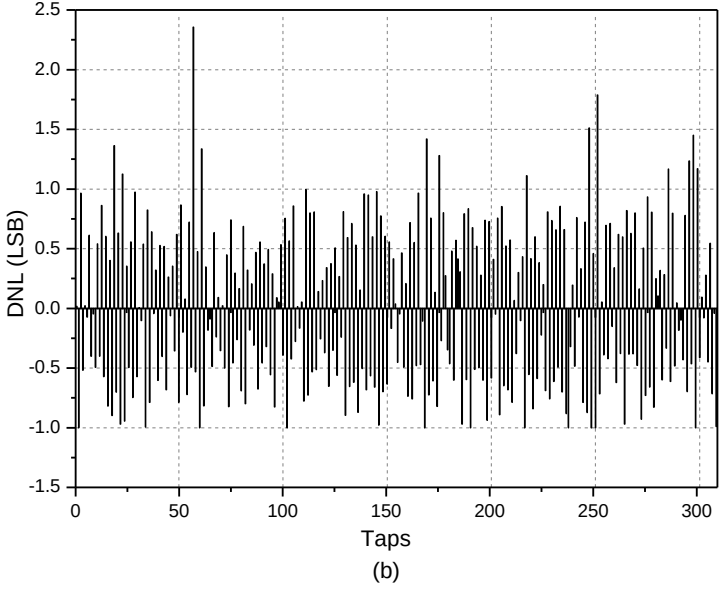



M=4, LSB = 10.2 ps

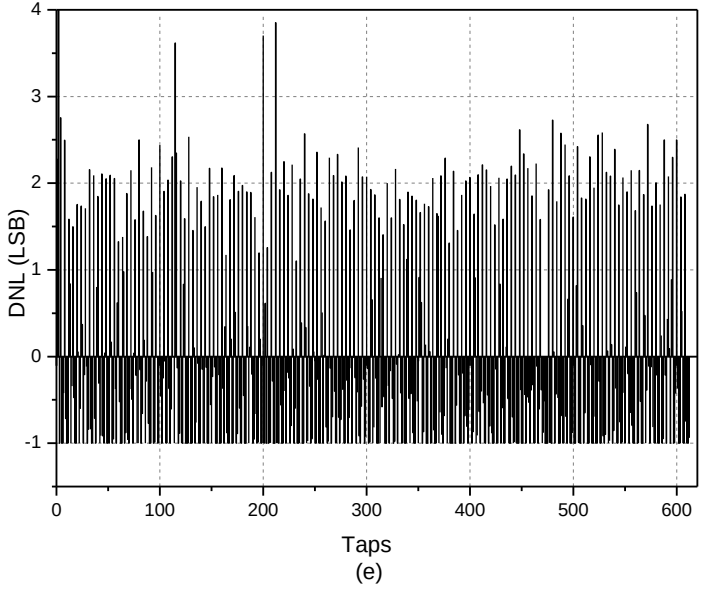


## DNL statistics

M=2




M=4

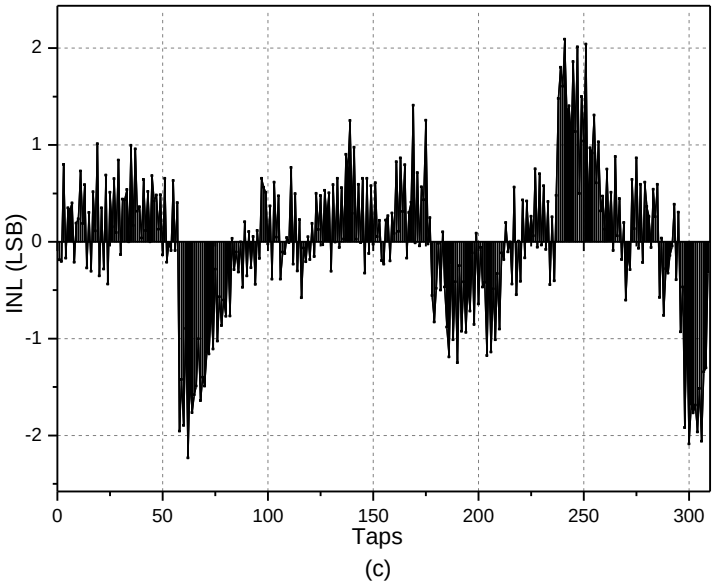



The DNL in most bins are smaller than ±1 LSB and the maximum is about 2.5 LSB.

The DNL with M = 4 are smaller than 2 LSB in most bins, worse than that M = 2

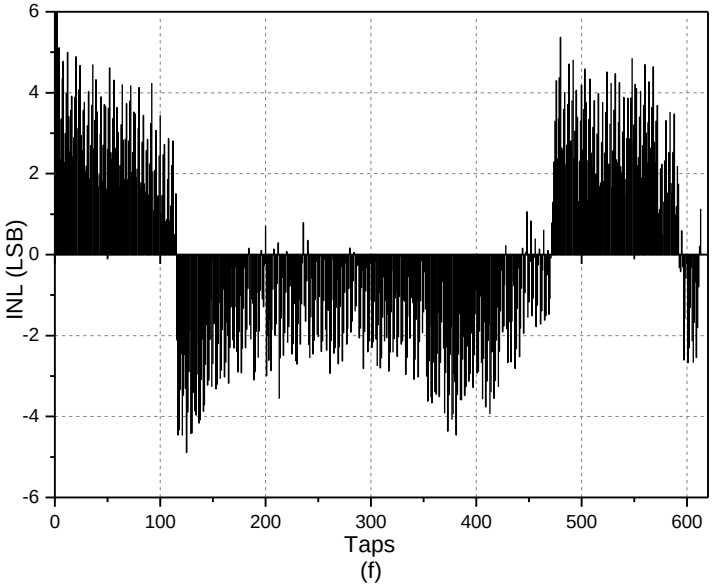
## INL statistics

M=2




The fitting INL in most bins is smaller than ±2 LSB.

M=4

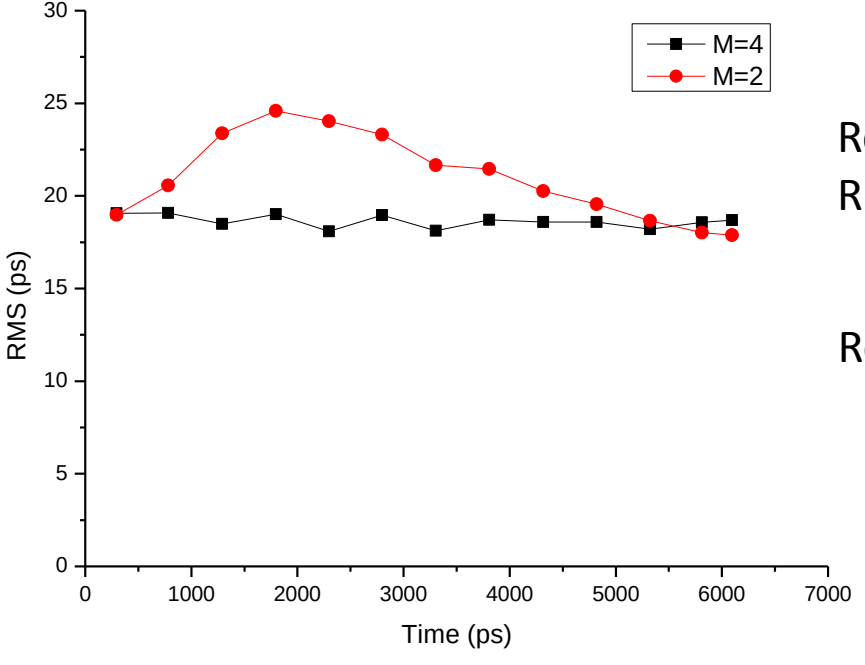



The fitting INL in most bins is smaller than ±4 LSB.

The fitting INL shows that a system error exists, which attributes to the large delay spanning banks in FPGA.

## Resolution test

Resolution test: a delay line test was applied to measure TDC resolution by constructing two identical delay chains




Resolution (M=2): 17.8 ps~24.6 ps RMS.

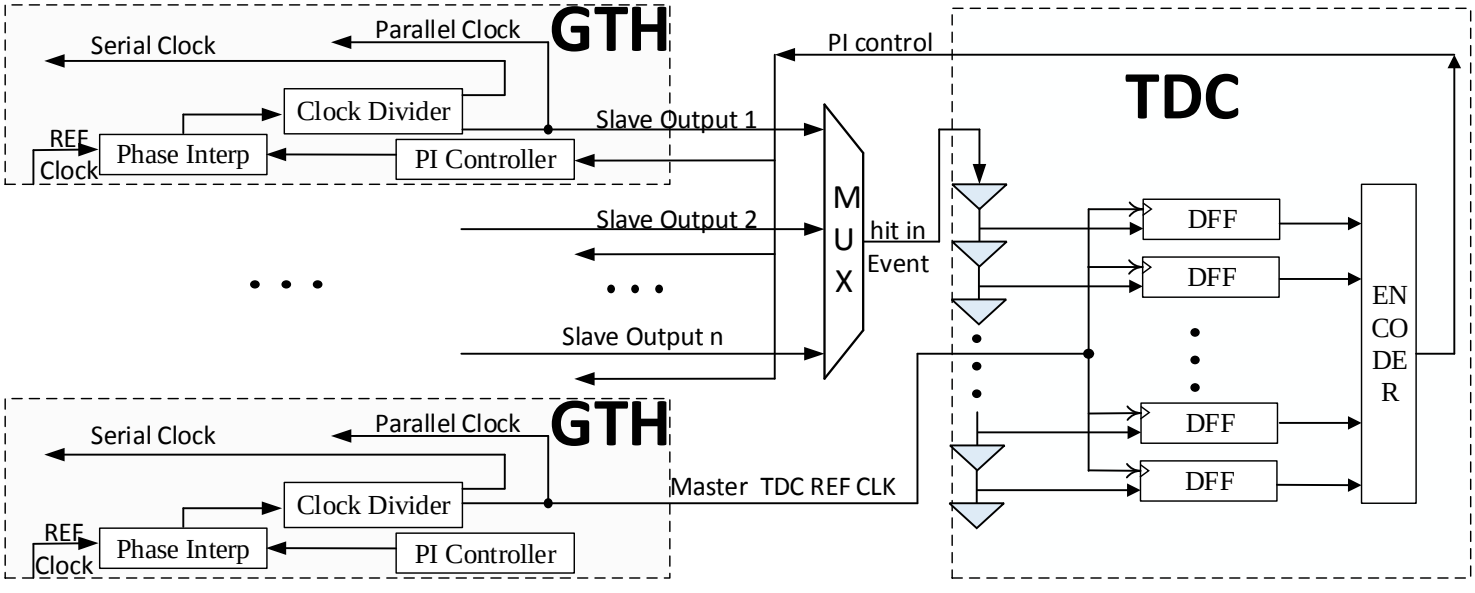
Resolution (M=4): 18 ps RMS. Flatter

# Outline

# Time Synchronization



## Multichannel time synchronization

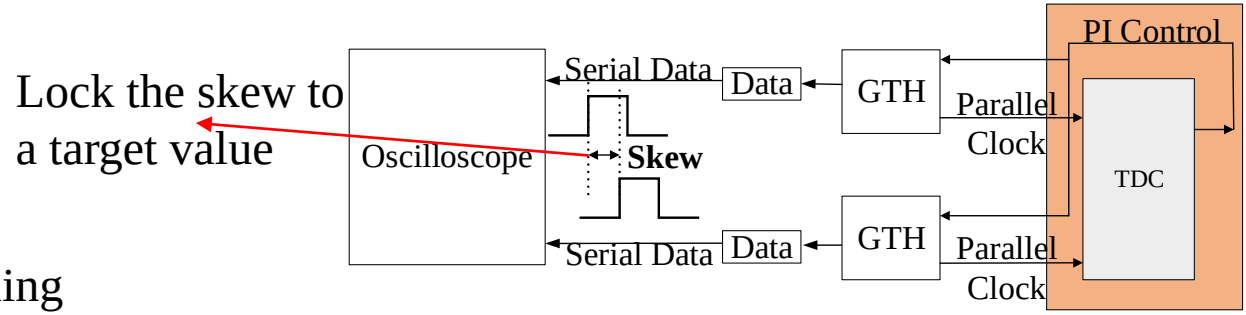



The parallel clock of master channel is routed as the system clock. All slave channels are combined into a mux.

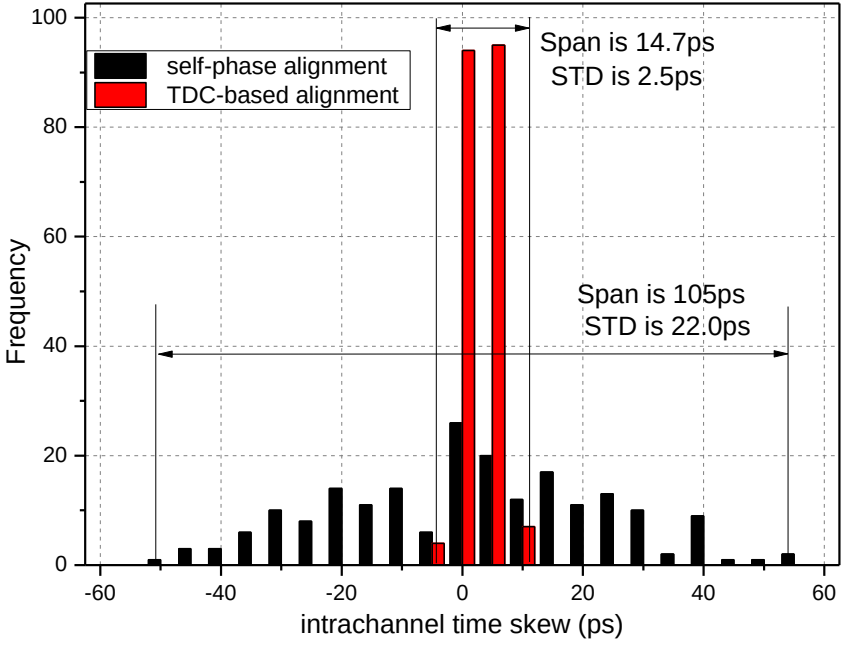
# Time Synchronization



## Test for precision of intrachannel time synchronization




200 sampling




Self-phase alignment :
the maximum is 105 ps,
the RMS is 22 ps.

TDC-based alignment:
the maximum is 14.7 ps,
the RMS is 2.5 ps.

# Time Synchronization

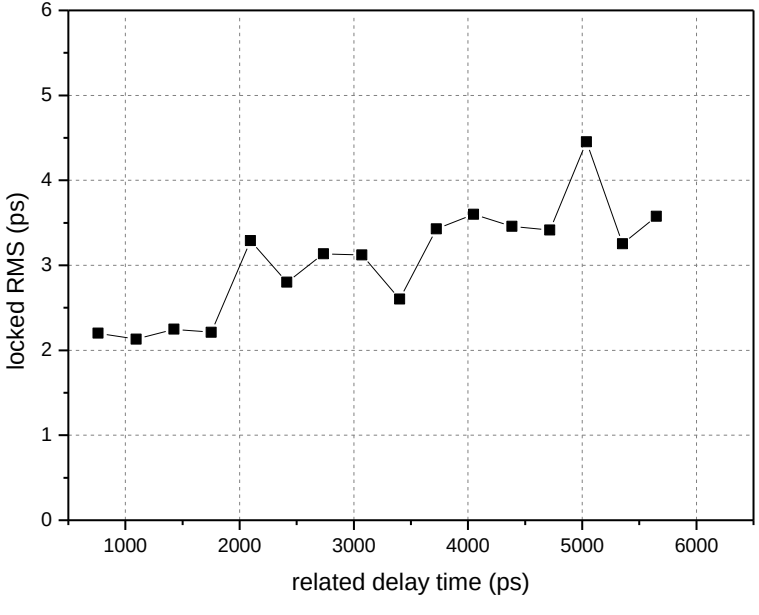


**Test for synchronized precision at different value**

- Self-phase alignment: the intrachannel skew is not capable of adjusting.
- TDC-based alignment: the intrachannel skew can be tuned to arbitrary value.

Synchronization precision at different points sampling 25 times.

Ranging from 2.2 ps~4.4 ps.



# Outline

# Summary



## ➢ Conclusion

With a PI and a TDC, we implement a high-precision 2.5 ps RMS time synchronization among multichannel serial transceivers. Besides, the intrachannel skew can be locked to arbitrary offset with approximate precision.

## ➢ Outlook

The employed TDC resolution is18 ps, we can further improve the TDC resolution with proper methods, such as INL calibration, bin decimation, and multiple chains measurement.
And eventually, a higher-precision time synchronization is achievable.

# Thank you!