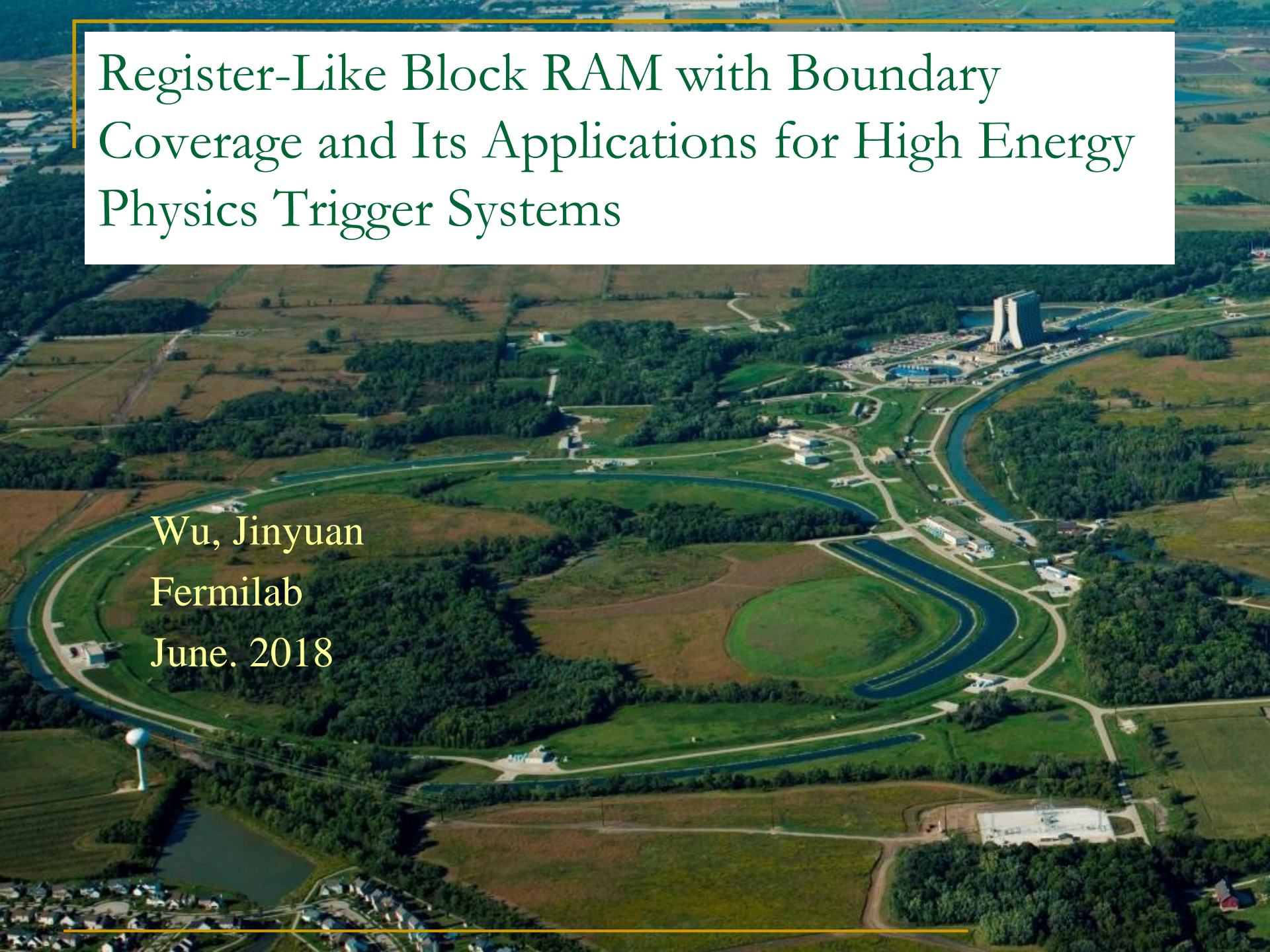


# Register-Like Block RAM with Boundary Coverage and Its Applications for High Energy Physics Trigger Systems

Wu, Jinyuan

Fermilab

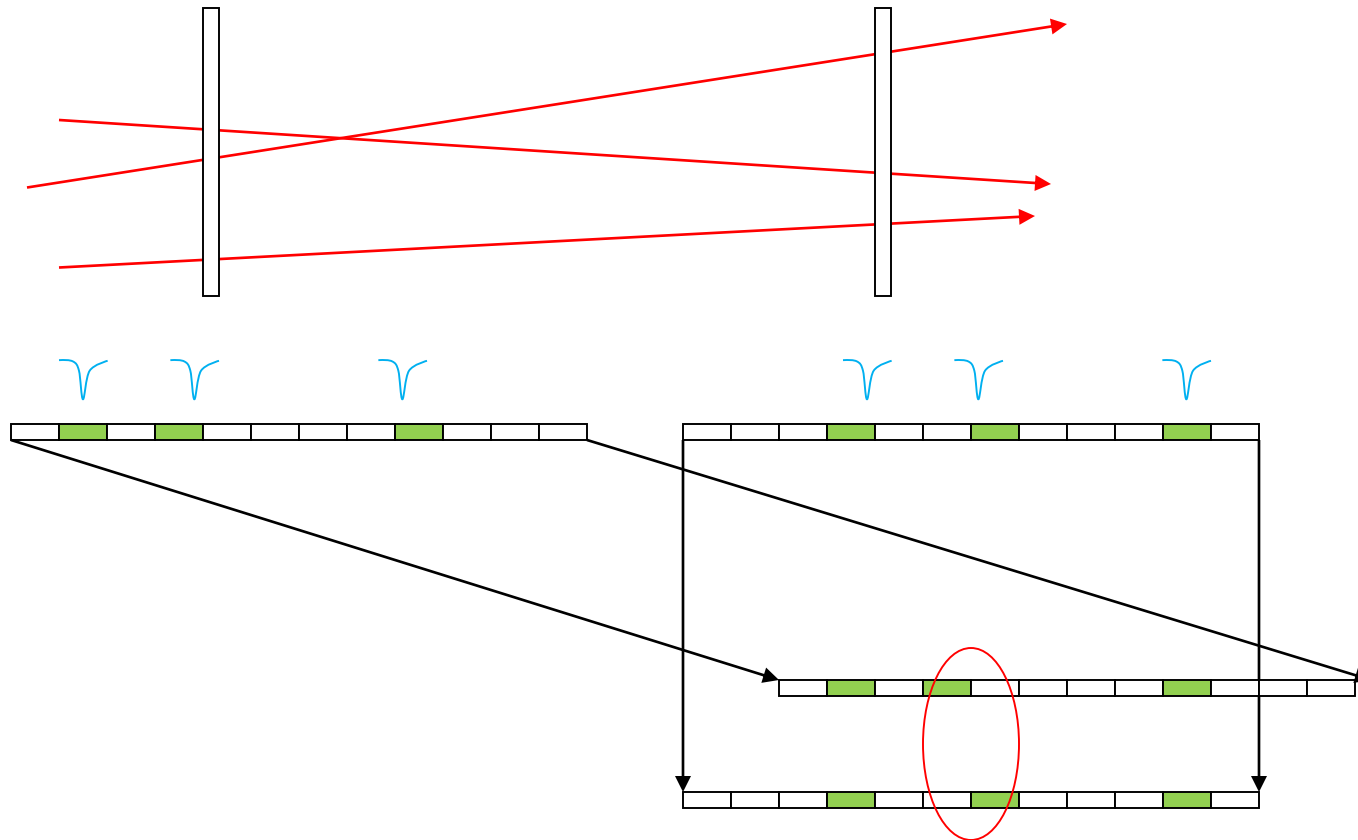
June, 2018



# Introduction

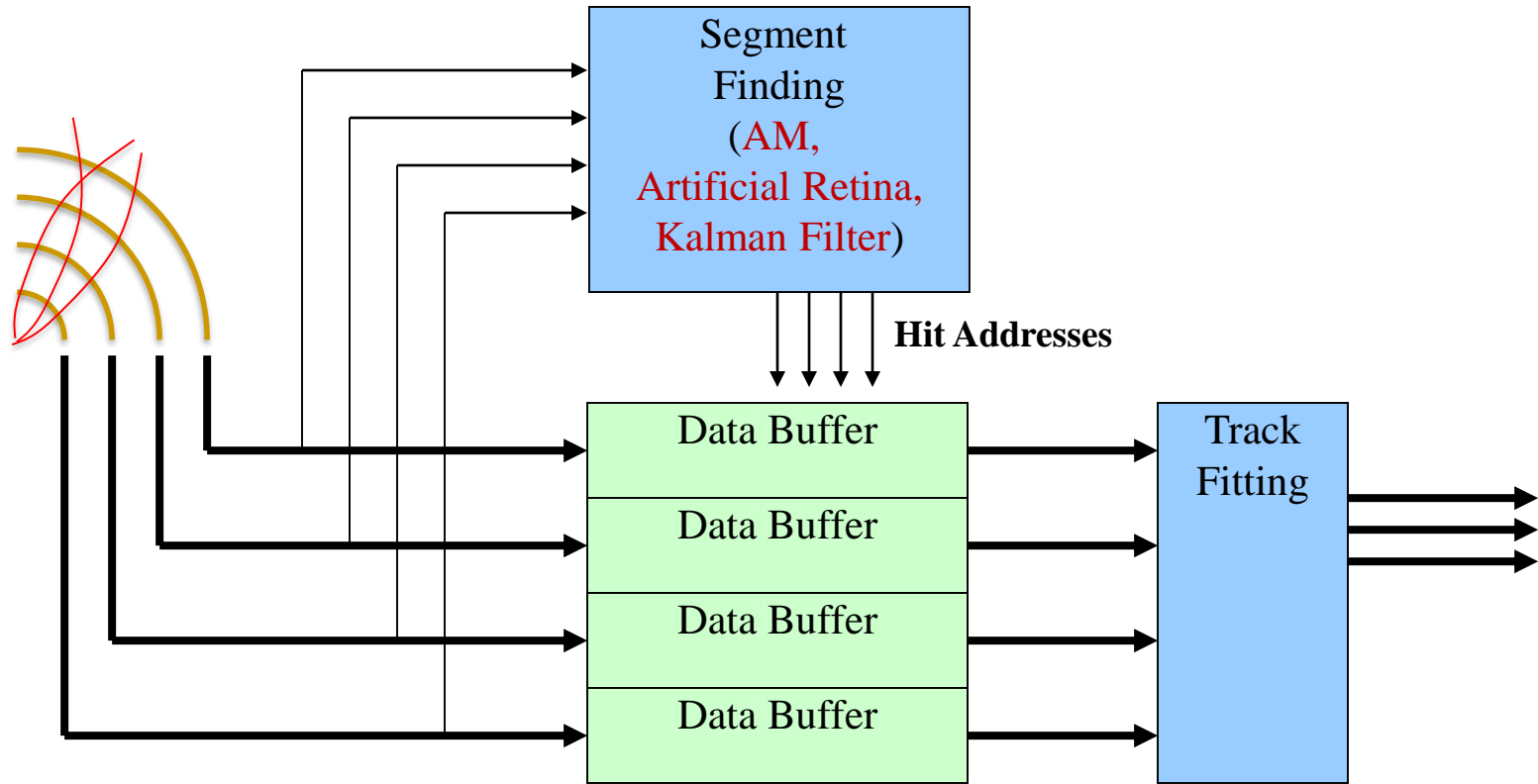
- (2016) The Register-Like Block RAM operates as if it is a register, supporting:
  - Single clock cycle booking
  - Single clock cycle reading
  - Single clock cycle refreshing
- (2018) Boundary coverage feature is added for convenience of practical applications.

# Boundary Coverage for Coincidence Algorithms



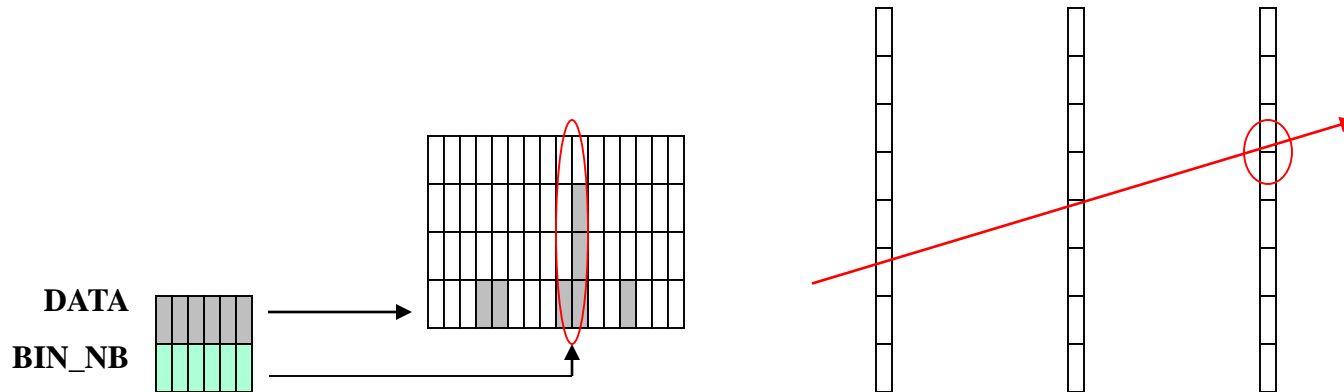
- In temporal domain coincidence trigger algorithms, it is necessary to check adjacent time bins to ensure well boundary coverage.

# Contemporary Tracking Trigger Schemes



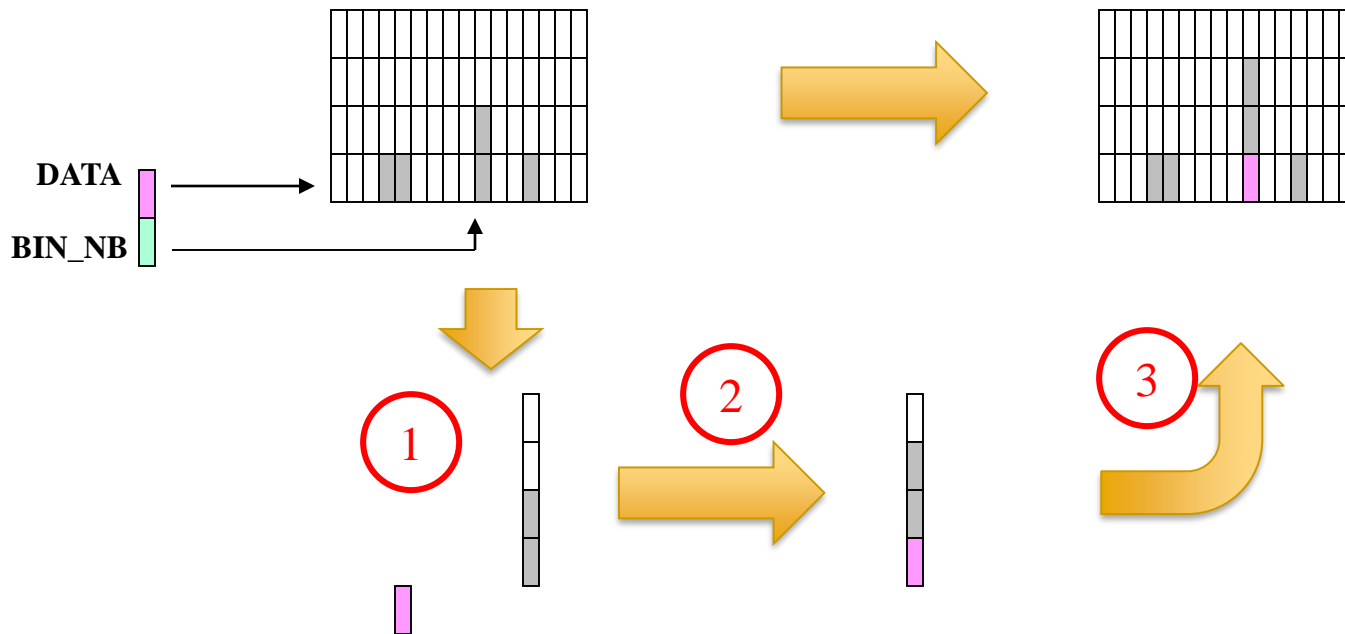
- Detector hit data are partially used in Segment Finding block while full data are stored in Data Buffer.
- Segment Finding block finds segments and output address of the hits in each segment.
- Full hit data are read out and sent to Track Fitting block to calculate track parameters.

# Boundary Coverage in Tracking Triggers



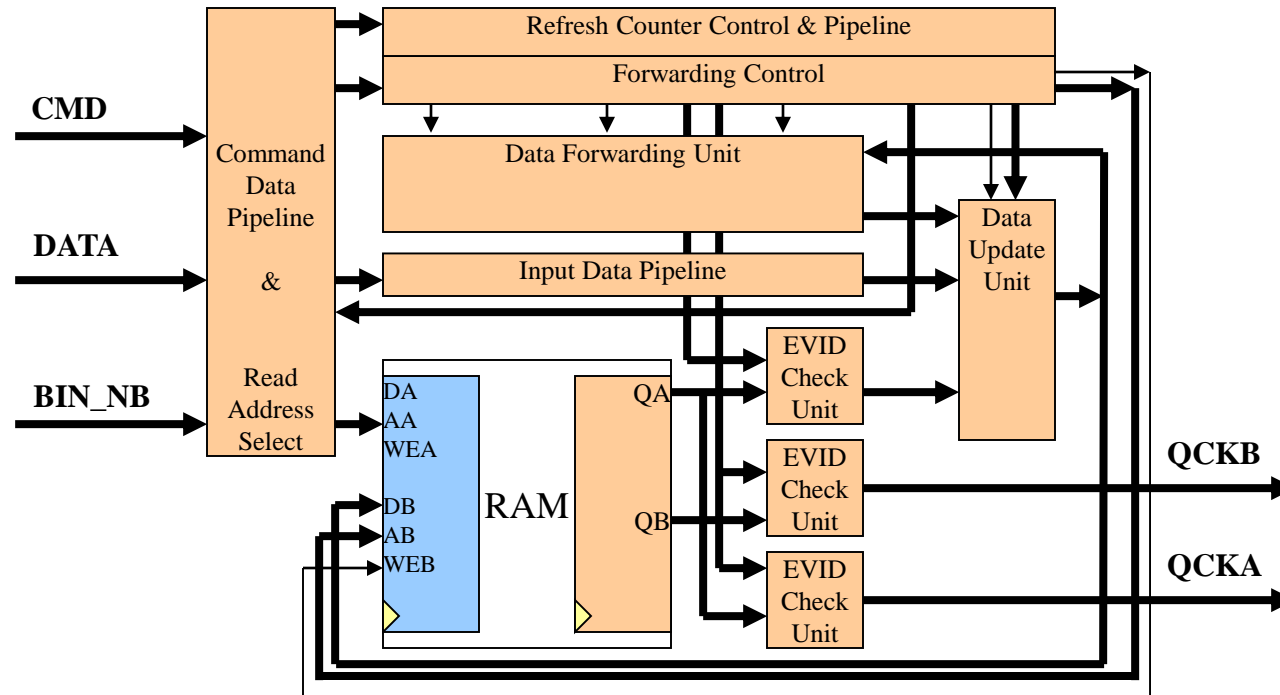
- Matching hits are checked in next neighbor bins for boundary coverage.

# Multiple Hits Per Bin



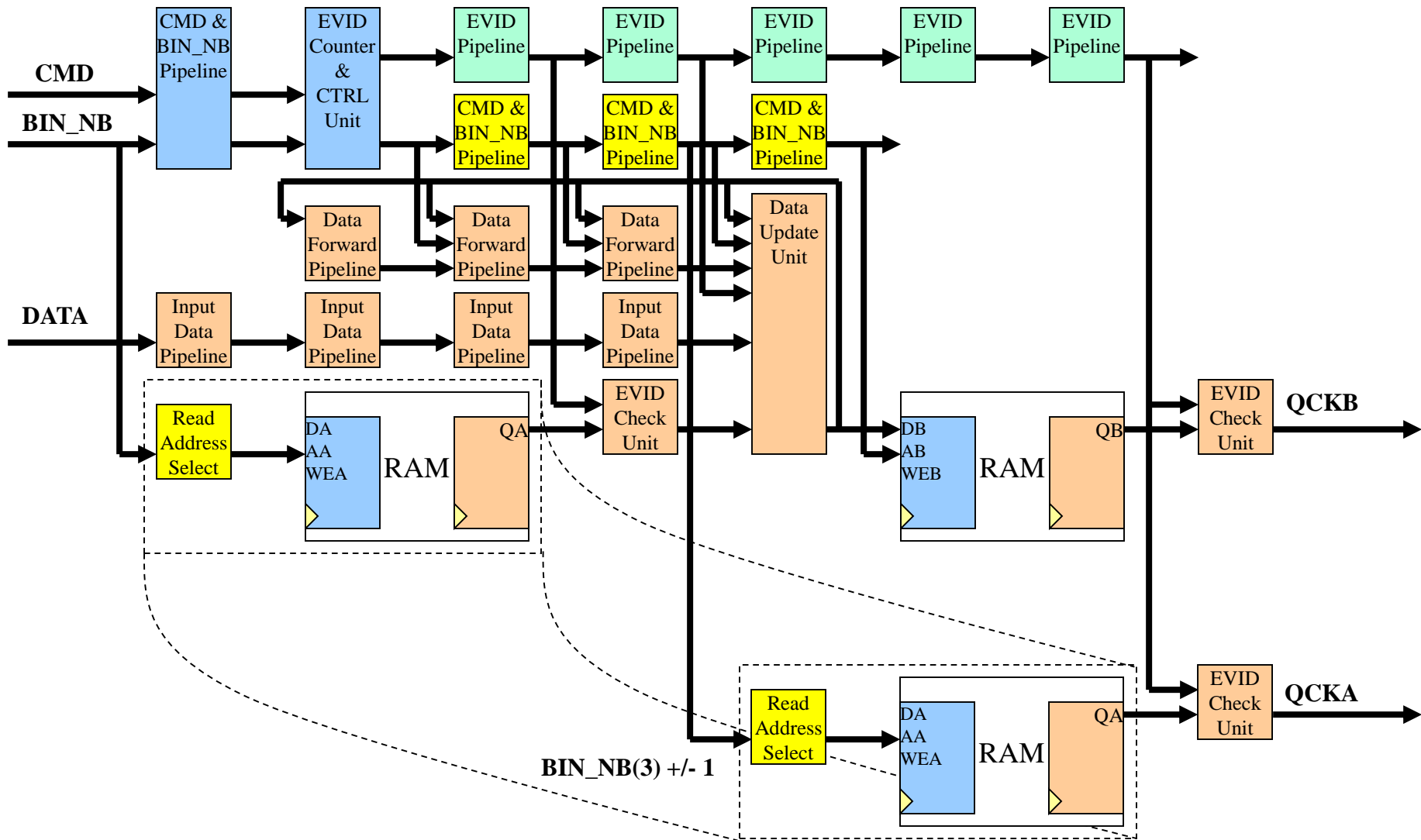
- Each bin may store multiple hits.
- A bin takes three steps to update:
  - Reading out the bin contents
  - Attaching new data
  - Writing back to the bin

# Block Diagram

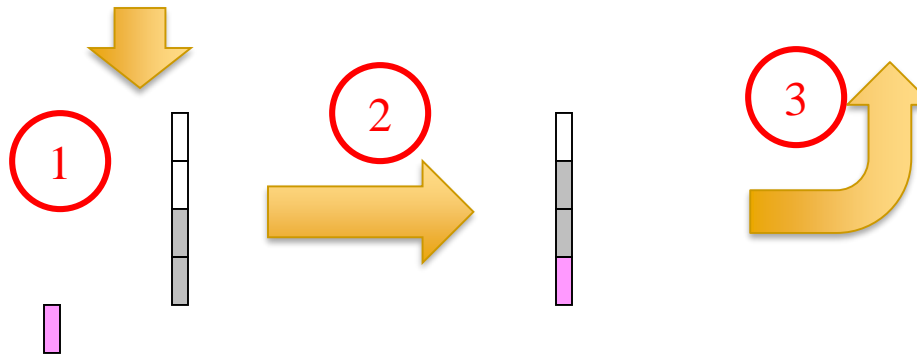
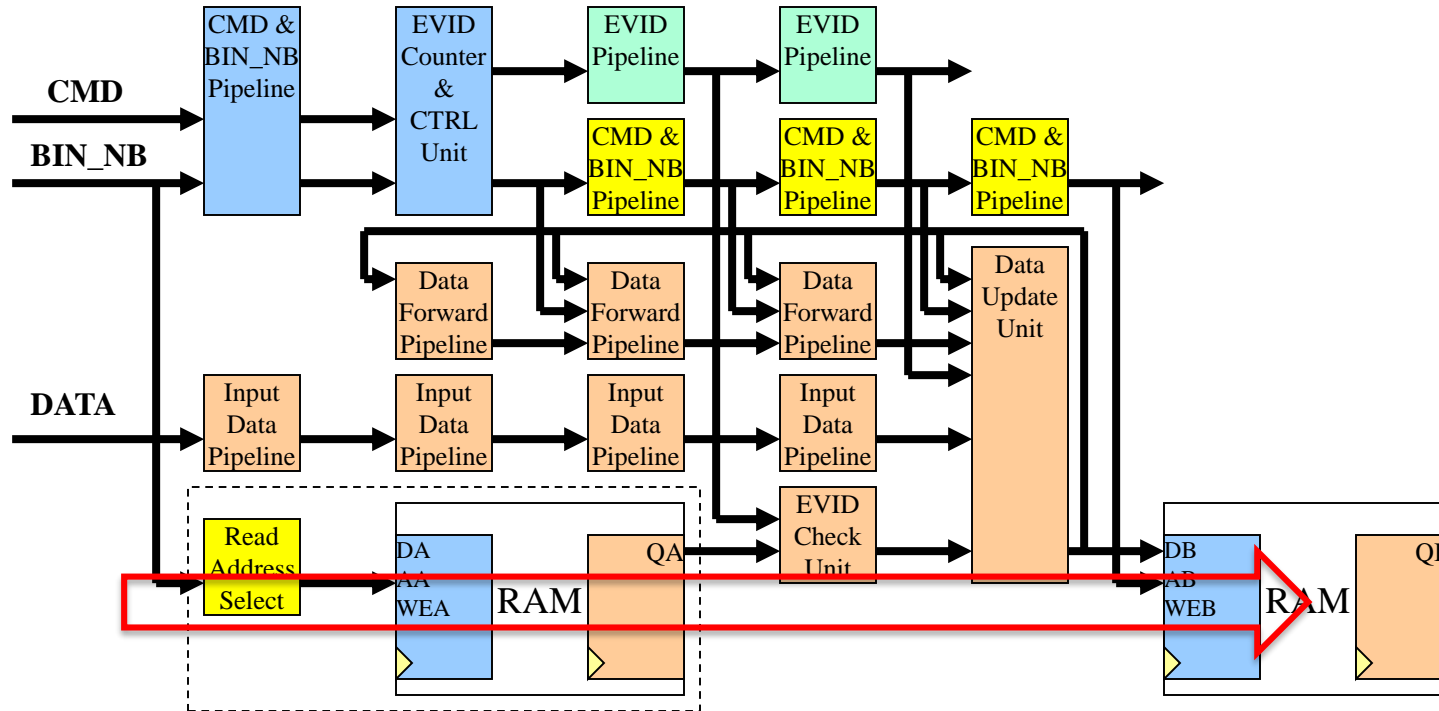


- Entire functional block is arranged as a multi-stage pipeline to ensure single clock cycle operations.

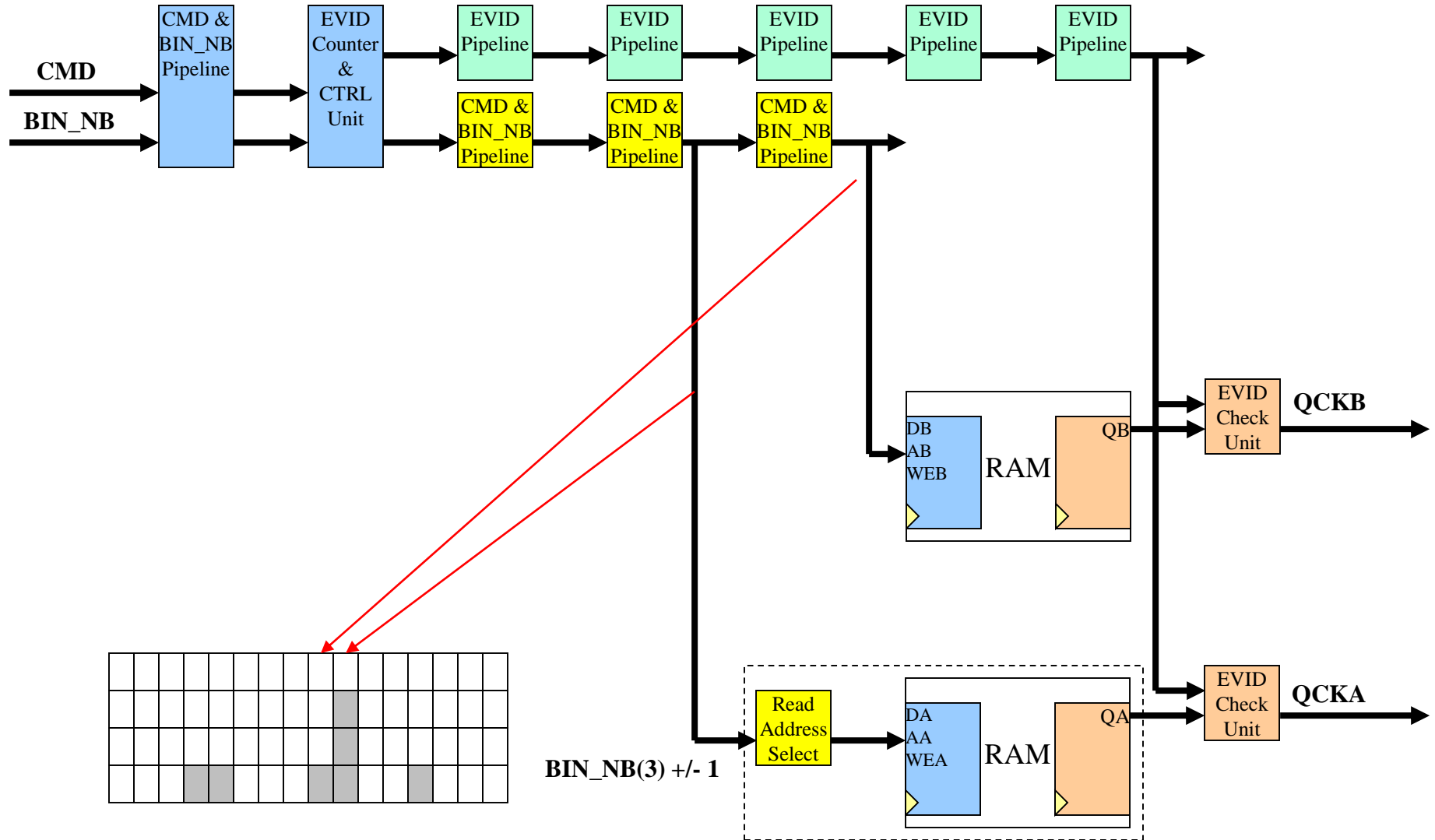
# Detailed Block Diagram



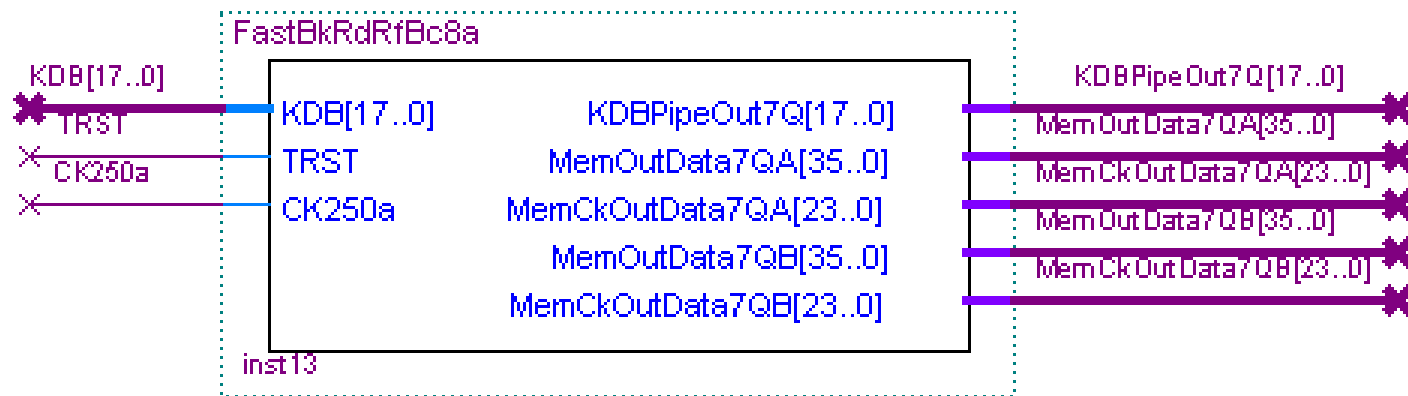
# Booking Operation



# Reading Operation

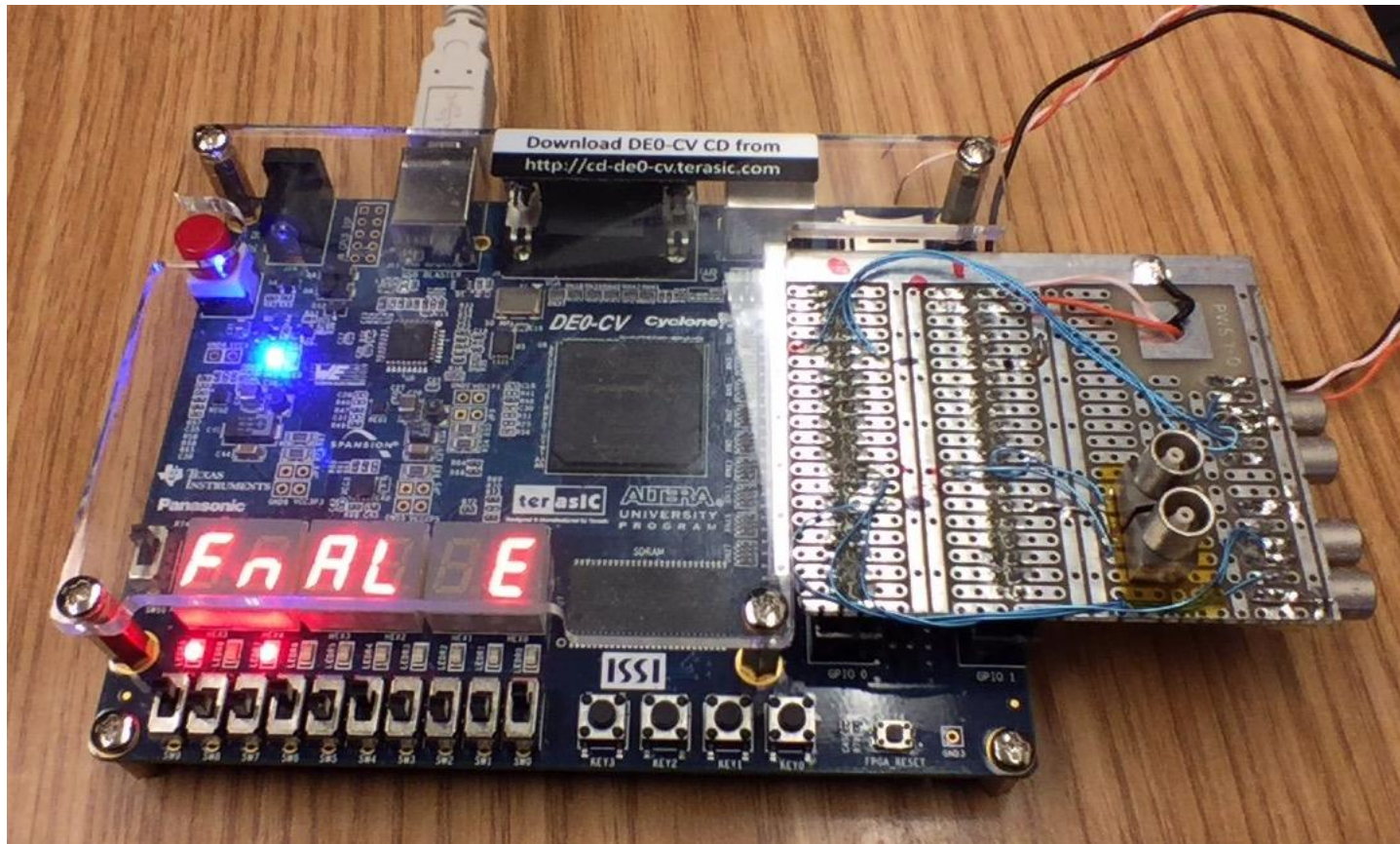


# Implementation



- The functional block has been implemented in a Cyclone V FPGA.
- Operating clock frequency was 250 MHz

# Test Platform



- The test was performed in a evaluation board.

# Test Results

		Op	InData	Addr	Valid	EvtID	MemDataB			MemDataA		
							1	2	3	1	2	3
0	00000FF300000000FF000000000000	0: NoOpRd		00	0	300						
1	00000FF300000000FF000000000000	0: NoOpRd		00	0	300						
2	00000FF300000000FF000000000000	0: NoOpRd		00	0	300						
3	00000FF300000000FF000000000000	0: NoOpRd		00	0	300						
4	00000FF300000000FF000000000000	0: NoOpRd		00	0	300						
5	30000FFB95000000FF000000000000	3: Refresh		00	1	395						
6	2A505FFB960000A5FF0000A5000000	2: Book	A5	05	1	396			A5			
7	2B505FFB9600A5B5FF00A5B5000000	2: Book	B5	05	1	396		A5	B5			
8	2C505FFB96A5B5C5FFA5B5C5000000	2: Book	C5	05	1	396	A5	B5	C5			
9	2A303FFB960000A3FF0000A3000000	2: Book	A3	03	1	396			A3			
10	2A404FFB960000A4FF0000A4000000	2: Book	A4	04	1	396			A4			
11	2B303FFB9600A3B3FF00A3B3000000	2: Book	B3	03	1	396		A3	B3			
12	2A808FFB960000A8FF0000A8000000	2: Book	A8	08	1	396			A8			
13	2B404FFB9600A4B4FF00A4B4000000	2: Book	B4	04	1	396		A4	B4			
14	2A707FFB960000A7FF0000A7000000	2: Book	A7	07	1	396			A7			
15	2A606FFB960000A6FF0000A6000000	2: Book	A6	06	1	396			A6			
16	2B808FFB9600A8B8FF00A8B8000000	2: Book	B8	08	1	396		A8	B8			
17	2A909FFB960000A9FF0000A900A3B3	2: Book	A9	09	1	396			A9		A3	B3
18	10000FF300000000FF000000000000	1: Read		00	0	300						
19	10001FF301000000FF000000000000	1: Read		01	0	301						
20	10002FF302000000FF000000000000	1: Read		02	0	302						
21	10003FFB9600A3B3FF00A3B3000000	1: Read		03	1	396		A3	B3			
22	10004FFB9600A4B4FF00A4B400A3B3	1: Read		04	1	396		A4	B4		A3	B3
23	10005FFB96A5B5C5FFA5B5C500A4B4	1: Read		05	1	396	A5	B5	C5		A4	B4
24	10006FFB960000A6FF0000A6A5B5C5	1: Read		06	1	396			A6	A5	B5	C5
25	10007FFB960000A7FF0000A70000A6	1: Read		07	1	396			A7			A6
26	10008FFB9600A8B8FF00A8B80000A7	1: Read		08	1	396		A8	B8			A7
27	10009FFB960000A9FF0000A900A8B8	1: Read		09	1	396			A9		A8	B8
28	1000AFF30A000000FF0000000000A9	1: Read		0A	0	30A						A9
29	1000BFF30B000000FF000000000000	1: Read		0B	0	30B						
30	1000CFF30C000000FF000000000000	1: Read		0C	0	30C						
31	1000DFF3630000BFFF000000000000	1: Read		0D	0	363			BF			
32	1000EFF30E000000FF000000000000	1: Read		0E	0	30E						
33	1000FFF30F000000FF000000000000	1: Read		0F	0	30F						
34	10010FF36A00006FFF000000000000	1: Read		10	0	36A			6F			
35	10011FF367000068FF000000000000	1: Read		11	0	367			68			
36	10012FF312000000FF000000000000	1: Read		12	0	312						
37	10013FF313000000FF000000000000	1: Read		13	0	313						
38	30000FFB96000000FF000000000000	3: Refresh		00	1	396						
39	2D121FFB970000D1FF0000D1000000	2: Book	D1	21	1	397			D1			
40	2D222FFB970000D2FF0000D2000000	2: Book	D2	22	1	397			D2			

Refreshing

Booking

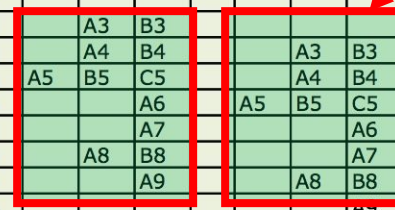
Reading

# The Boundary Coverage

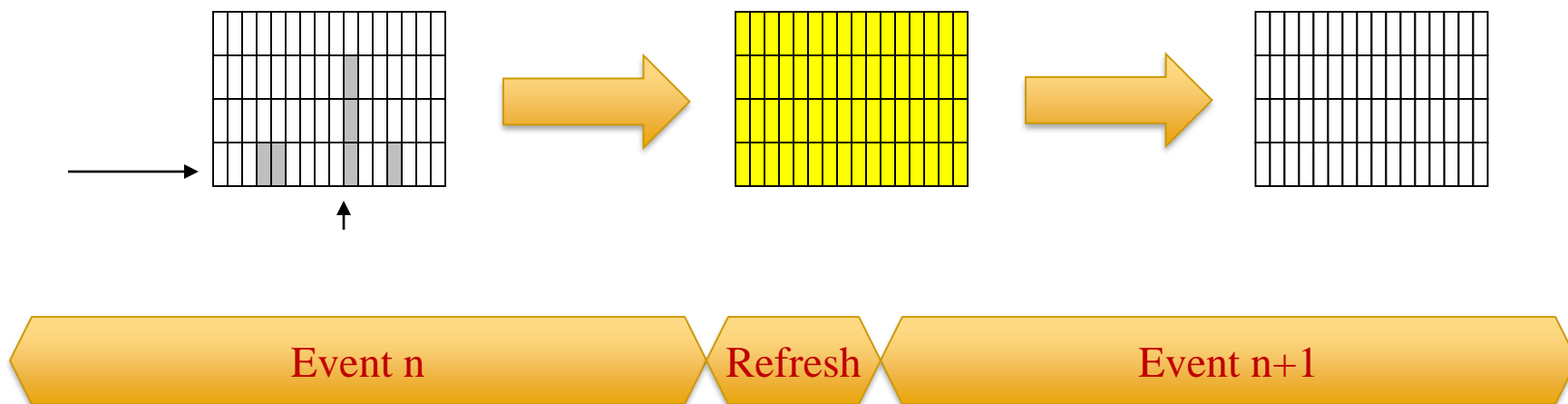
		Op	InData	Addr	Valid1	EvtID	MemDataB			MemDataA		
							1	2	3	1	2	3
0	00000FF300000000FF000000000000	0: NoOpRd		00	0	300						
1	00000FF300000000FF000000000000	0: NoOpRd		00	0	300						
2	00000FF300000000FF000000000000	0: NoOpRd		00	0	300						
3	00000FF300000000FF000000000000	0: NoOpRd		00	0	300						
4	00000FF300000000FF000000000000	0: NoOpRd		00	0	300						
5	30000FFB95000000FF000000000000	3: Refresh		00	1	395						
6	2A505FFB960000A5FF0000A5000000	2: Book	A5	05	1	396			A5			
7	2B505FFB9600A5B5FF00A5B5000000	2: Book	B5	05	1	396		A5	B5			
8	2C505FFB96A5B5C5FFA5B5C5000000	2: Book	C5	05	1	396	A5	B5	C5			
9	2A303FFB960000A3FF0000A3000000	2: Book	A3	03	1	396			A3			
10	2A404FFB960000A4FF0000A4000000	2: Book	A4	04	1	396			A4			
11	2B303FFB9600A3B3FF00A3B3000000	2: Book	B3	03	1	396		A3	B3			
12	2A808FFB960000A8FF0000A8000000	2: Book	A8	08	1	396			A8			
13	2B404FFB9600A4B4FF00A4B4000000	2: Book	B4	04	1	396		A4	B4			
14	2A707FFB960000A7FF0000A7000000	2: Book	A7	07	1	396			A7			
15	2A606FFB960000A6FF0000A6000000	2: Book	A6	06	1	396			A6			
16	2B808FFB9600A8B8FF00A8B8000000	2: Book	B8	08	1	396		A8	B8			
17	2A909FFB960000A9FF0000A900A3B3	2: Book	A9	09	1	396			A9		A3	B3
18	10000FF300000000FF000000000000	1: Read		00	0	300						
19	10001FF301000000FF000000000000	1: Read		01	0	301						
20	10002FF302000000FF000000000000	1: Read		02	0	302						
21	10003FFB9600A3B3FF00A3B3000000	1: Read		03	1	396		A3	B3			
22	10004FFB9600A4B4FF00A4B400A3B3	1: Read		04	1	396		A4	B4		A3	B3
23	10005FFB96A5B5C5FFA5B5C500A4B4	1: Read		05	1	396	A5	B5	C5			
24	10006FFB960000A6FF0000A6A5B5C5	1: Read		06	1	396			A6	A5	B5	C5
25	10007FFB960000A7FF0000A70000A6	1: Read		07	1	396			A7			A6
26	10008FFB9600A8B8FF00A8B80000A7	1: Read		08	1	396		A8	B8			A7
27	10009FFB960000A9FF0000A900A8B8	1: Read		09	1	396			A9		A8	B8
28	1000AFF30A000000FF0000000000A9	1: Read		0A	0	30A						A9
29	1000BFF30B000000FF000000000000	1: Read		0B	0	30B						
30	1000CFF30C000000FF000000000000	1: Read		0C	0	30C						
31	1000DFF3630000BFFF000000000000	1: Read		0D	0	363			BF			
32	1000EFF30E000000FF000000000000	1: Read		0E	0	30E						
33	1000FFF30F000000FF000000000000	1: Read		0F	0	30F						
34	10010FF36A00006FFF000000000000	1: Read		10	0	36A			6F			
35	10011FF367000068FF000000000000	1: Read		11	0	367			68			
36	10012FF312000000FF000000000000	1: Read		12	0	312						
37	10013FF313000000FF000000000000	1: Read		13	0	313						
38	30000FFB96000000FF000000000000	3: Refresh		00	1	396						
39	2D121FFB970000D1FF0000D1000000	2: Book	D1	21	1	397			D1			
40	2D222FFB970000D2FF0000D2000000	2: Book	D2	22	1	397			D2			

Addressed Bin

Neighboring Bin

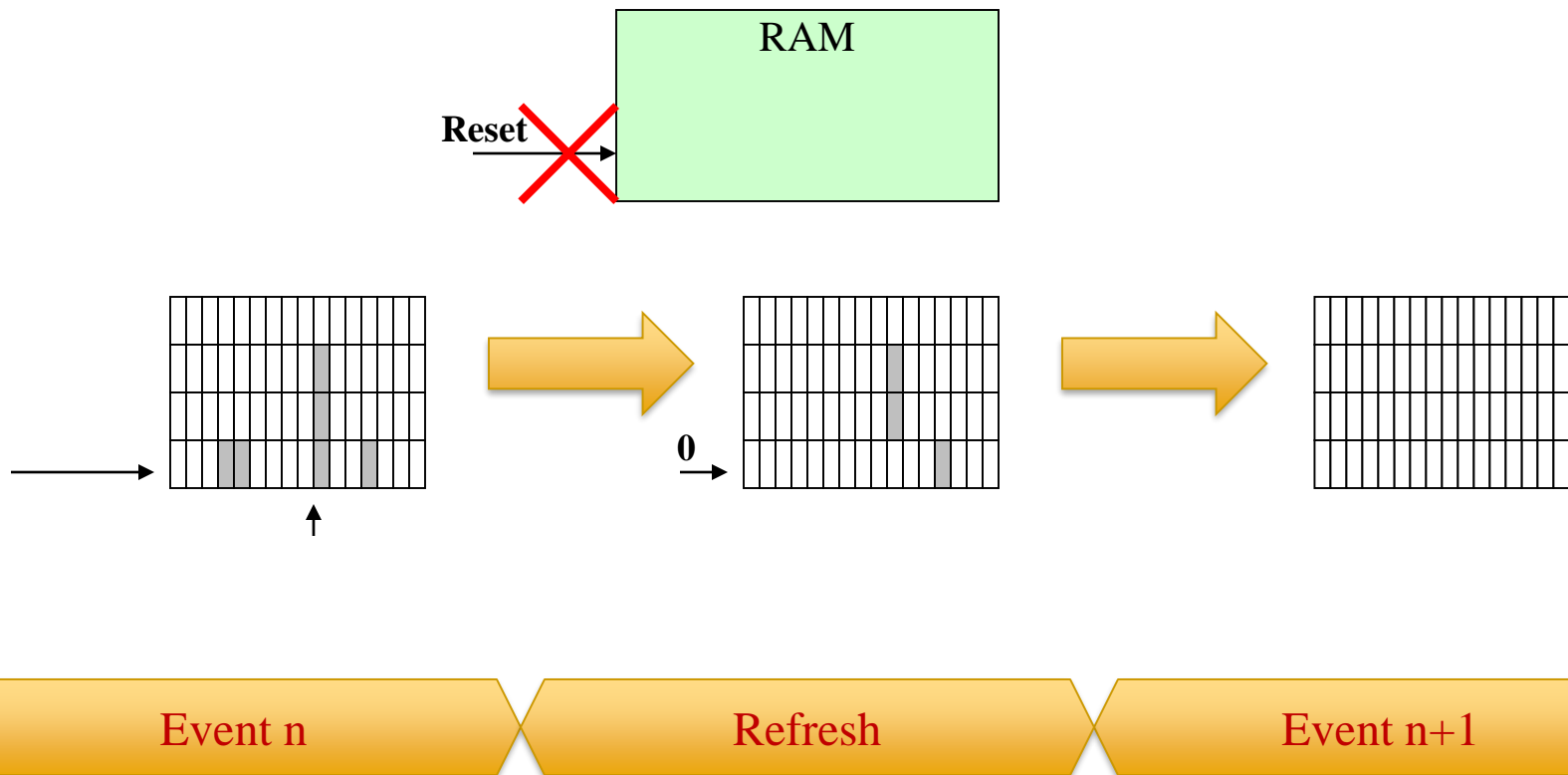


# Fast Refresh between Events



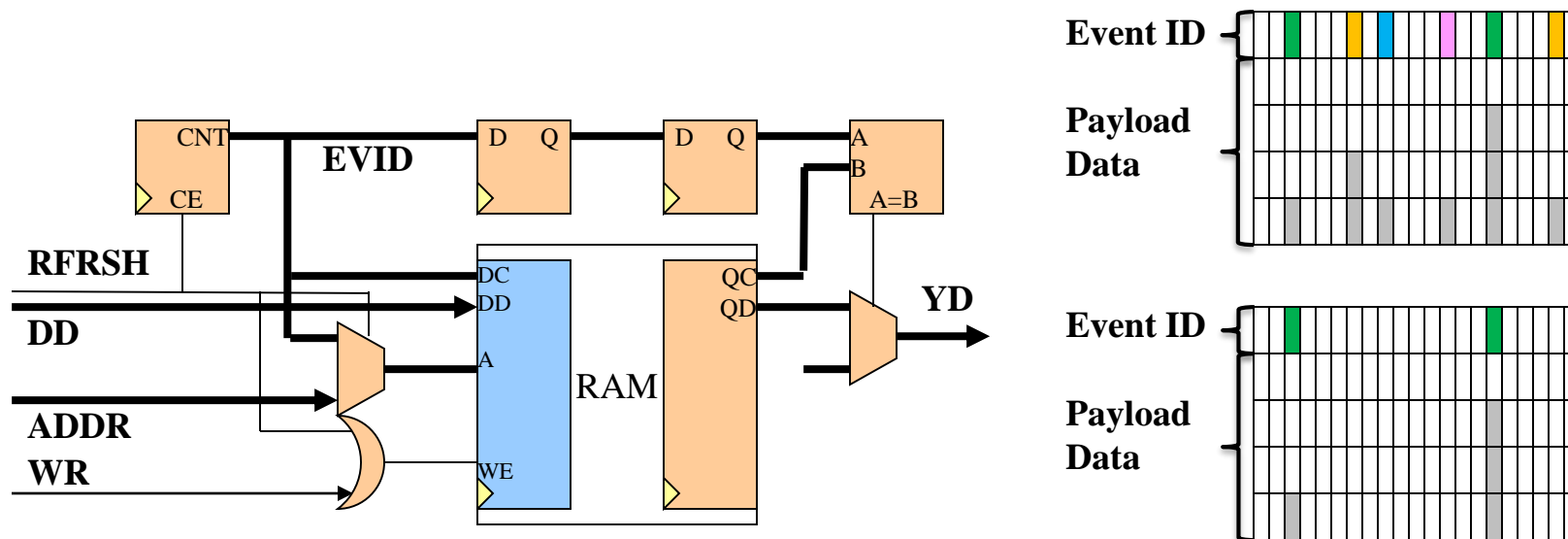
- The buffer operates event by event.
- It is desirable to refresh the buffer, i.e., to clean up the contents, between two events.
- The refreshing process should be as fast as possible, ideally in single clock cycle.

# Typical Refreshing Process



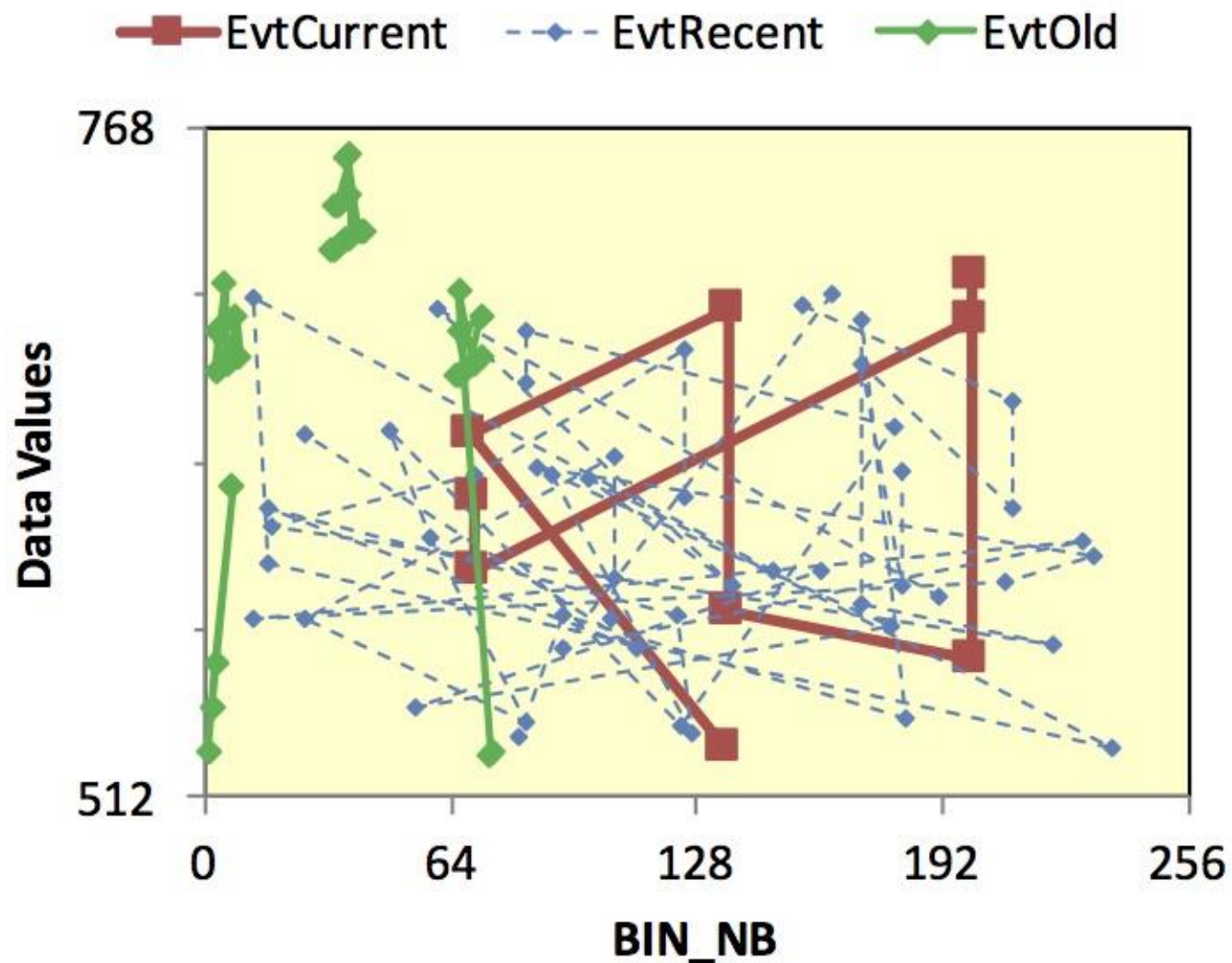
- The regular RAM devices are not resettable globally.
- In order to refresh a memory buffer for next event, all locations are to be written with 0.
- The process takes many clock cycles.

# Global Refresh Scheme



- An event ID counter **EVID** is kept and is written into **RAM** along with **Payload Data**.
- The refreshing takes a single clock cycle to increase **EVID** (i.e., **EVID++**).
- During readout, the **EVID** is checked to validate the output data.

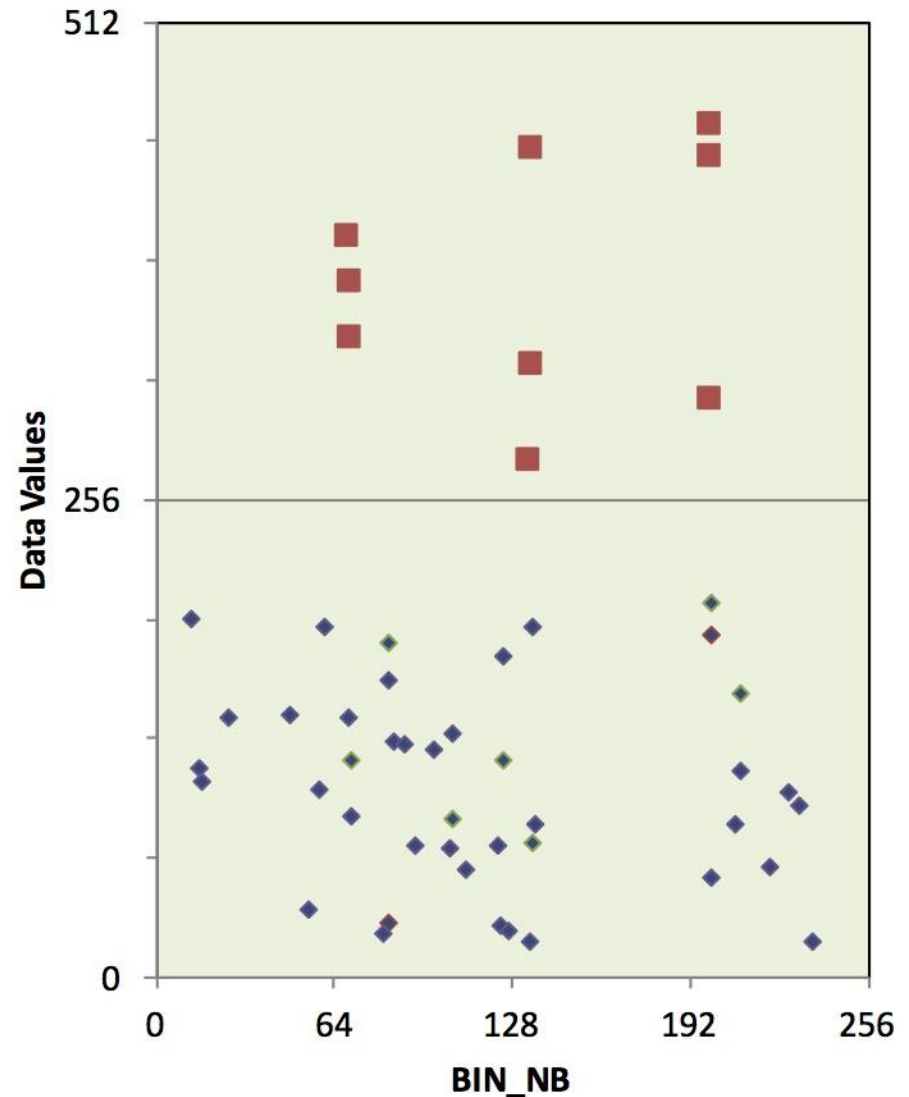
# Test: Events



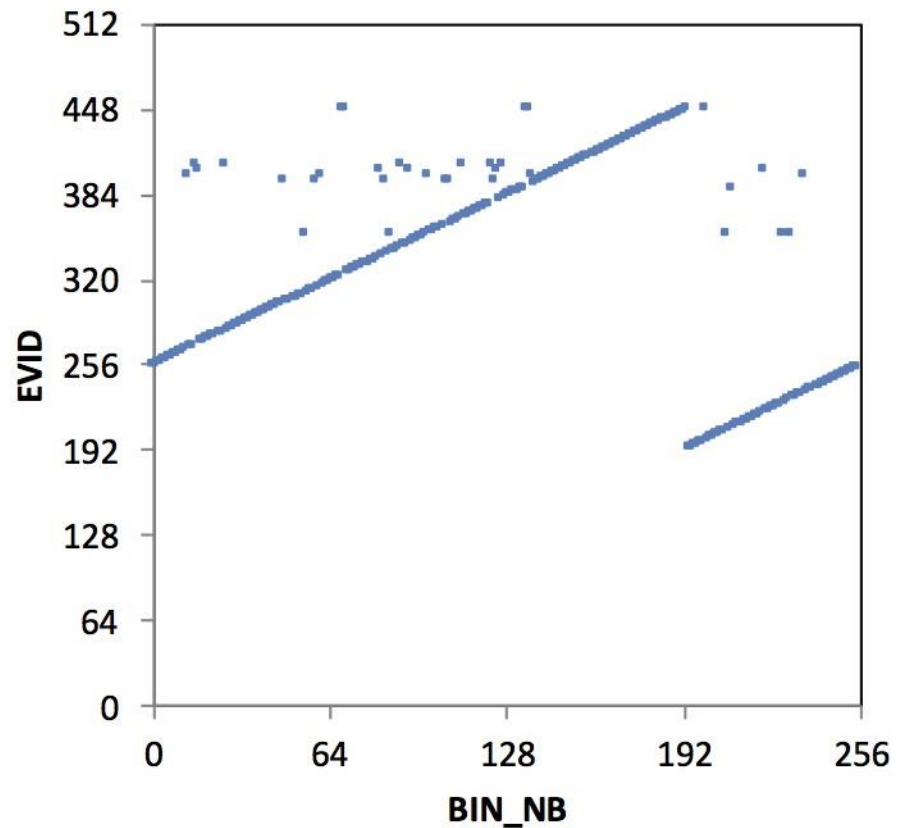
- Several data points are written into the memory in each event.
- In general, there are multiple old events exist in the memory.

# Identifying the Current Event

- The data points of the current event are recognizable from the accompanying event ID.
- Memory bins with old event ID are treated as empty.



# Event ID



- In each refreshing process, one bin is cleared.
- This will prevent EVID from rolling over.
- (The actual operation is to overwrite the EVID field with the previous event number.)

# Summary

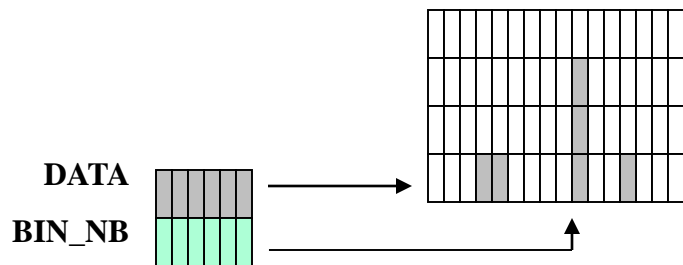
- The block RAM operates as if it is a register. It supports:
  - Single clock cycle booking
  - Single clock cycle reading
  - Single clock cycle refreshing
- Boundary coverage is supported.
- It operated in Cyclone V at 250 MHz and is portable to other FPGA families.

The End

Thanks

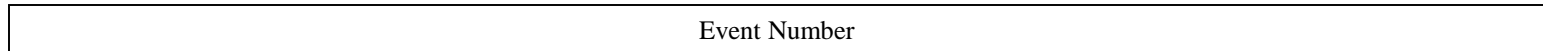
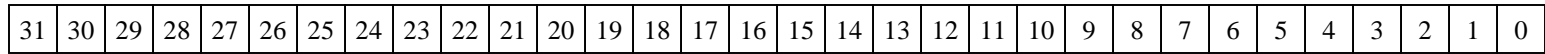


# Block RAM in Trigger System



- The RAM is organized in bins.
- Hit data arrives along with bin numbers (e.g., hit coordinates).
- Hit data are stored in corresponding bins.
- Each bin may store multiple hits.
- Hits in each bin are read out for fitting once addressed.

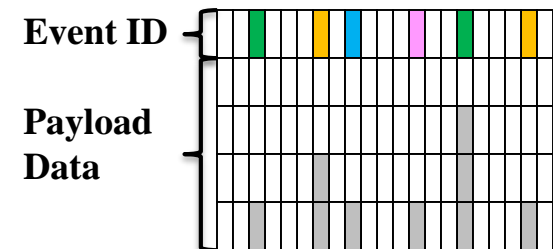
# Event ID Rollover Issue



**8-bit EVID: Rolling Over every 256 events**



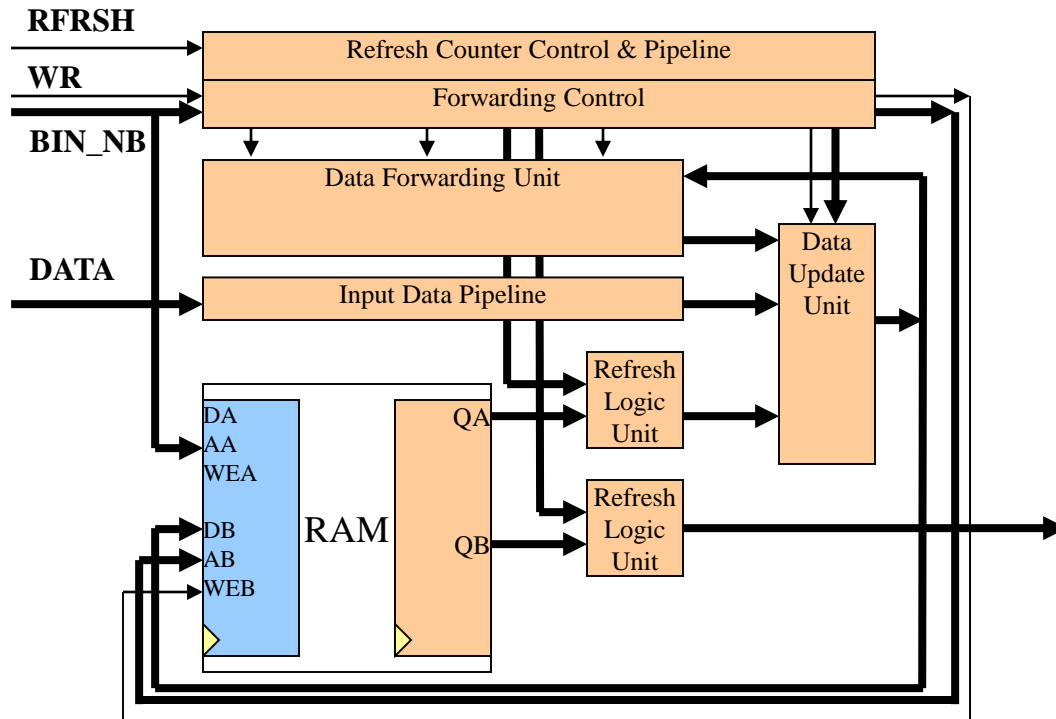
**16-bit EVID: Rolling Over every 64K events**



- With finite number of bits storing the EVID, the counter will roll over.
- The data from old events may be viewed as new.

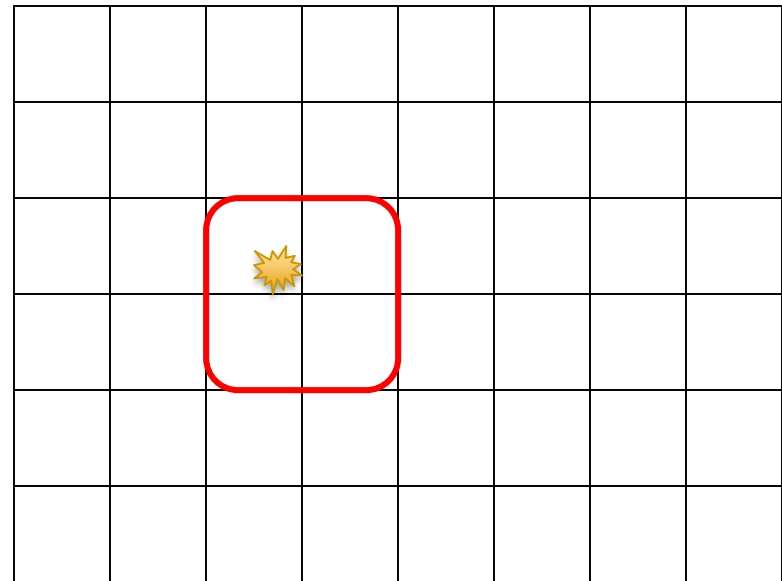
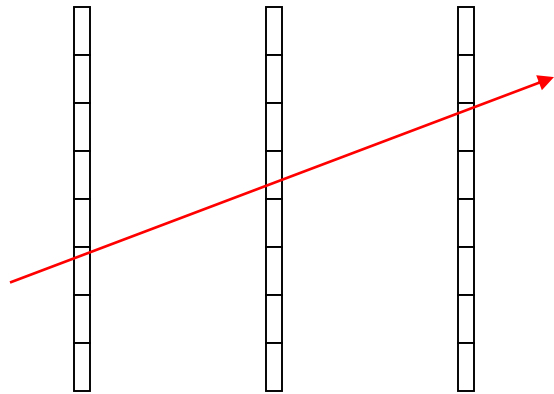


# Data Forwarding Scheme



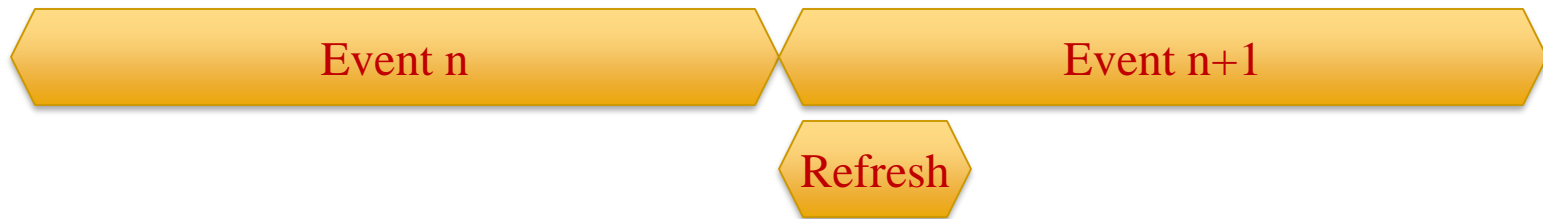
- A data forwarding unit is used to eliminate the RAW hazard.
- The data forwarding is a scheme transplanted from micro-processor design method.

# Future Improvement (1) Boundary Coverage



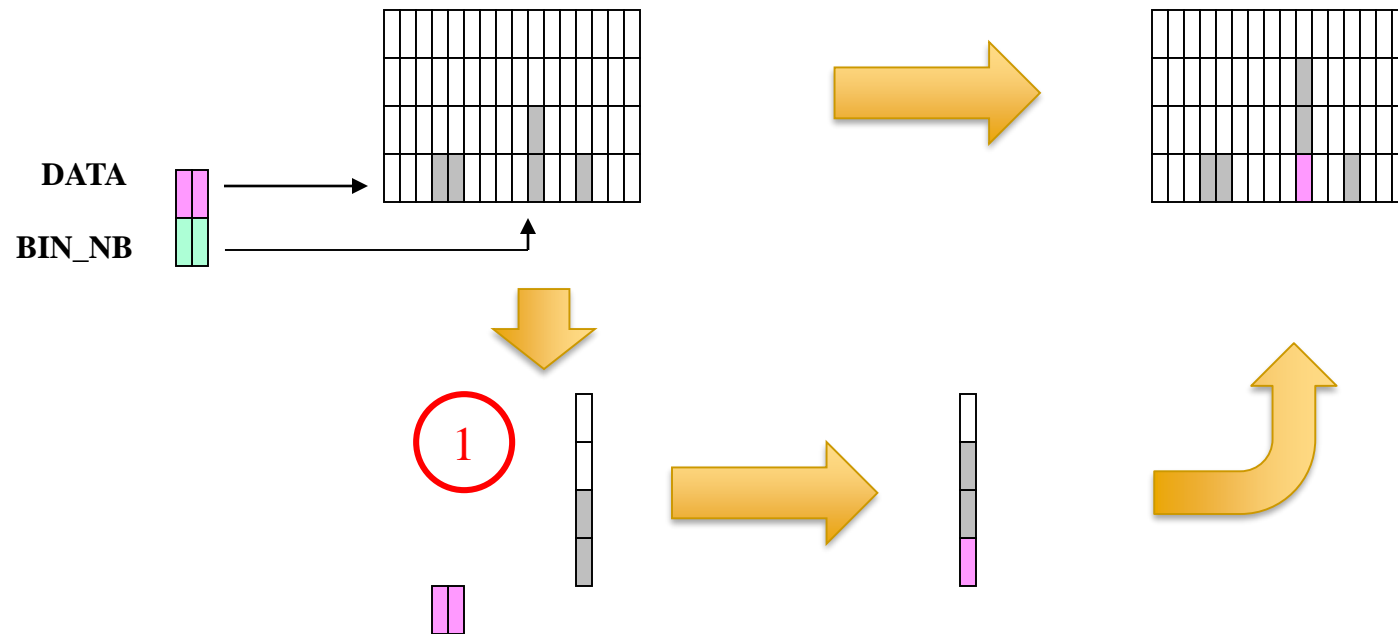
- For each detector layer, once a bin is addressed, the actual hit data may be found in up to 4 bins to ensure correct boundary coverage.

## Future Improvement (2) Hidden Refreshing Process



- The refreshing process can be hidden during the event transition.
- Totally no dead time between two events.

# Read-after-Write (RAW) Hazard



- If the same bin is to be booked in two adjacent clock cycles, a read-after-write (RAW) hazard will occur.
- When the second data arrives, the bin has not been updated by the first data.