Contribution ID: **582** Type: **Oral presentation**

Development of a multichannel FPGA based high resolution Time-to-Digital Converter

Friday 15 June 2018 12:10 (20 minutes)

Time-of-Flight measurement is a powerful tool to distinguish particles in nuclear and hadron physics experiments. For such purpose, a low cost, multichannel and high resolution of better than 30 ps time to digital converter (TDC) is needed. In this work, a multichannel TDC is implemented in Xilinx Kintex-7 (XC7K160T-1).
The TDC employs tapped delay line (TDL) for fine time measurement. Each TDL is composed of a carry chain with 160 taps and measures both leading edge and trailing edge at sampling frequency of 625 MHz. The dead time of the measurement is 2 cycles of the sampling frequency (i.e. 3.2 ns). Auto calibration logic of the bin width is implemented with cascaded PLL and block RAM. The typical bin width is 11 ps. The measurement range is extended by a clock count based coarse time measurement up to 100 us. Time window matching sequence selects a valid hits in the specified time window. For data readout, 1 Gbps TCP/IP protocol based on SiTCP is used. The firmware is implemented with Vivado 2017.4 for a demostrator module. The detail of the firmware design including floor planning and performance test will be presented.

Minioral

Yes

Description

FPGA-TDC

Speaker

Takahashi Tomonori

Institute

Osaka University

Country

Japan

Author: TAKAHASHI, Tomonori (RIKEN)

Presenter: TAKAHASHI, Tomonori (RIKEN)

Session Classification: Front End Fast Detectors 2