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Accurate Synchronization of Multichannel Acquisition for Field Digitizer Modules at CSNS-WNS

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The under-construction White Neutron Source at China Spallation Neutron Source (so-called Back-n) is a facility for nuclear data measurements which has planned seven spectrometers. As the different of physical objectives, the requirements for readout electronics of each spectrometer differs from each other. To accommodate the variety of detectors, the general-purpose readout electronics with a unified structure has been proposed and applied to all spectrometers at Back-n, in which a field digitizer module (FDM) with two digitizing channels has been designed to obtain the full waveform data. In this paper, an accurate synchronous acquisition approach for multi FDMs is introduced. The trigger and clock module (TCM) in the general-purpose readout electronics synchronously fans out clock (125MHz) and trigger signals to each FDM channel separately through the dedicated differential star buses on the PXIe backplane. In FDM, a dual-loop PLL referenced by this synchronous clock generates a higher frequency clock (1GHz) as the digitizer sampling clock. After being divided by the sampling clock, the digitizer data clock (250MHz) is fed into a field programmable gate array (FPGA) for high speed data receiving and further as the global clock for FPGA firmware. To compensate the sampling offset caused by the skew discrepancy of digitizer clock, a FPGA-based TDC is implemented to accurately measure the time interval between the rising edge of global clock received at the FPGA and the global synchronous trigger signal. Test result shows that the synchronization performance of the multi-channel acquisition meets requirements.

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