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A 5.5 ps Time-interval RMS Precision Time-to-Digital Converter Implemented in Intel Arria 10 FPGA

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As an important part of the field programmable gate array (FPGA) market, Intel FPGA has also great potential for implementation of time-to-digital converter (TDC). In this paper, the basic tapped delay line (TDL) TDC structure is adapted in Intel Arria 10 FPGA, which is manufactured with 20 nm process technology. Because of the serious bubble problem for FPGA made by state-of-art process, the ones counter encoding scheme is employed to maintain the delay elements in TDL resolvable for achieving high TDC time precision. The test of TDC bin width reveals that the characteristics of the delay chain are highly consistent with the fundamental structure of logic resource in the FPGA. To improve TDC time precision, four TDLs are combined parallel for final TDC implementation. Using two identical TDC channels, the average RMS precision for measurements of time-intervals in the range from 0 to 50 ns reaches 5.45 ps. The test results demonstrate that high performance TDC can be implemented in current Intel main-stream FPGAs as well.

Minioral

Yes

Description

FPGA-TDC

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