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The Design and Test of LAr Trigger Digitizer Board in ATLAS Phase-I Upgrade

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The LHC upgrade is planned to enhance the instantaneous luminosity to 2-3×1034 cm-2s-1 during Run 3 from 2021 through 2023. The Phase-I upgrade of the trigger readout electronics for the ATLAS Liquid Argon (LAr) Calorimeters will be installed during the second long shutdown of LHC in 2019/2020. In this upgrade, so-called Supercells are introduced to provide higher granularity, higher resolution and longitudinal shower shape information from the LAr calorimeters to the Level-1 trigger processors. A new LAr Trigger Digitizer Boards (LTDB) will process and digitize 320 channels of Supercell signals, and transmit it to the back-end processors via 40 fiber optical links where data are further processed and transmitted to the trigger processors. Five pairs of bidirectional GBT links are used for slow control. LTDB also sends 64 summed analog signals to the Tower Builder Board through the baseplane, to maintain the present analog L1 trigger functionality as a possible backup system.
A test system is developed to test all functions of LTDB and perform the performance measurement. A back end PCIe card is designed which has the interface to the ATLAS TTC system. It can control the generation of injection signals to the LTDB for performance test. It can also communicate with the GBTx, and all ASICs on LTDB via GBT-SCA (Slow Control Adapter) through fiber optical links. A front-end test board, test baseplane and a crate will be designed to extend the capability of the test setup, which will be used for the production test of 124 LTDBs.

Minioral

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Description

LAr Trigger

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