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Pulsar3a: Next Generation ATCA Full Mesh General Purpose FPGA Based Processing Board

Tuesday 12 June 2018 10:10 (20 minutes)

In this talk we present the Pulsar3a, our next generation full mesh enabled FPGA-based ATCA processing board. Originally motivated by silicon-based tracking trigger needs for HL-LHC experiments, the Pulsar3a is designed with the goal of creating a scalable architecture abundant in flexible, non-blocking, high bandwidth interconnections. Based on Xilinx Ultrascale FPGAs, the Pulsar3a represents a significant step up from the Pulsar2b board in terms of logic resources (693k to 5M logic cells), I/O channels (40 to 96 serial transceivers) and I/O bandwidth (1 to 2 Tbps). Significant redesign of this board was necessary to address the challenges associated with increasing the I/O channel density and bandwidth. For example, the fiber optic transceivers have been relocated from the rear transition module to the front board and positioned near the FPGAs. Moving the optics inboard dramatically shortens the traces between the FPGA and optical transceivers and the Zone-3 connector bottleneck has been avoided completely; this change was necessary to achieve the stringent signal integrity performance required as data transmission rates approach 25 Gbps. Various hardware subsystems developed for the Pulsar2b, such as the direct connection between the FPGAs and the full mesh ATCA fabric interface and custom IPMC mezzanine, have been retained in the Pulsar3a design. These and many other Pulsar3a design details will be presented with a focus on the common challenges facing ATCA board designers, such as high-speed routing, high bandwidth interconnections, power thermal and related cooling issues, as well as the initial prototype performance results.

Minioral

Yes

Description

Next Generation

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