

Development and Characterization of a 3.2 Gb/s Serial Link Transmitter for CMOS Image Sensors

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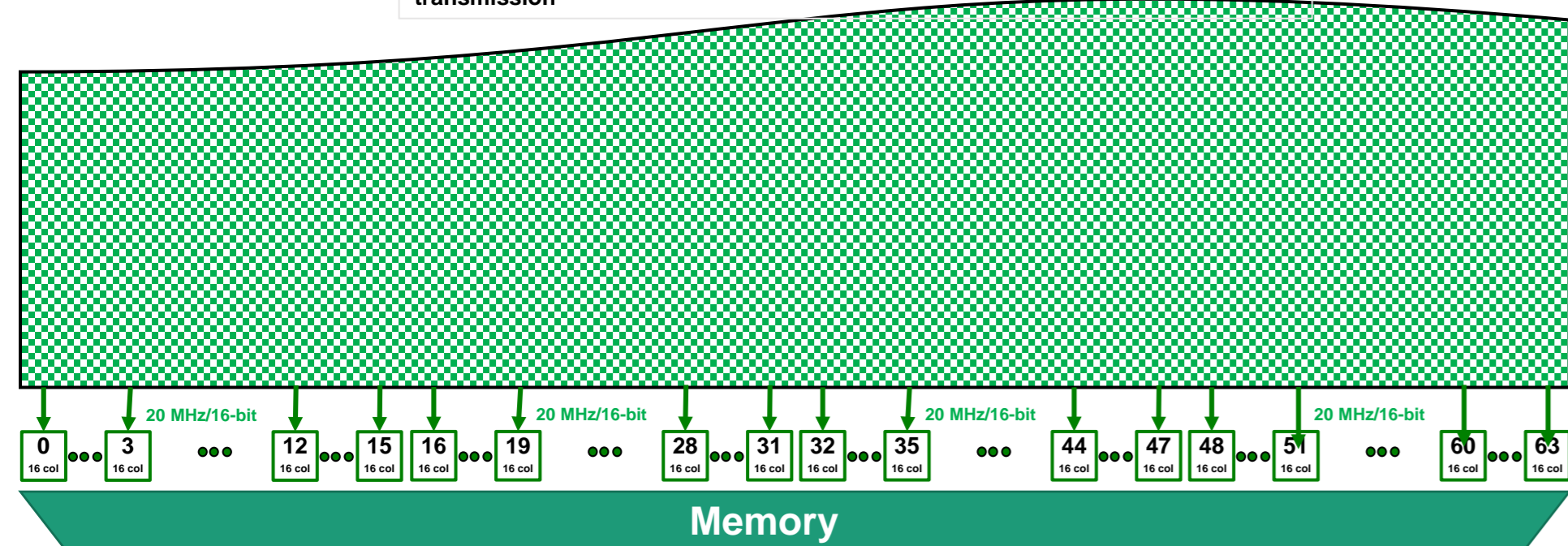
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1. Motivation

- CMOS monolithic active pixel sensors (MAPS) for future subatomic physics experiments require integration of high-speed serial data link due to
 - Increasing hit-density
 - Low material budget
- We developed a 3.2 Gbps serial link transmitter for MAPS application

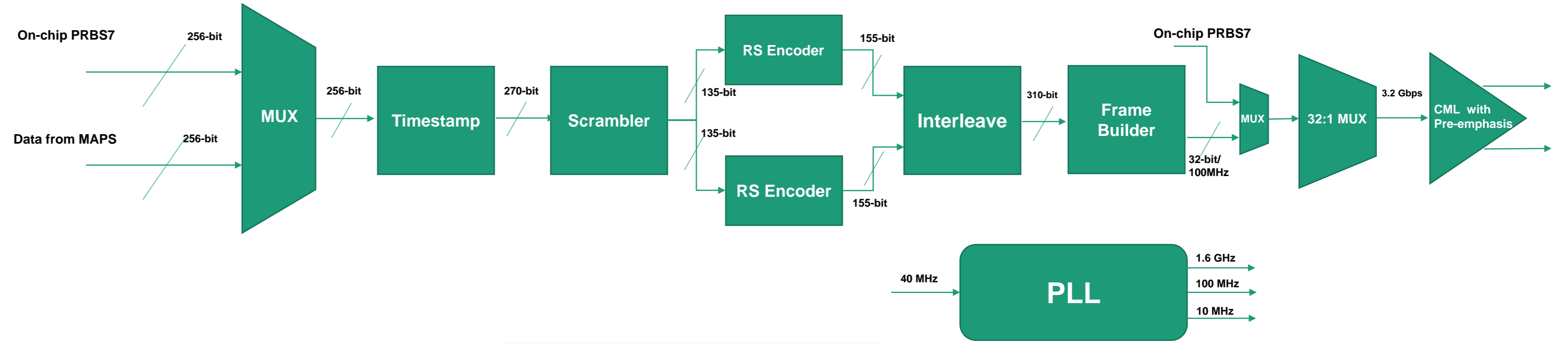
	Current Parallel Data Transmission (8 X 320 Mbps, LVDS)	Serial Data Transmission
Cables	18 (16 of them for data and other 2 for clock)	2
Clock Skew	Yes	No
Error Correction	No error correction	Up to 20 bits in a frame

Comparison between current parallel data transmission and serial link transmission



Conceptual diagram of the application of a serial link transmitter in a MAPS

2. Architecture



Block diagram of the proposed serial link transmitter

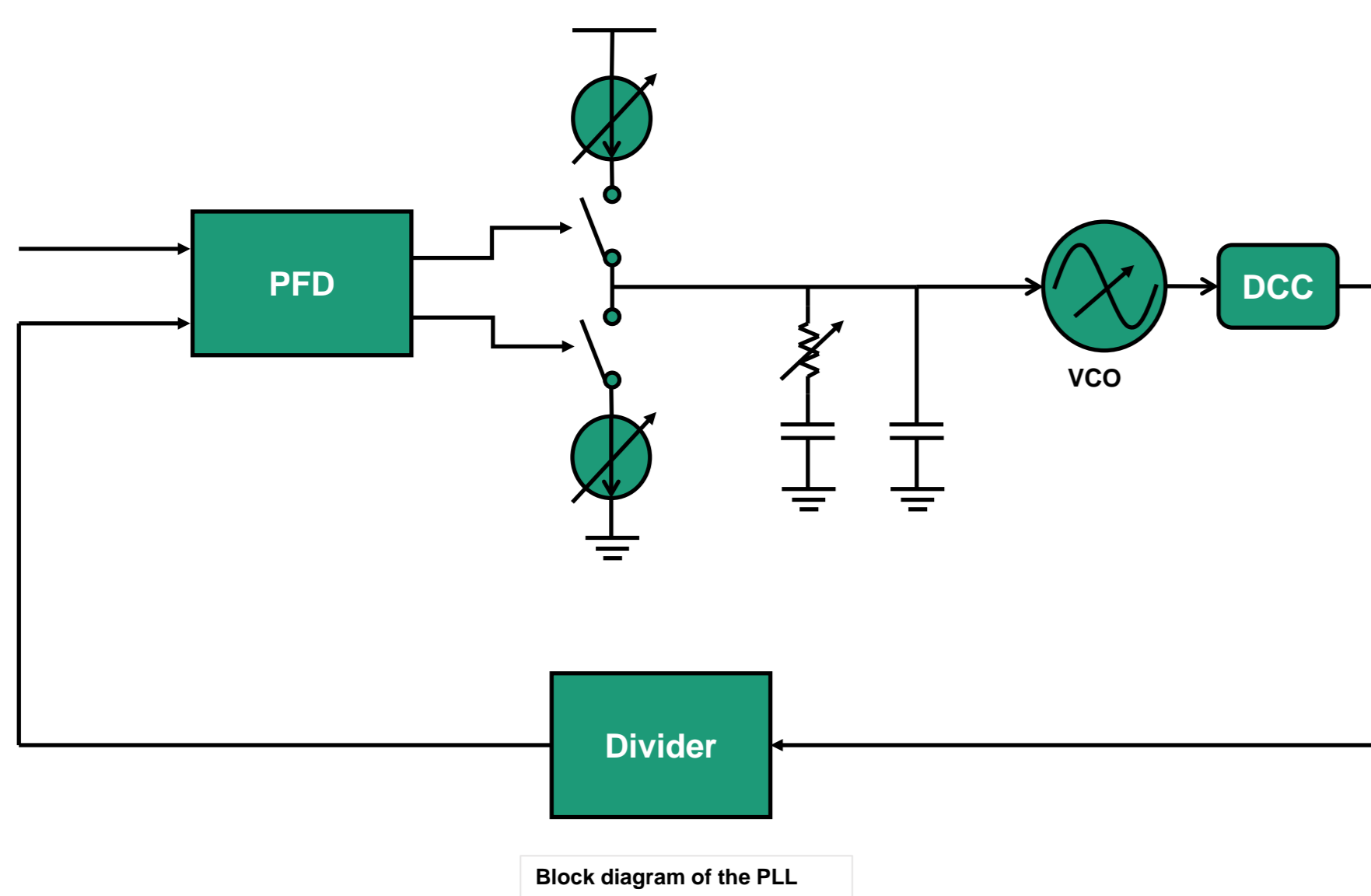
- 256-bit raw data at 10 MHz
- 14-bit timestamp
- Scrambler defined by polynomial $x^{58} + x^{39} + 1$
- Interleaved Reed-Solomon (31,27) FEC encoder, correct burst bits up to 20 bits
- Digital circuits are fully triplicated to tolerate SEU

- Half-rate serialization scheme
- 1.6 GHz clock generated with duty-cycle correction
- 32:1 multiplexer with 5-stage binary-tree structure
- CML driver with 3-tap pre-emphasis
- On-chip PRBS-7 for testability



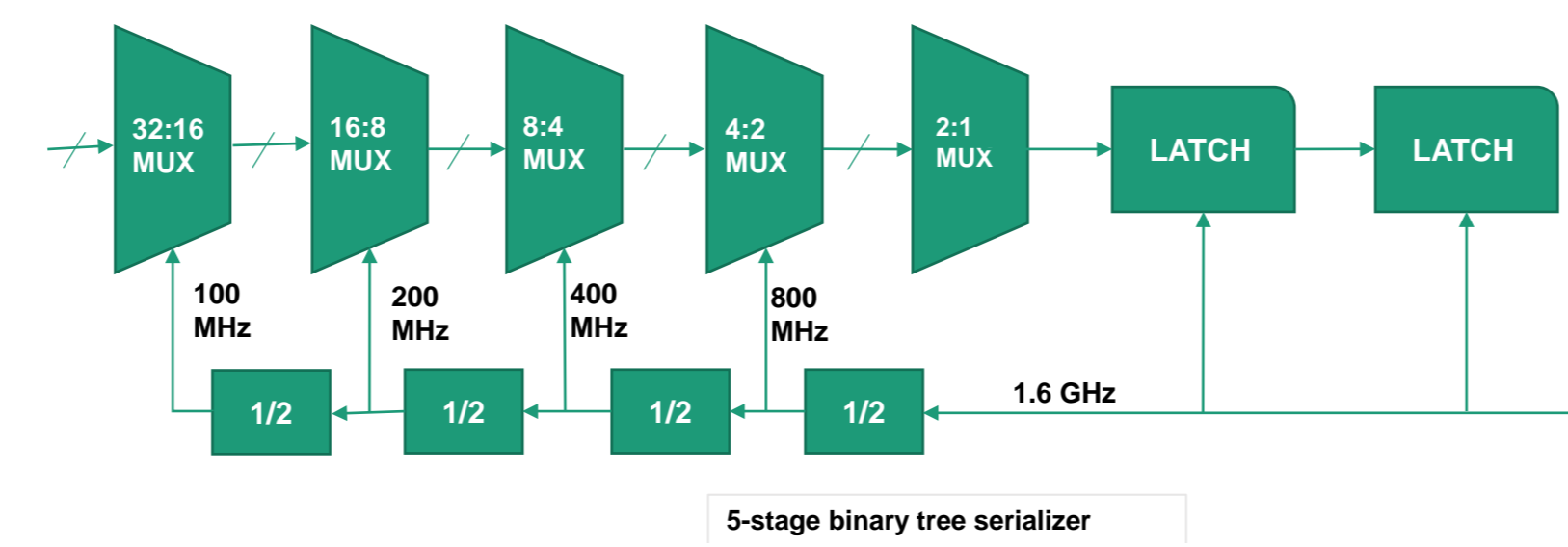
Frame definition

3. The PLL and the serializer

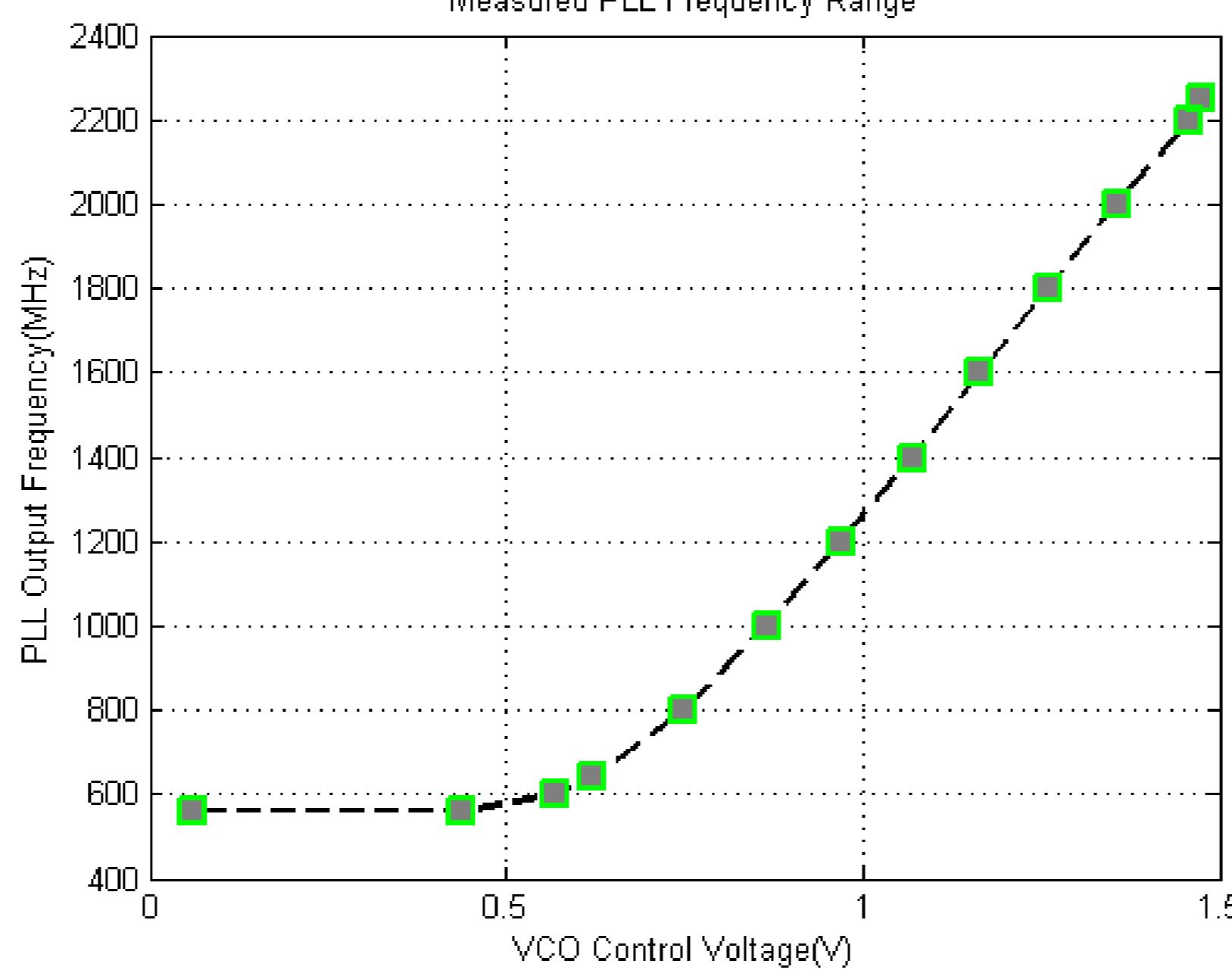


Block diagram of the PLL

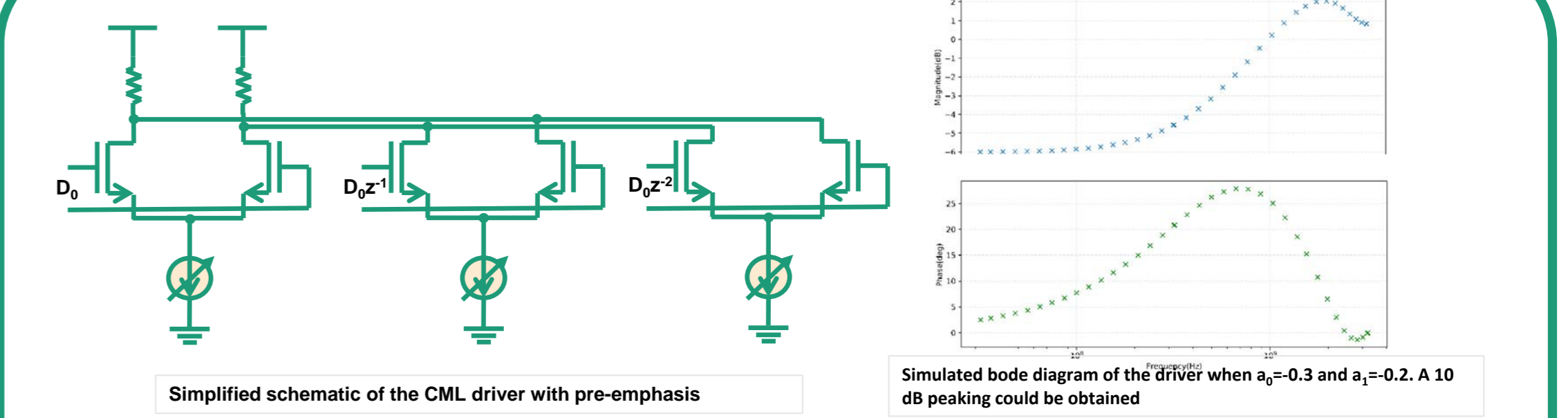
- Charge-pump PLL for clock multiplying by a factor of 40
- Loop bandwidth is programmable to ease in-band noise and out-band noise trade-off
- 4-stage ring voltage-controlled oscillator covers frequency ranging from 0.6 GHz to 2.2 GHz
- Duty-cycle correction circuit minimizes duty-cycle distortion (DCD)
- The divider is fully triplicated to tolerate SEU
- 5-stage binary-tree structure based serializer



5-stage binary tree serializer



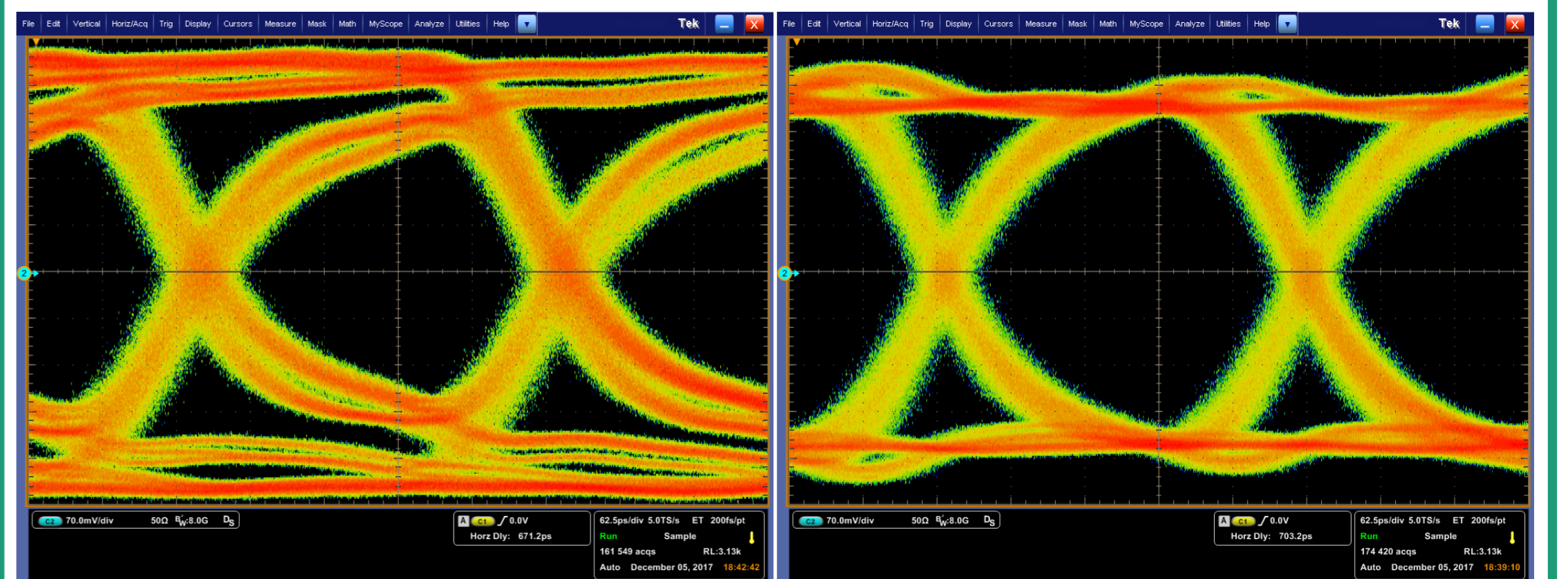
4. The Driver with Pre-emphasis



Simplified schematic of the CML driver with pre-emphasis

Simulated bode diagram of the driver when $a_0=0.3$ and $a_1=0.2$. A 10 dB peaking could be obtained

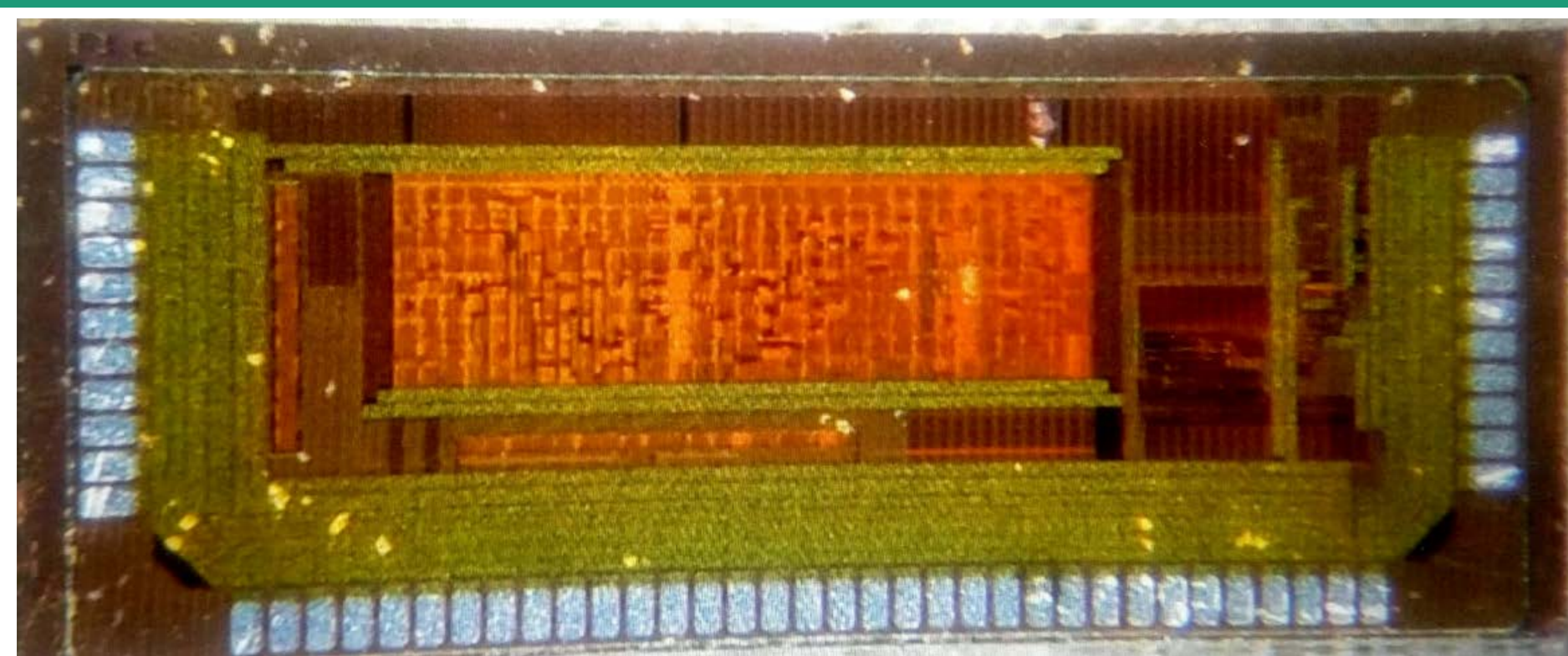
- Pre-emphasis was implemented in the driver because low mass cables are preferred in the system
- Output CML driver realizes programmable 3-tap pre-emphasis
 - Z-domain transfer function $(z^{-1}) = 1_0(1 + a_0z^{-1} + a_1z^{-2})$
- 2 delayed copies of data are generated by the serializer



Measured eye diagram including the on-chip PRBS 7 generator, the serializer, and the driver with a 1.5 meter cable, pre-emphasis off

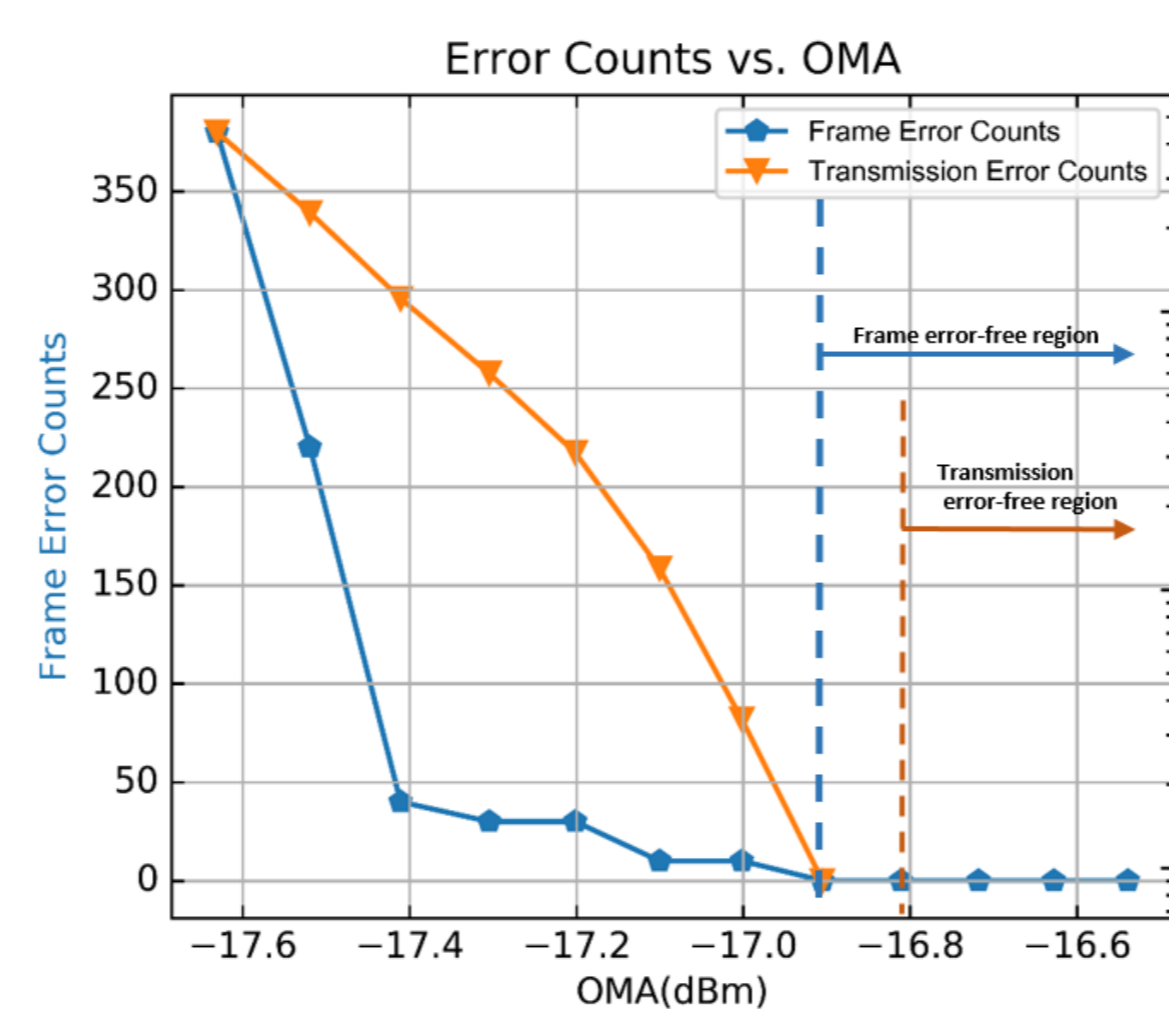
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4. Test Results Summary

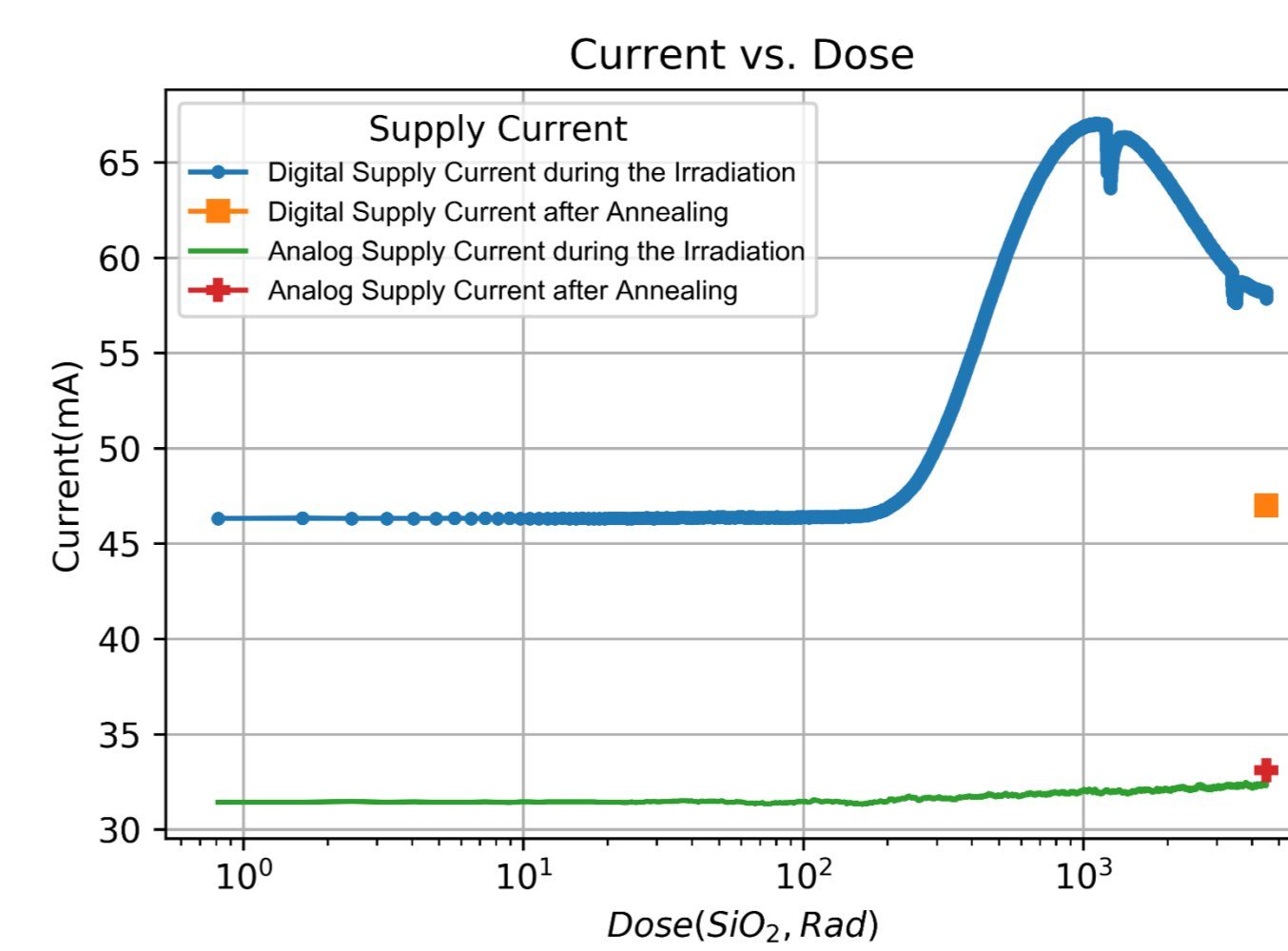


Micrograph of the transmitter prototype chip

- The transmitter was fabricated in TowerJazz 0.18 um CIS process.
- Core area is 2360 um X 760 um.
- The transmitter was directly wire-bonded to a FR-4 PCB for testing.
- A FPGA based receiver was used in the measurement.



- Some transmission errors were deliberately introduced on the transmission path.
- Frame errors with and without the RS decoding were measured.



- The transmitter was irradiated to a TID of 4.5 Mrad (SiO2)
- A peak current consumption on the digital supply at around 1 Mrad
- Current recovered to normal level after 22 hour annealing at room temp.

Jitter Classification	Value
Random (RMS)	3.1 ps
Deterministic (PK-PK)	25.7 ps
Periodic	16.4 ps
Duty Cycle	4.6 ps
Total @ 10^{-12} BER (PK-PK)	60.2 ps

5. Conclusion and outlook

We developed a serial link transmitter is developed aiming to meet the requirement of serial data transmission for MAPS in future subatomic physics experiments. Measurement shows the transmitter sending data at 3.2 Gb/s reliably. Reed-Solomon code provides additional robustness for data transmission. The pre-emphasis in the transmitter allows transmission over low-mass cables. The transmitter is able to withstand TID of up to at least 4.5 MRad.