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Timing and clocking scheme in the upgraded LHCb detector

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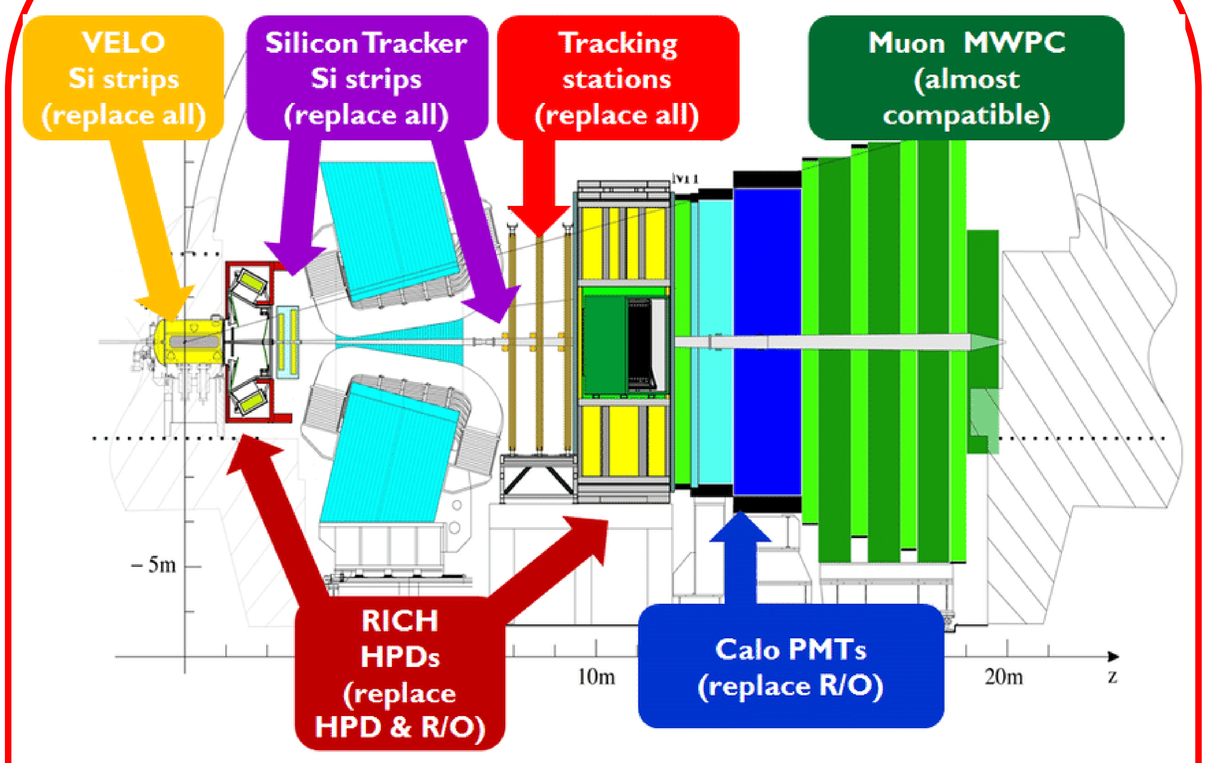
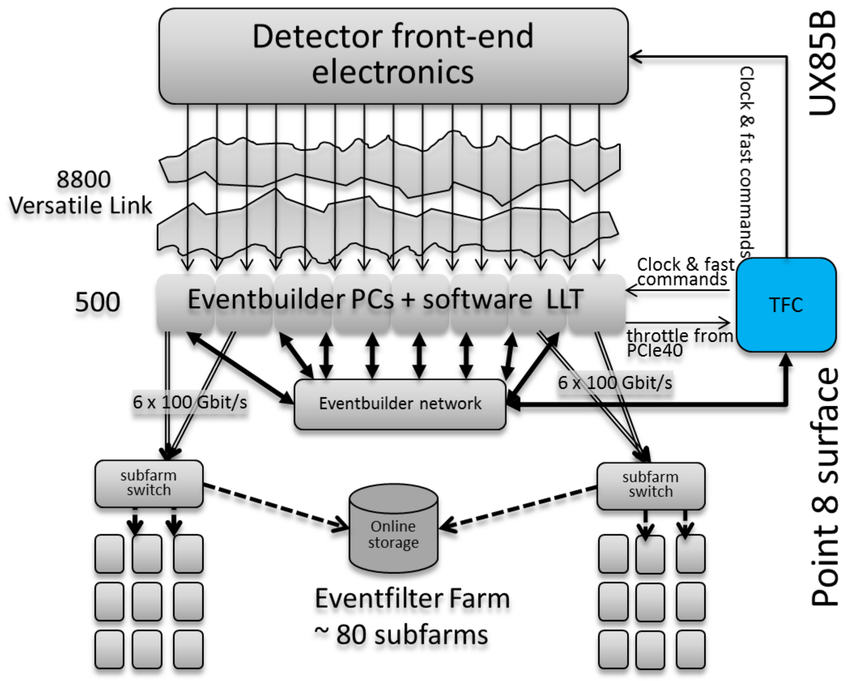
The upgraded LHCb detector



Complex upgrade of the LHCb detector in 2019-2020

- replace all Front-End and Back-End electronics
- replace >90% of the detector channels
- trigger-less data taking at full LHC frequency
- run at x10 more instantaneous luminosity for the next 10 years
- commissioning starting in 2019 and ready by end of 2020
- ~40 Tbps data acquisition system
  - fully flexible and software trigger

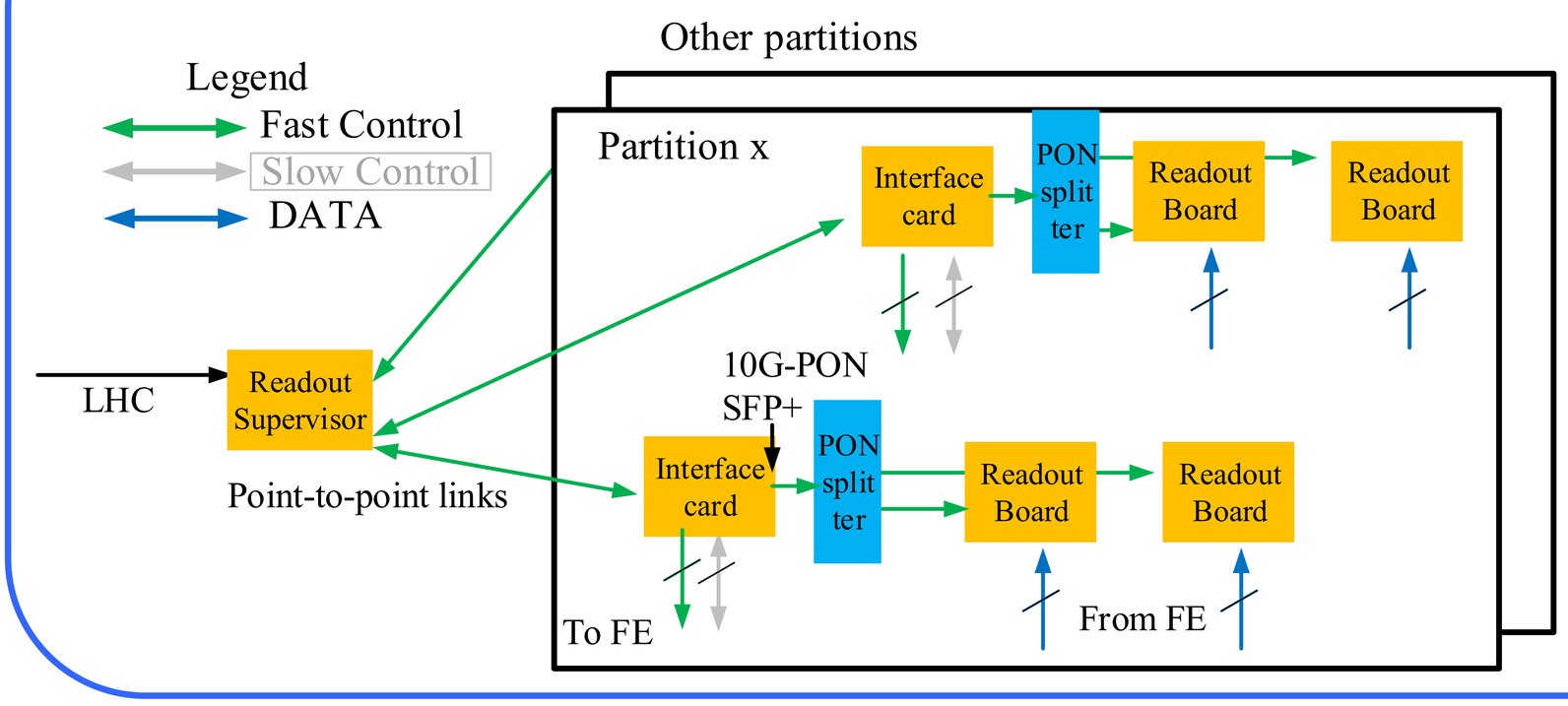
The upgraded LHCb readout system



The upgraded LHCb readout system[1] will be centrally controlled by a single Readout Supervisor, with these functionalities:

- reception and distribution of global timing
- generation and distribution of synchronous and asynchronous commands
- generation of events veto, triggers and calibration events
- interface to central control system for run management, activity configurations and special data taking recipes
  - timestamping and description of events

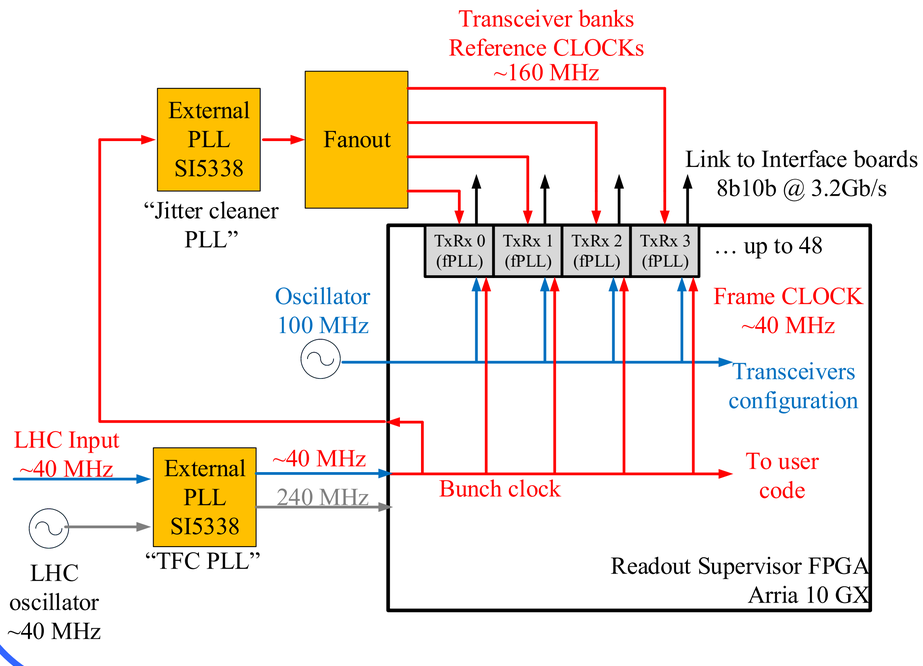
Clock and timing distribution

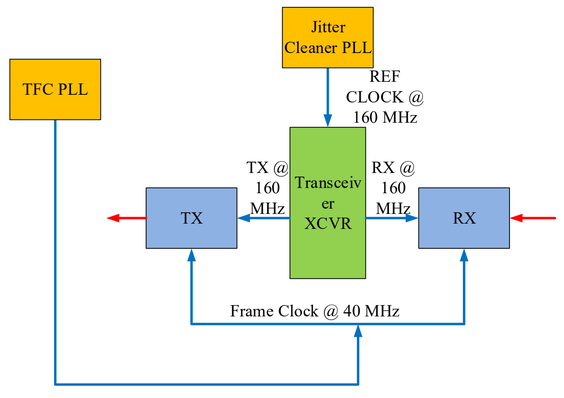


Centrally manager by TFC system:

- Respect partitioning of sub-detectors
- Scalability in case of expanding the system
  - ⇒ Point-to-point to Front-End
  - ⇒ Optical splitter to Readout Boards
- Flexibility in the usage of the hardware
  - ⇒ 10G-PON SFP+ as Tx/Rx medium
  - ⇒ Common LHCb hardware backbone[2]
- Possibility of profiting from the uplink as well
- Interface to the LHC clock
- Fixed latency commands distribution
- Deterministic and reproducible clock phase

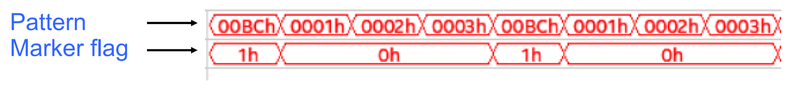
Readout Supervisor clock tree



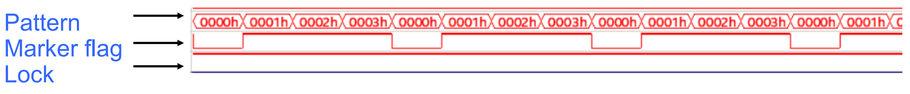


Synchronization between Master and Slave using a specific pattern (classic K28.5)

Transmitter side —> input to TX transceiver



Receiver side —> output from RX transceiver



- Usage of external PLLs: cleaning and proper frequency generator
- Point-to-point links to Interface Boards
- Same clock used everywhere : fan-out for distribution to individual transceivers
- Marker edge to identify main Master clock edge
- Simple usage of commercial FPGA (Altera) available features

References:
[1] K. Wyllie et al, "Electronics Architecture for the LHCb Upgrade", LHCb-PUB-2011-011, 2011
[2] J-P. Cachemiche, P-Y. Duval, R. Le Gac, F. Hachon, F. Rethore, "The PCIe-based readout system for the LHCb experiment", HAL id: in2p3-01258850