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DepFET Movie Chip (DMC) - enabling ultra high speed mega pixel full frame data acquisition for the DepFET direct electron detector (EDET DH80K) system

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Based on the technology of the pixel detector (PXD) at the Belle II experiment @KEK/Japan a direct electron detector system was developed for time-resolved imaging applications. It consists of four two-side buttable all silicon modules (512x512 pixels each) capable to capture full frame images in a burst mode with up to 100 pictures @80k frame rate.

To realize the necessary 26Mbit memory for the local frame storage array and the sequencer memories under the tight space conditions a TSMC 40nm technology was chosen.

To send out the captured picture data sets to the following DAQ, up to 8 middle speed serial links and a cross bar switch like routing structure are implemented.

Selected sub-circuits, as the PLL, a fine grained delay unit and the SRAM IP integration were already successfully verified with a test chip manufactured via an Europractice miniasic run in the same technology.

The DMC is fully controllable via a standard JTAG interface, where all configuration registers are implemented as JTAG chain extensions and well described in a standard conform extended Boundary Scan Description Language (BDSL) file. The python based test-bench preparation includes serial vector file (SVF) format generation based on this BSDL file and a small sequencer compiler. With these a digital full system verification of the all silicon module was performed to check the system behavior before the final submission.

Minioral

Yes

Description

chip, image collection

Speaker

Andreas Wassatsch

Institute

MPI

Country

Author: Dr WASSATSCH, Andreas (Semiconductor Laboratory of the Max Planck Society (HLL))

 $\textbf{Co-authors:} \quad \text{KOFFMANE, Christian (MPI für Physik);} \quad \text{Dr PRINKER, Eduard (Semiconductor Laboratory of the authors)} \\$

Max Planck Society (HLL))

Presenter: Dr WASSATSCH, Andreas (Semiconductor Laboratory of the Max Planck Society (HLL))

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