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An FPGA based high speed network processor - Preprocessing detector images relieving data backend systems

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At the Paul Scherrer Institut several types of X-ray detectors are being developed. All of them have in common that they use network interfaces to transmit the images to a server for processing and storage.

One, concerning data rate, especially demanding detector is Eiger.

It is module based with 512x1024 pixels and two 10Gbit/s Ethernet connections per module. Since all modules are operated parallel the data rate scales with the size of the detector. So a 1 Megapixel detector with its two modules has four 10 Gbit/s ports and a 9 Megapixel detector with 18 modules 36 10 Gbit/s ports. Since every module can easily saturate the two 10Gb/s Ethernet ports, powerful servers are necessary to receive and sort the arriving network packets.

The current available Xilinx Virtex Ultrascale FPGAs have up to 60 30.5Gb/s GTY transceivers. They are suitable for PCIe and Ethernet connections because of their integrated have a PCIe Gen3 and 100Gb/s Ethernet MAC hard cores.

To unload the host CPU an FPGA design using the MAC and PCIe core in the FPGA has been created.

It receives the network packets and reassembles the images in the host memory via PCIe. To do so the network packets are analysed and destination memory address are generated in the FPGA. Finally an interrupt is triggered.

We present the FPGA design as well as first results from a prototype system.

Minioral

Yes

Description

image processing

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