Contribution ID: **397**   Type: **Poster presentation**

Design of 32-channel TDC Based on Single FPGA for µSR Spectrometer at CSNS

Thursday 14 June 2018 15:50 (15 minutes)

Muon Spin Rotation, Relaxation and Resonance (uSR) technology has an irreplaceable role in studying the microstructure and properties of materials, especially micro-magnetic properties. An experimental muon source is being built in China Spallation Neutron Source (CSNS) now. At the same time, a 128-channel uSR spectrometer as China's first uSR spectrometer is being developed. The time spectrum of uSR can be obtained by fitting the curve of positron count rate with time. This paper presents a 32-channel Time-to-Digital Converter (TDC) implemented in a Xilinx Virtex-6 Field Programmable Gate Array (FPGA) for measuring the positron's flight time of µSR Spectrometer. Signal of each channel is sampled by 16 equidistant shifted-phase 200 MHz sampling clocks, so the TDC bin size is 312.5ps. The measuring range is up to 327us. This TDC has the ability to store multiple hit signals in a short time with a deep hit-buffer up to 512. Time tag is added to each data to record the moment when the data was detected. Programmable time window and channel shielding give the flexibility to choose the time range and channels of interest. The delay of each channel can be calibrated. The data is transmitted to data acquisition system (DAQ) through Gigabit Ethernet. TDC and control logic are configured in real time by DAQ. The results of test show that the Full Width at Half Maximum (FWHM) precision of single channel is better than 273 ps with a low sensitivity to temperature and the linearity is pretty well.

Minioral

Yes

Description

FPGA-TDC

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Session Classification: Poster 2

Track Classification: Front End Electronics and Fast Digitizers