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Implementation of a High-Performance Pattern Recognition Associative Memory in an FPGA

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Pattern recognition associative memory (PRAM) devices are parallel processing engines which are used to tackle the complex combinatorics of track finding algorithms, particularly for silicon based tracking triggers. PRAM development has been mostly limited to the realm of ASICs, which often leads to lengthy and expensive design cycles. FPGAs allow for quick iterations, making them an ideal hardware platform for designing and evaluating new PRAM features before committing to silicon. The FPGA implementation of PRAMs is also highly desirable for early performance studies; for example, it can bring system interface to maturity much sooner and minimize the number of ASIC design cycles. In this talk we present our new PRAM designs and discuss how logic blocks which were originally developed for ASICs are redesigned to take advantage of modern FPGA architectures to increase both speed and pattern density.

Minioral

Yes

Description

Pattern Recognition

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