Contribution ID: **565** Type: **Oral presentation**

Vertical Slice System Demonstration of a Tracking Trigger using an Associative Memory Approach

Monday 11 June 2018 13:40 (20 minutes)

It has become evident that the development of a Level 1 tracking trigger system is crucial for the success of the HL-LHC physics program at the CMS experiment. The high pile-up and high occupancy conditions anticipate an input data rate into the tracking trigger system of ˜100 Tbps. This, combined with the 4 s latency required the L1 track finding trigger stage introduce an unprecedented set of challenges requiring the most advanced real time processing technology. A silicon-based Level 1 tracking trigger system has never been realized under these conditions., It is therefore mandatory to demonstrate its feasibility at the system level. Recently, the HEP community has made significant progress in the area of fast track finding using ASICs and FPGAs. This includes a successful vertical-slice demonstration for a CMS tracking trigger at Level 1 for the HL-LHC era, developed by a Fermilab/LPC R&D collaboration. The demonstration solves the data delivery problematic using an ATCA, full-mesh based, system architecture. It uses a fast pattern recognition algorithm, based on associative memories, that can be implemented on specialized ASICs, or on modern FPGAs when the pattern bank size needed is not very large, followed by precision track fitting implemented on dedicated FPGAs. The demonstration system achieved excellent performance in terms of tracking efficiency and momentum resolution, within a very short latency (2.5 s). The details of the demonstration will be presented, with highlights on the new techniques developed to address the unique challenges at the chip, board, and system level.

Minioral

Yes

Description

Tracking, AM

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Session Classification: Large Experiments 3