APA integration test for the ProtoDUNE-SP LAr TPC at CERN

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On behalf of the cold electronics team
Brookhaven National Laboratory

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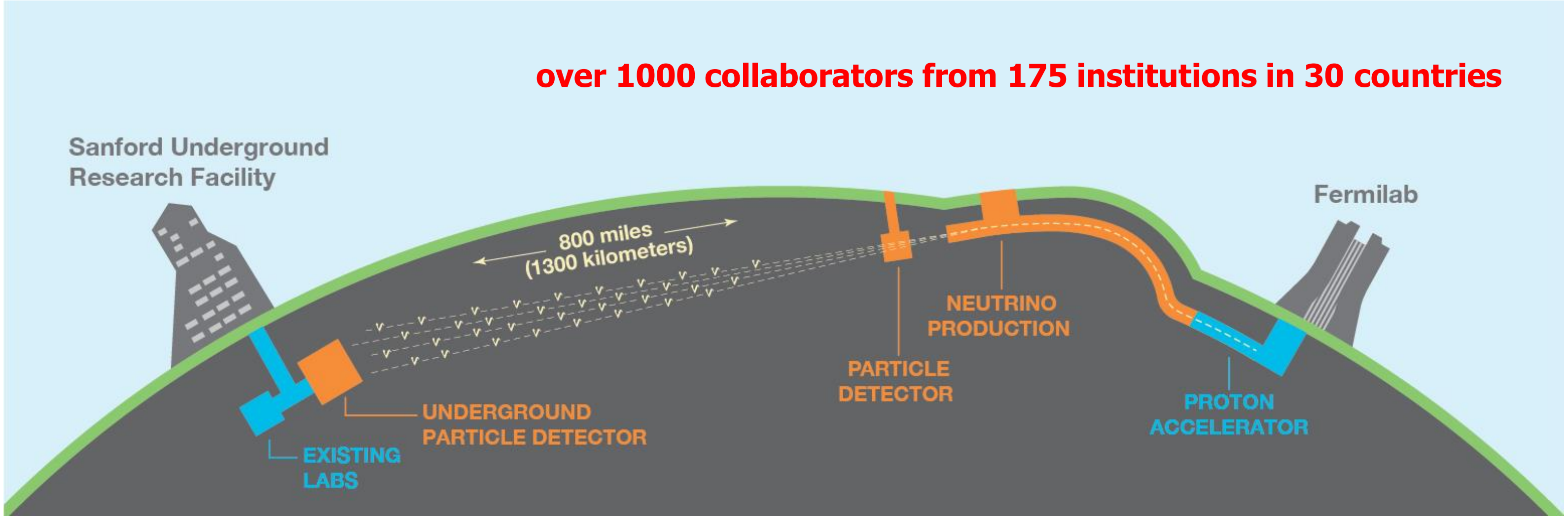
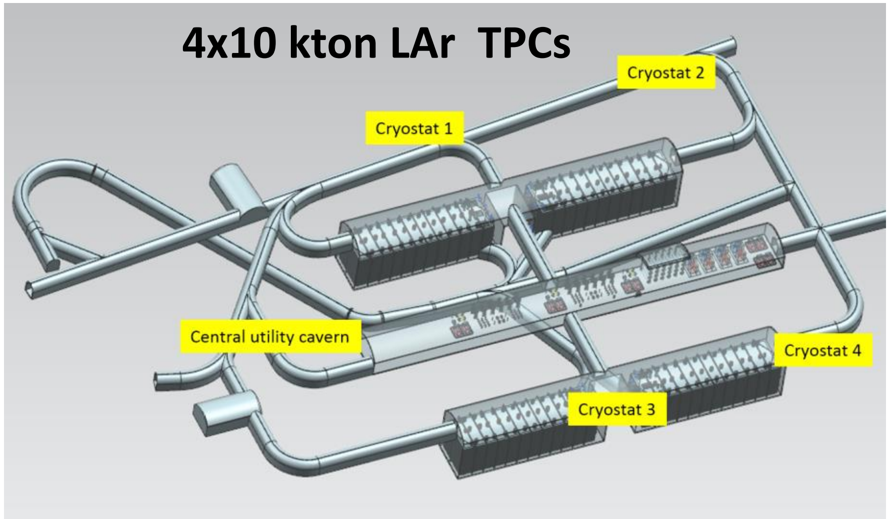
Deep Underground Neutrino Experiment (DUNE)



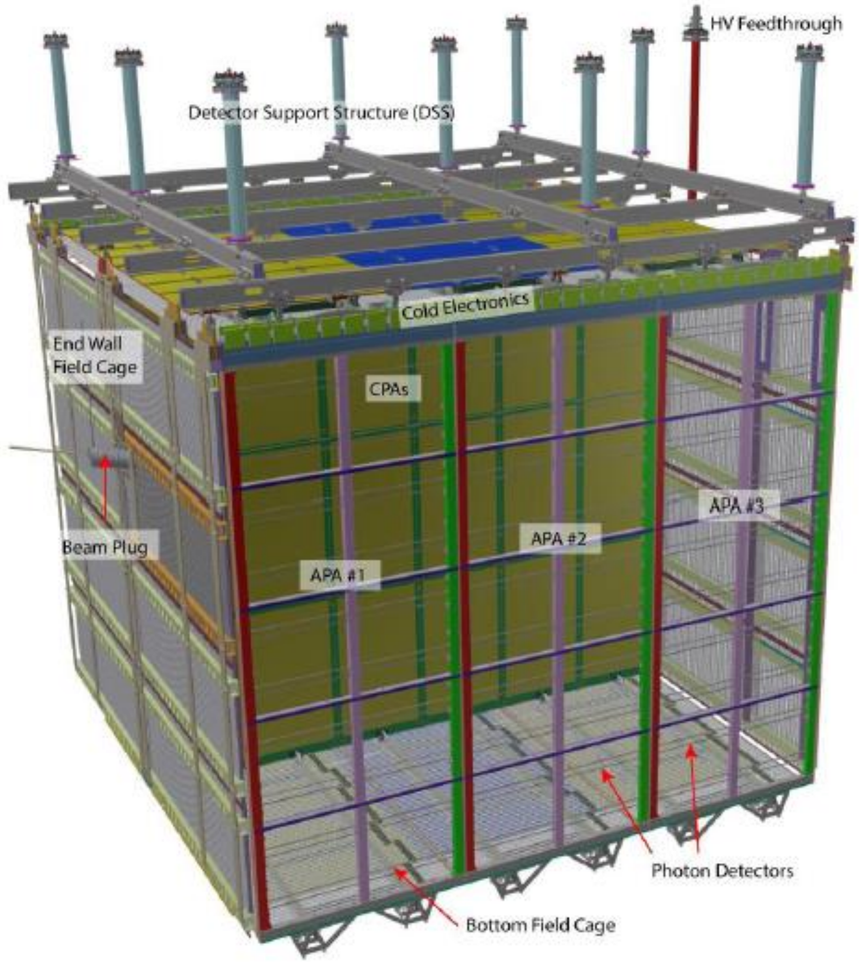
Far Detector at 1.5km underground:
4x10 kton Liquid Argon Time Projection Chambers (TPCs)



Two TPC concepts:
- **Single Phase (LAr)**
- **Dual Phase (Ar gas + LAr)**

NP04 (ProtoDUNE-SP) ~ 1% of DUNE

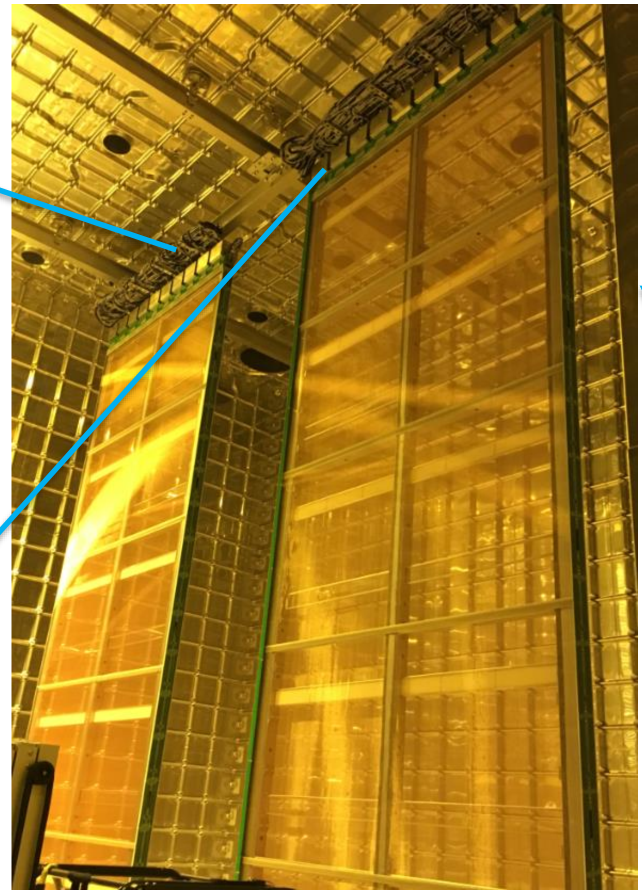
- **ProtoDUNE-SP TPC:**
  - **6 full-size (6x2.4 m^2) Anode Plane Assemblies (APAs)**
    - **A total of 15,360 TPC channels**
  - 3 **Cathode Plane Assemblies** (CPA)
    - 2 x 3.6 m^2 drift regions
- **Goals:**
  - Prototyping production and installation procedures for DUNE
  - Validate design from perspective of basic detector performance
  - Accumulate test-beam data to understand/calibrate response of the detector
  - Demonstrate long term operational stability of the detector.

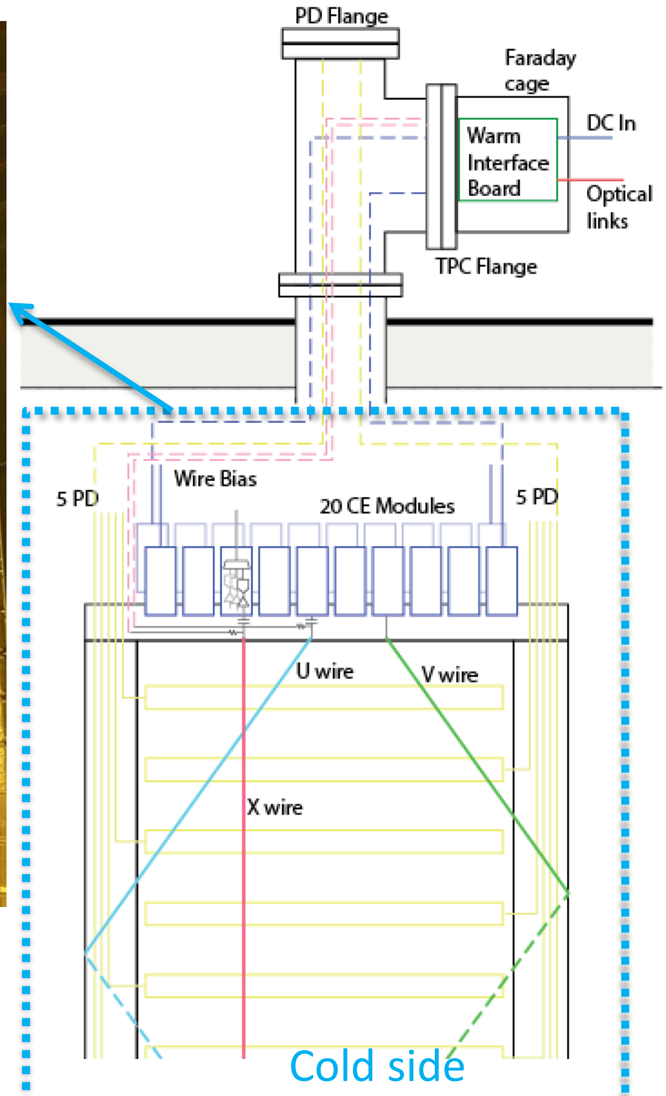


Readout electronics (cold side)

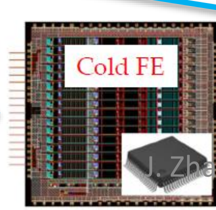
7m cold cables

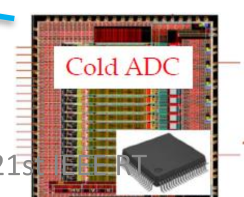
20 FEMBs / APA





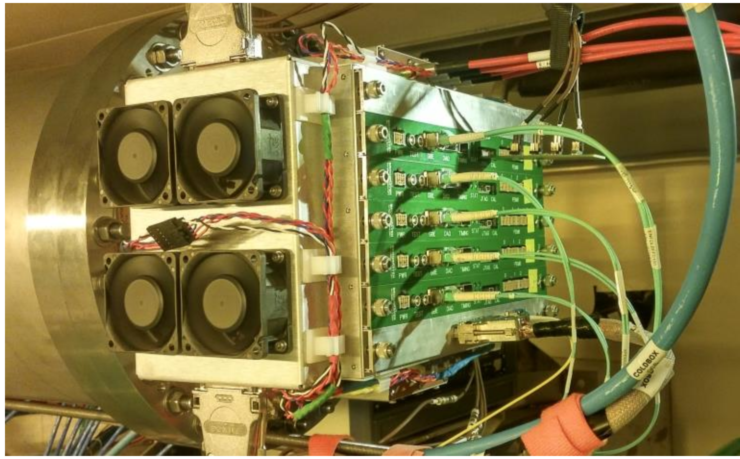
8 FE ASICs + 8ADC ASICs / FEMB

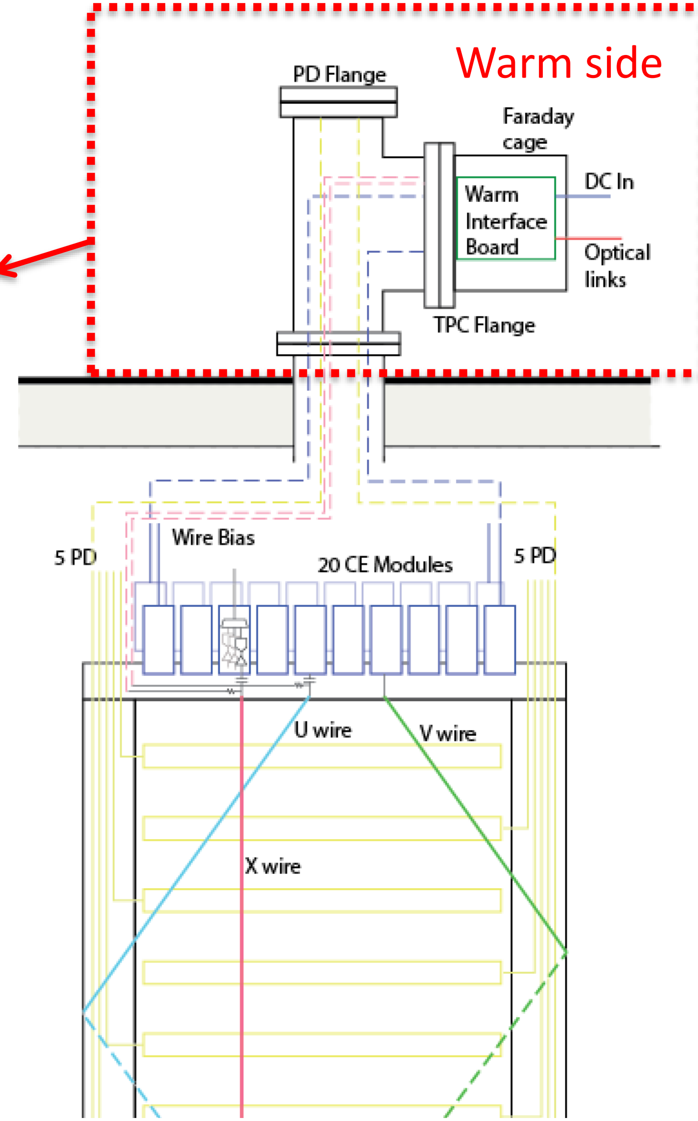


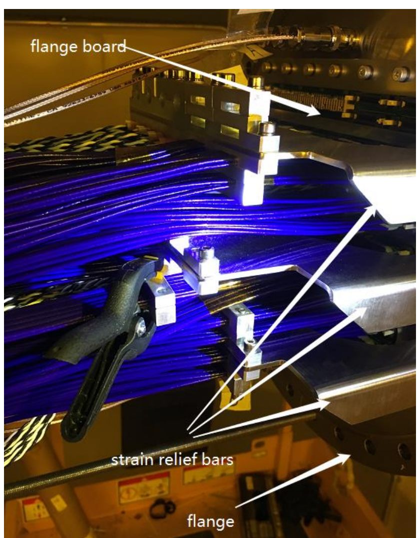


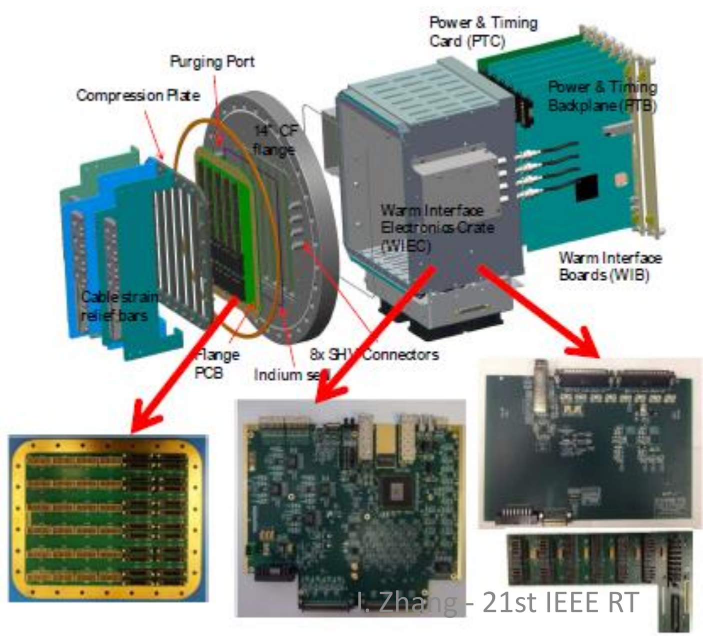
Readout electronics (warm side)

1 WIEC / APA
1 flange board / APA
1 PTC / APA
1 PTB / APA
5 WIBs / APA

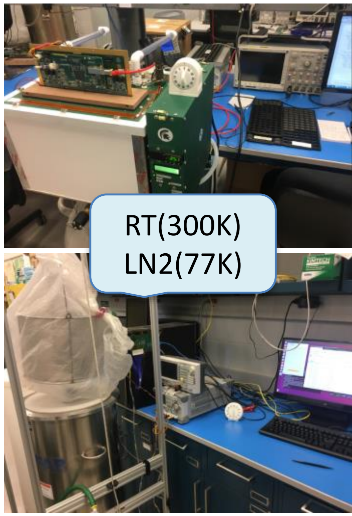




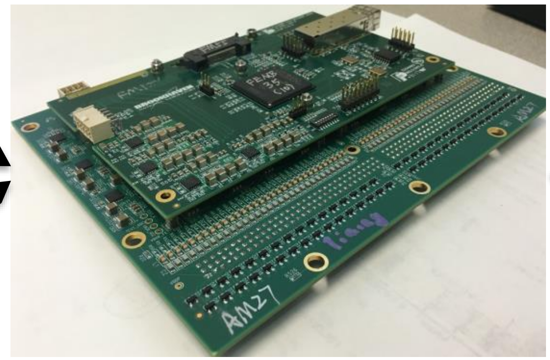




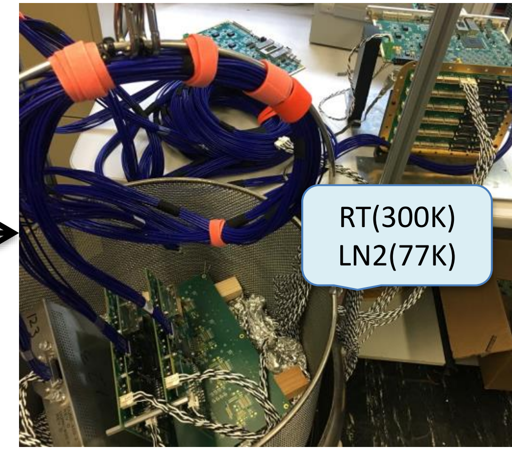
FEMB production



FE + ADC ASIC Screening



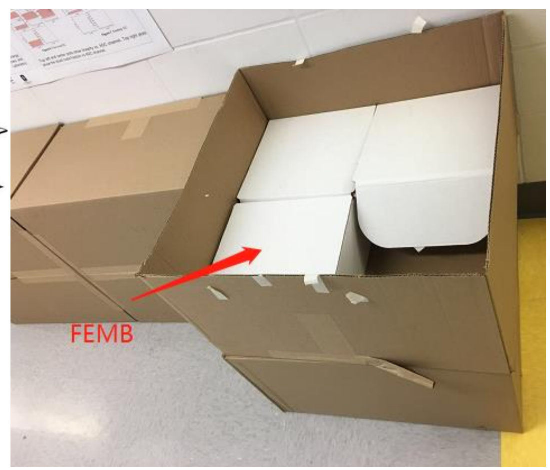
FEMB Assembly



FEMB Screening (Preliminary)

(FEMBs assembled in CE boxes)

FEMB Final Screening



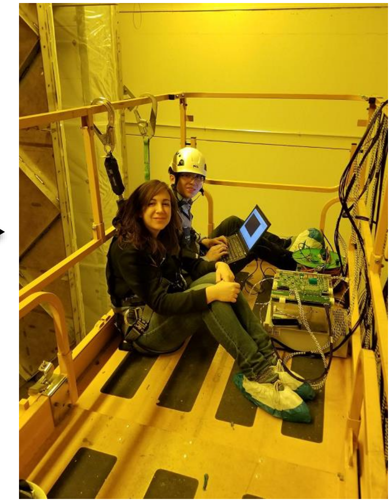
Packaging

CERN

APA Integration Test

CE box checkout (in barrack)

Install CE boxes on the top of APA



CE box checkout (on APA)

Move APA into the cold box

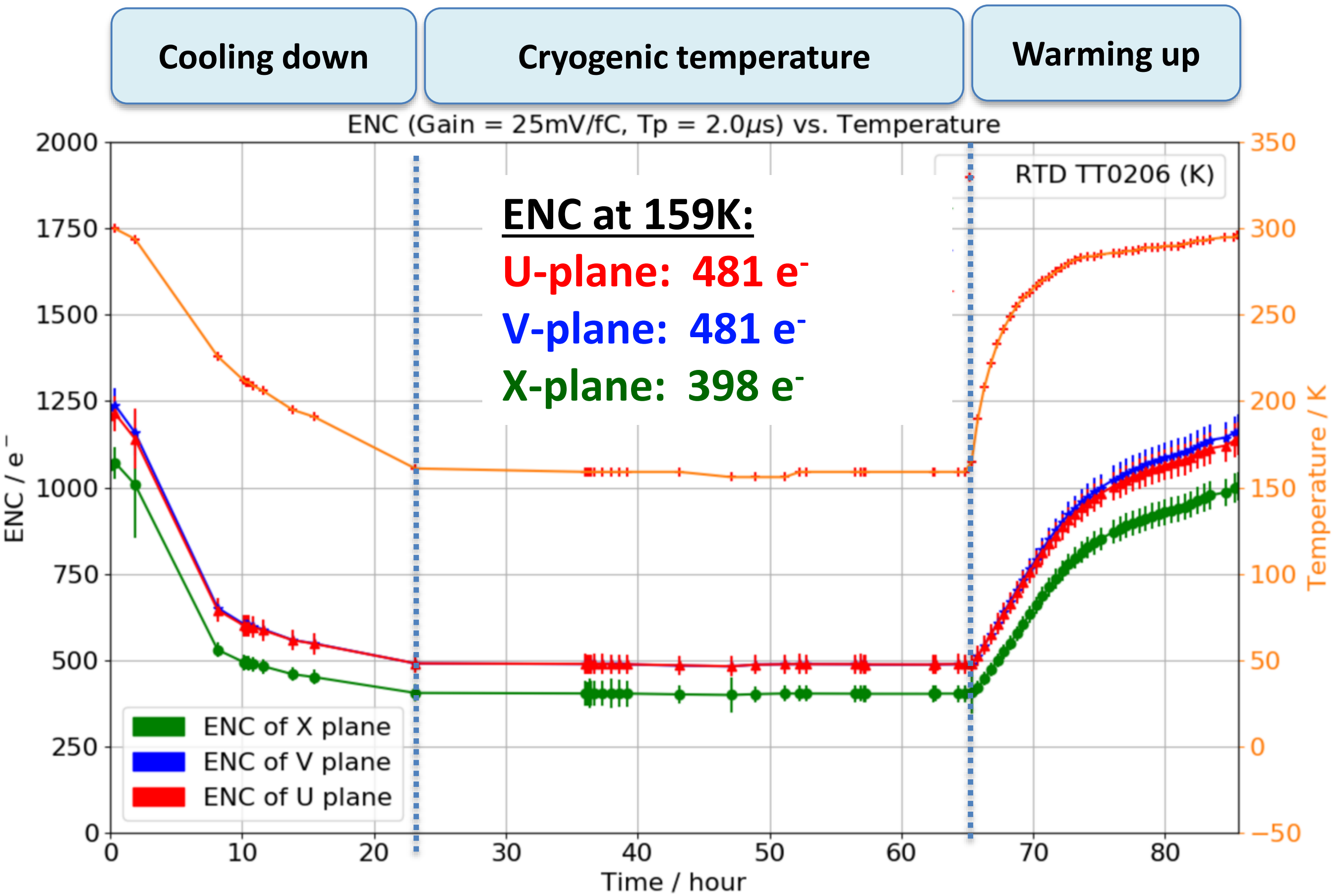
Experimental area--- extension EHN1 hall

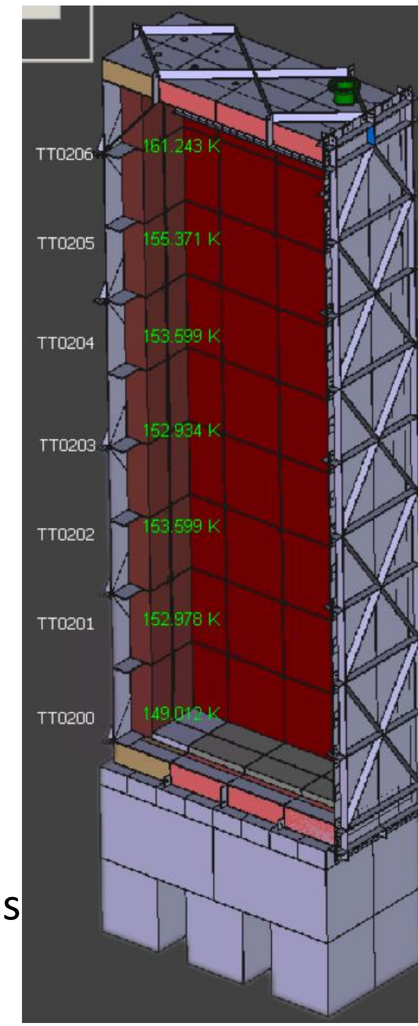
Warm test → Cooling down → Cold test (150 K) → Warming up → Warm test

Move APA into Cryostat

ENC Performance vs Temperature

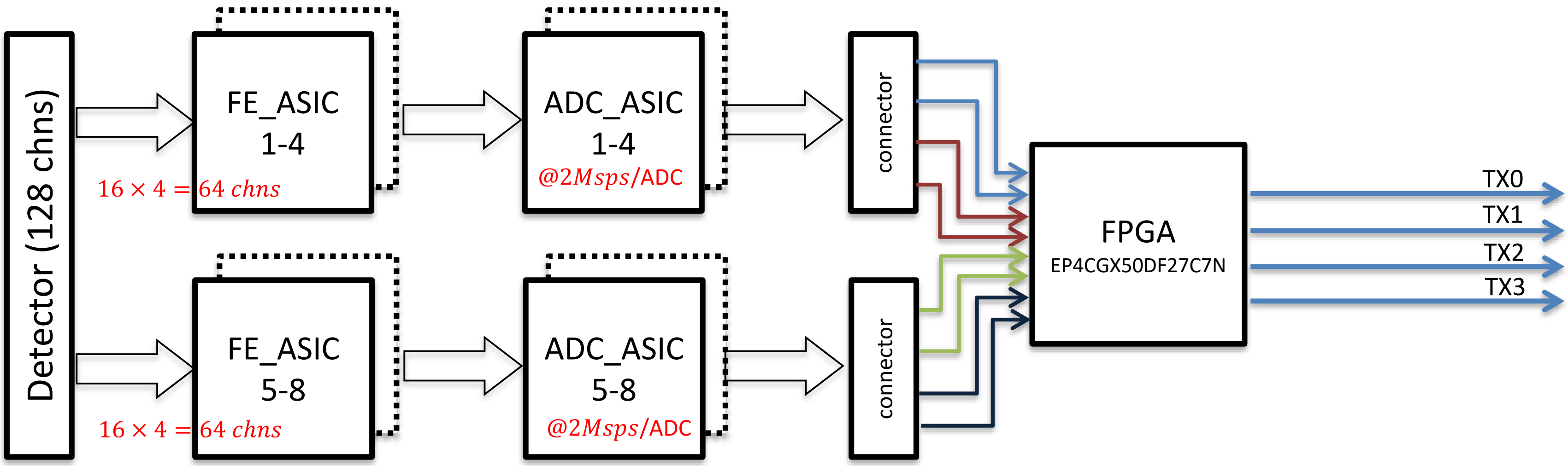
APA2 (2018-01) **Lowest temperature reached ~ 159K**

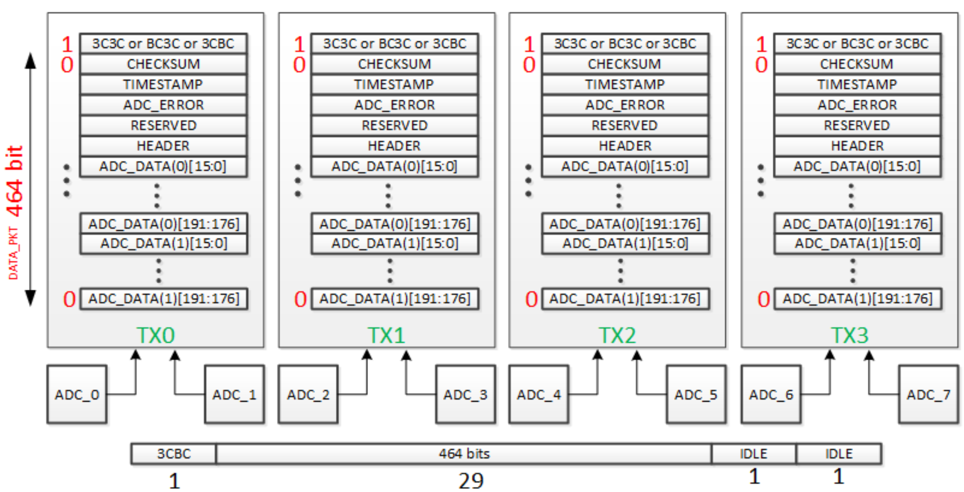




1. Uniform gain (77 e-/bin) is applied for calculating noise of all channels
2. HV Bias voltages were off
3. Data are read out chip by chip over local diagnostic GbE port.

Data flow (FEMB in cold side)





For each Tx link:

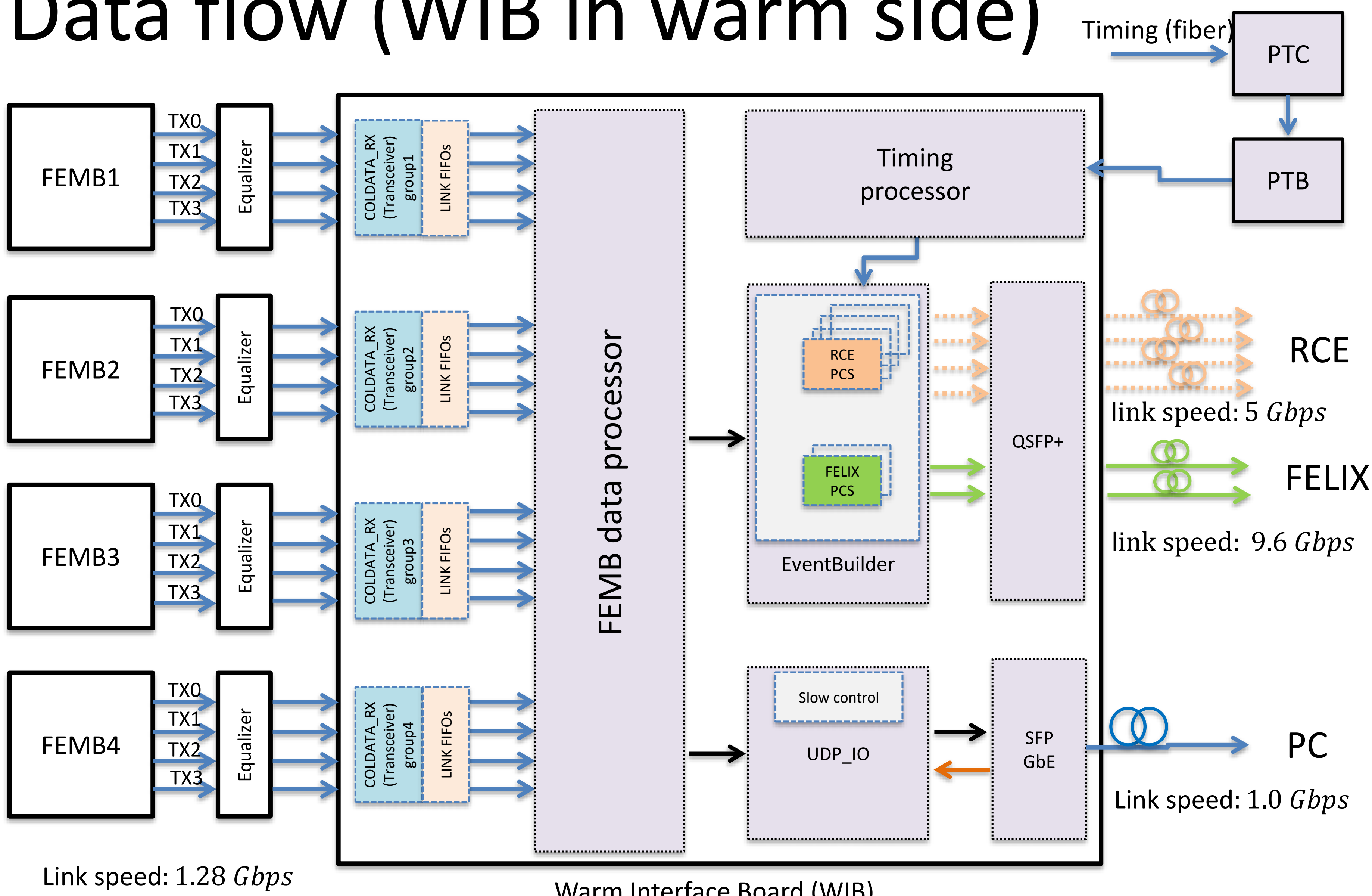
Data rate of payload

$$29 \times 16bit \times 2MHz \times 1.25(8B/10B) = 1.16Gbps$$

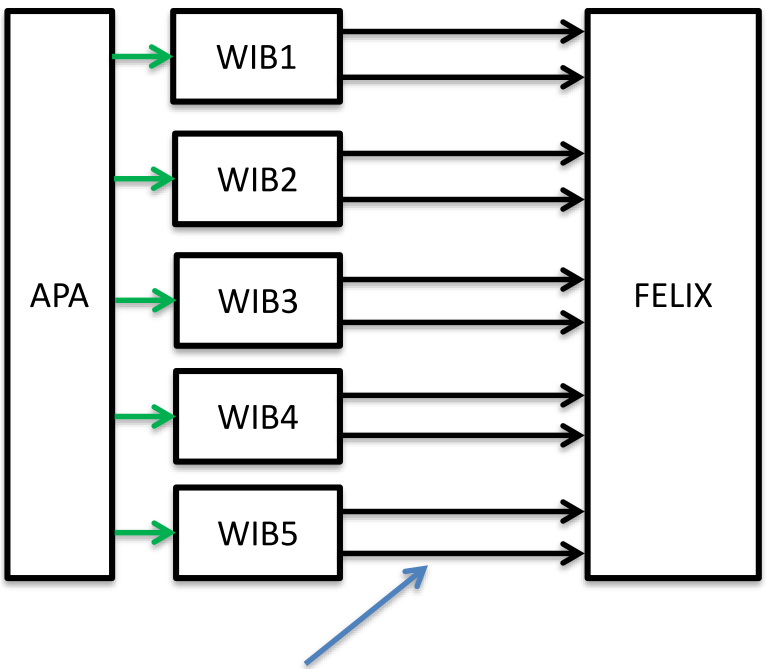
Data rate of physical link

$$32 \times 16bit \times 2MHz \times 1.25(8B/10B) = 1.28Gbps$$

Data flow (WIB in warm side)



ProtoDUNE-SP WIB-FELIX readout



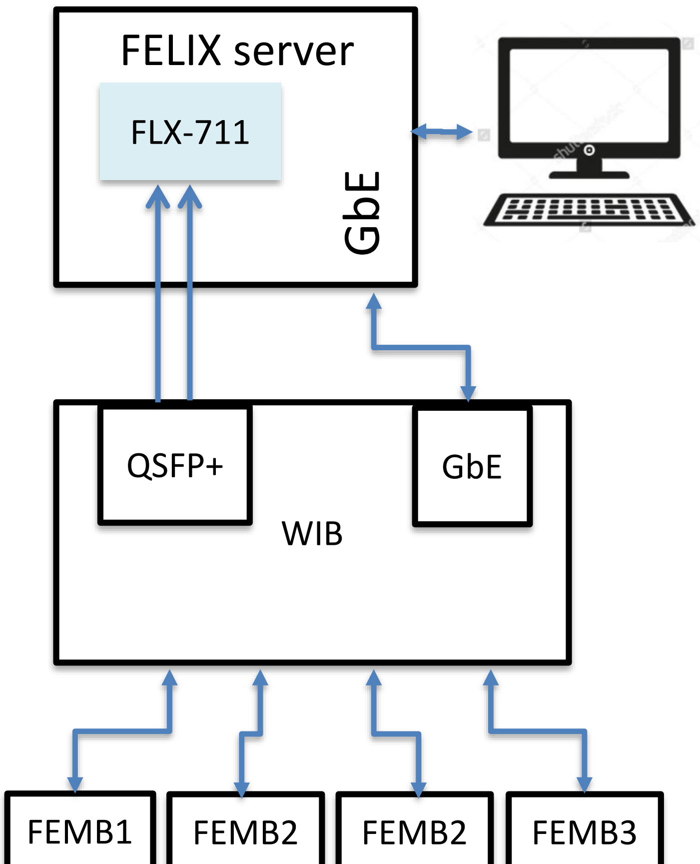
FULL mode: @9.6 Gbps per link

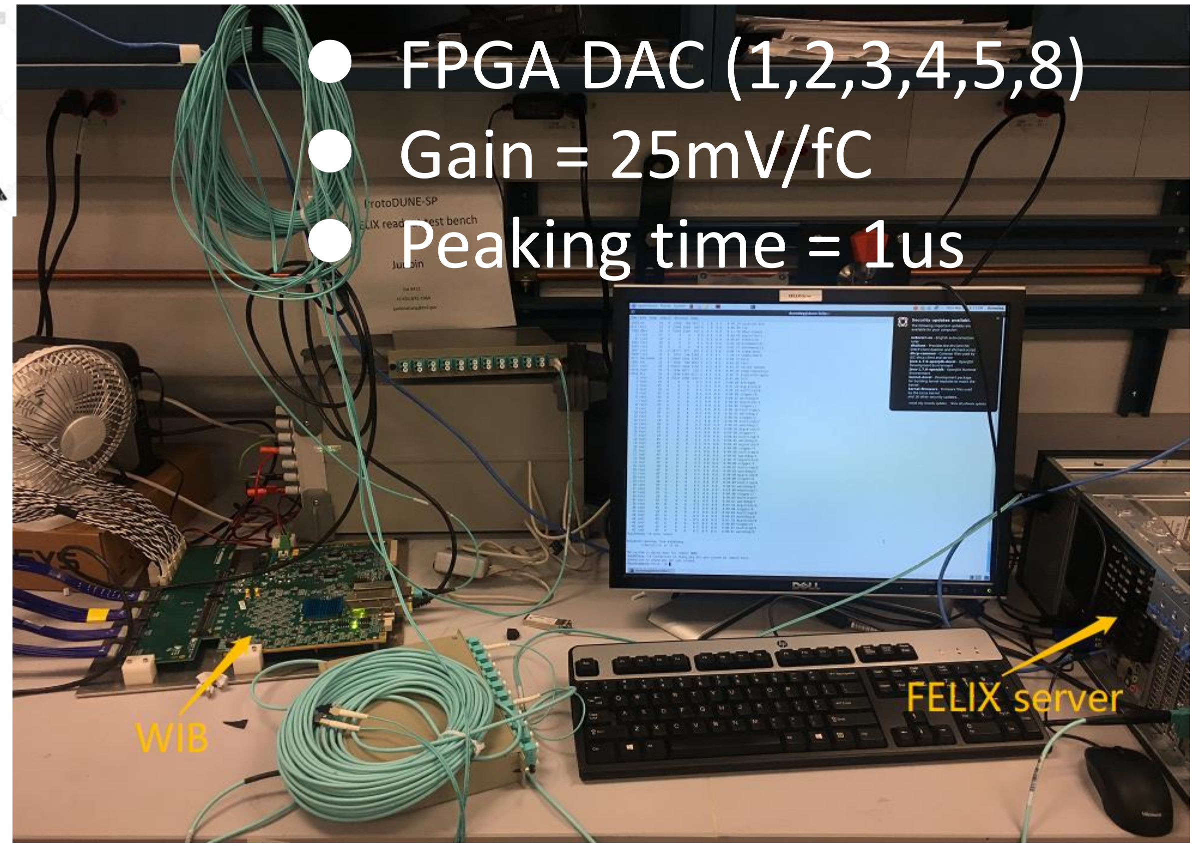
BNL-712 (FLX-712) PCIe card

One FLX-711/712 card has enough bandwidth to read out one APA with 10 FULL mode links.

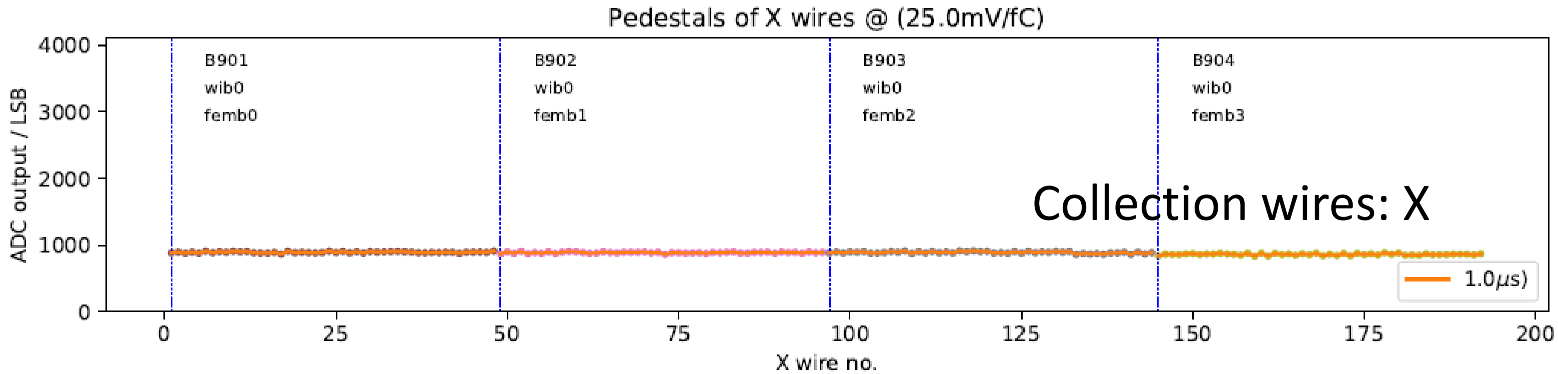
- Xilinx Kintex UltraScale
- 16-lane PCIe Gen3.0, throughput tested ~101Gb/s
- 48 optical transceivers (MiniPOD)
- On-board timing interface

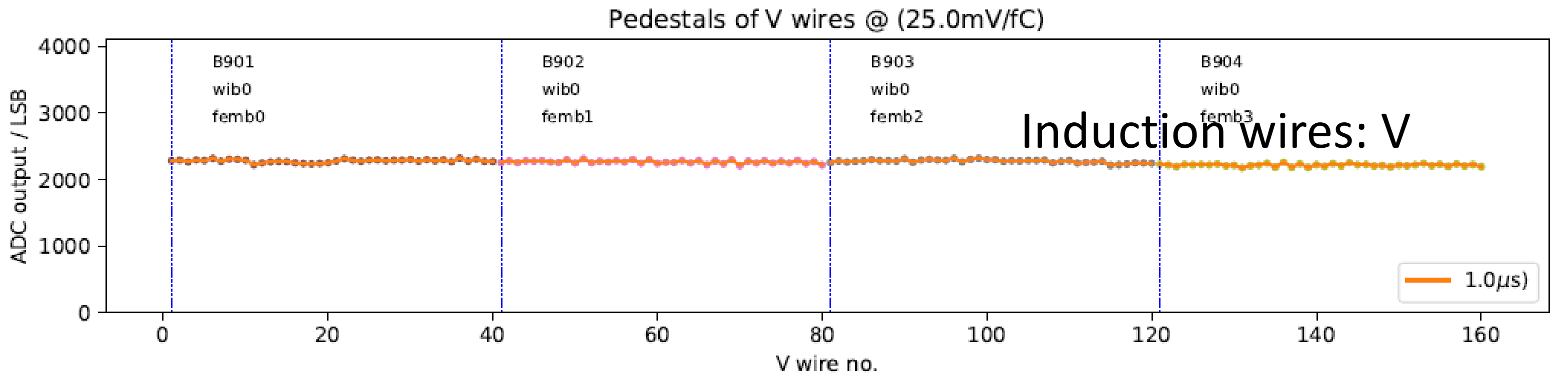
WIB-FELIX test stand @ BNL

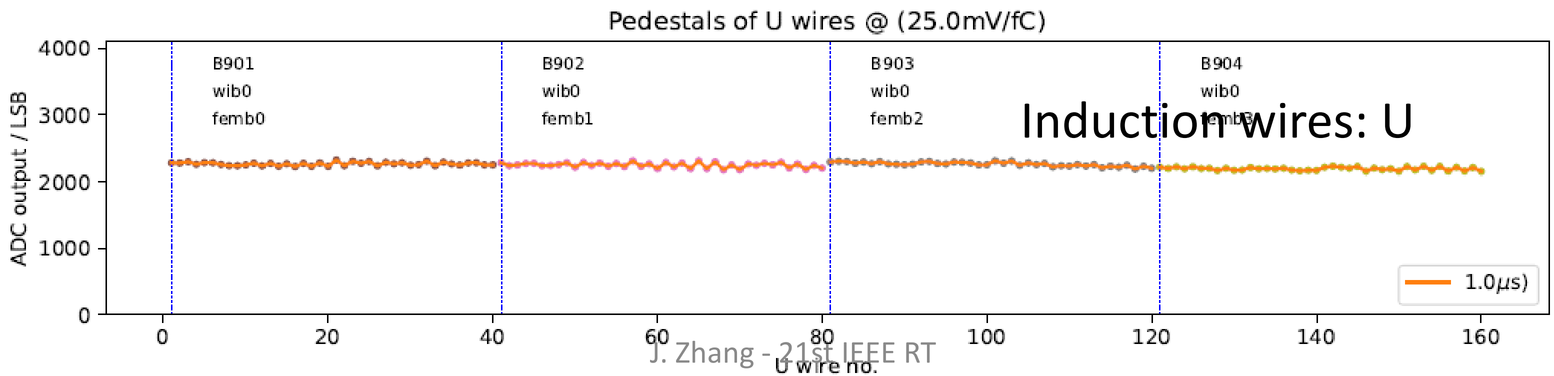




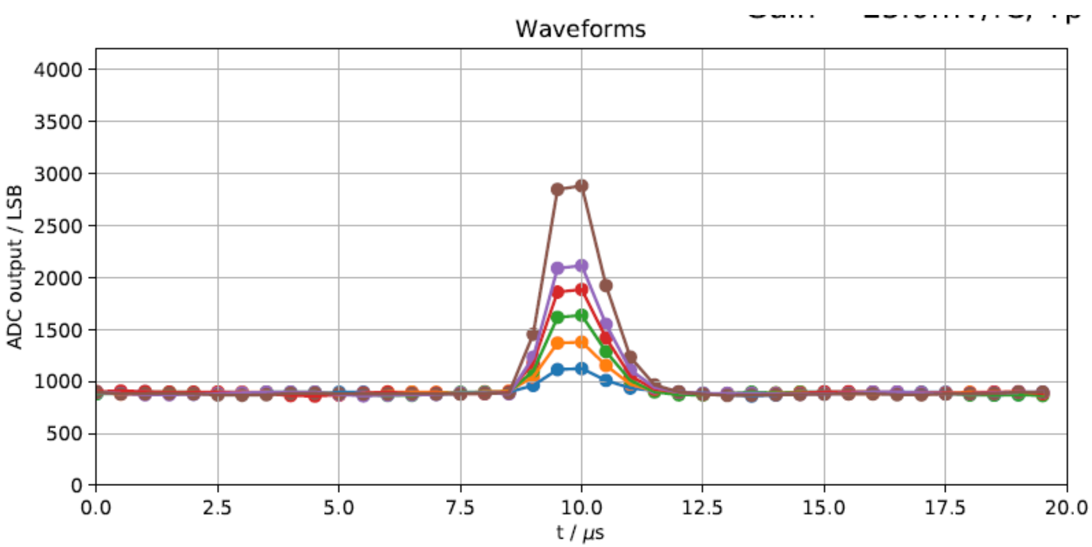
Pedestal from one WIB





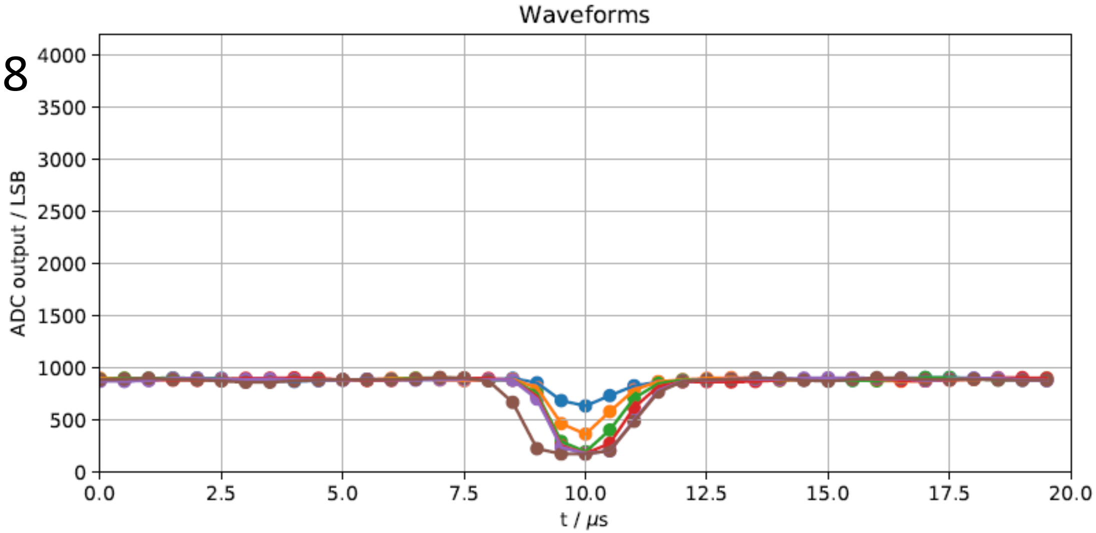


Calibration Waveform

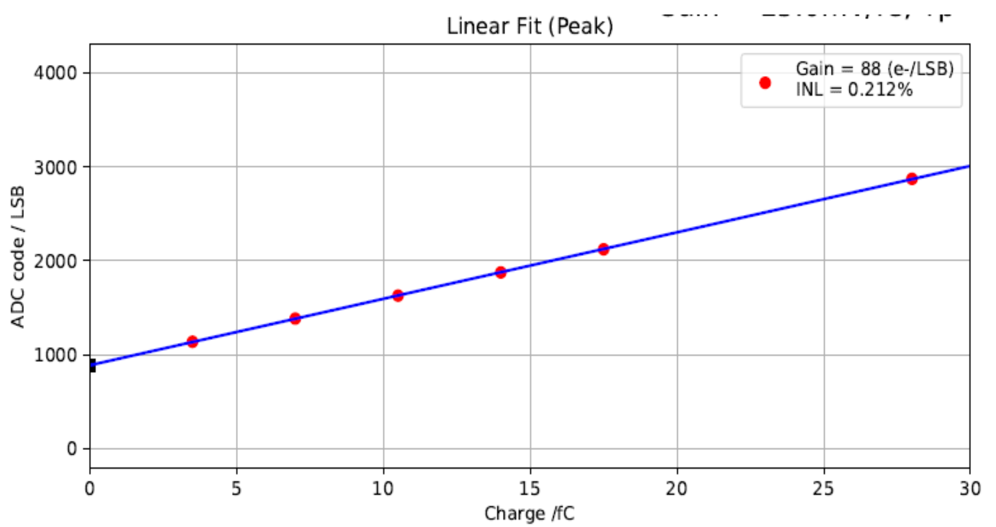


Collection wire

DAC = 1,2,3,4,5,8

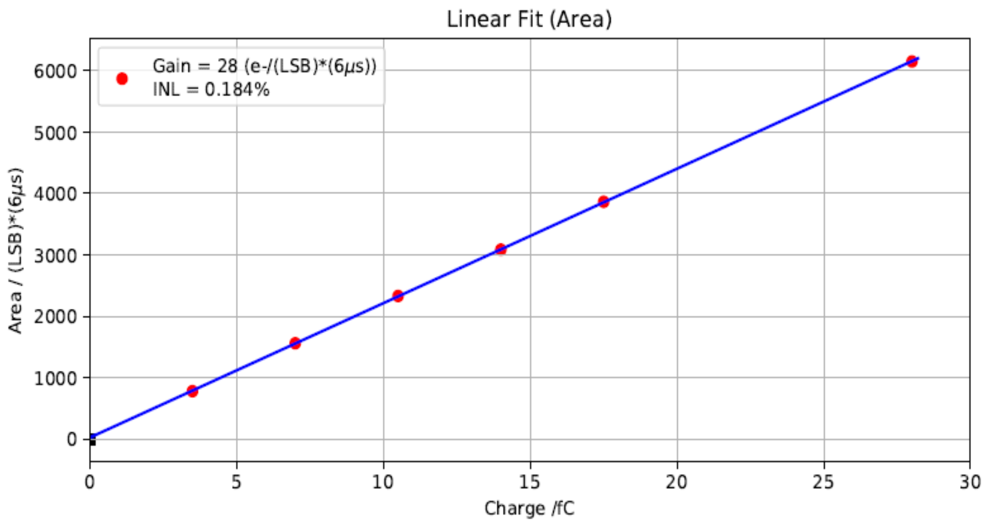


Calibration: ADC (Peak & Area) vs. Charge



Peak vs. Charge

DAC = 1,2,3,4,5,8
INL = 0.212%



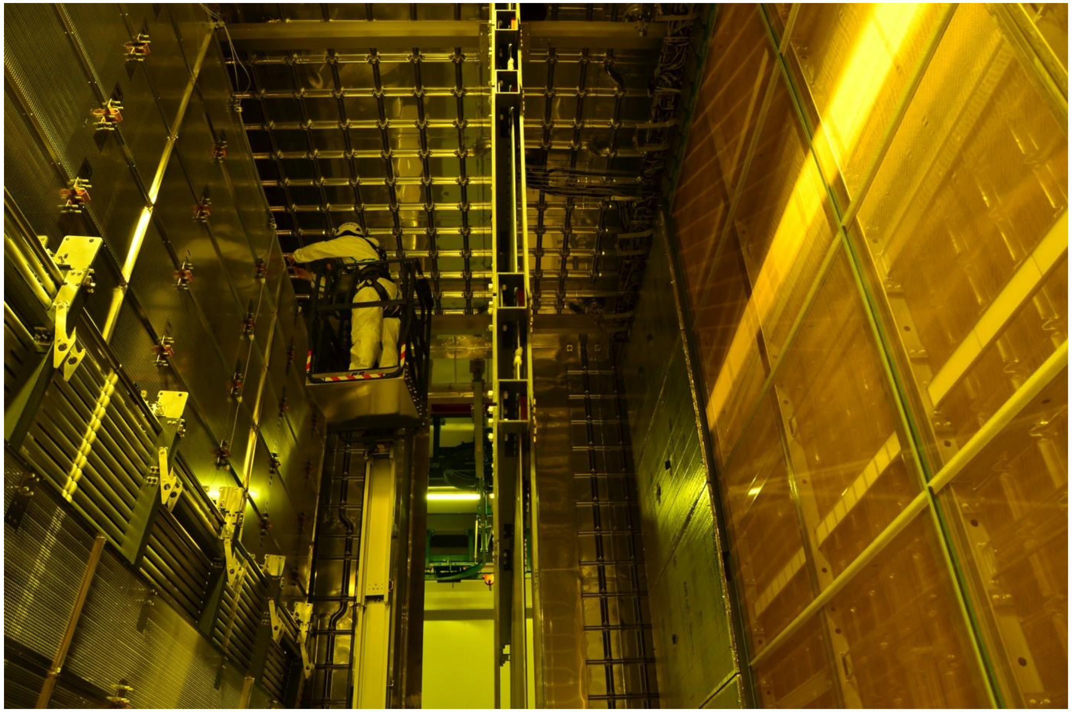
Area vs. Charge

DAC = 1,2,3,4,5,8
INL = 0.184%

ProtoDUNE-SP –Present and Future

All **6 APAs** and **3 CPAs** have been installed into the ProtoDUNE-SP cryostat

- Cold Electronics (CE) and photodetectors (PD) have been tested before and after the installation on APAs
- All CE and PD cables are routed though the chimney out of the cryostat and connected to the corresponding crate.
- Integration and readout tests are ongoing at CERN and BNL
- Beam run is scheduled from August 29th to November 11th



Summary

- BNL developed cold electronics towards low temperature (77K-89K) is an enabling technology for liquid detectors. All CE boxes were assembled at BNL and shipped to CERN after a comprehensive set of QA/QC tests.
- All APAs are fully characterized before moving into the cryostat.
- Good ENC performance reached at 159K (398 e- for X, 481e- for U,V)
- BNL will advance the design of DUNE cold electronics and continue to contribute efforts at FELIX readout for ProtoDUNE and DUNE in future.

Thank You!

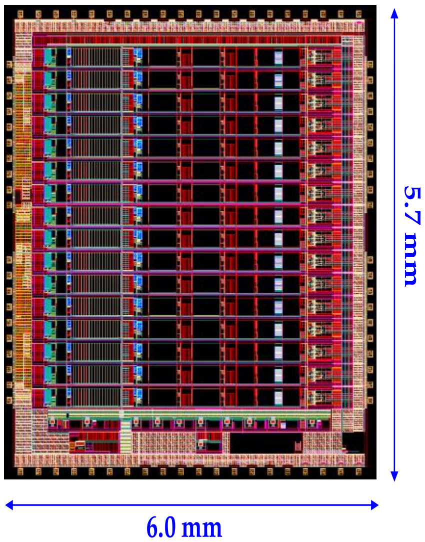
Job opening at BNL for Trigger & DAQ

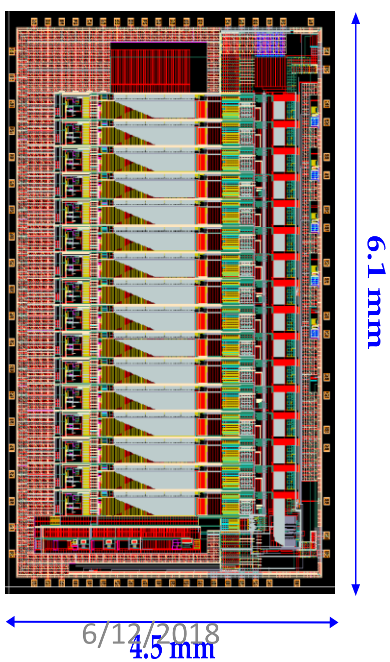
https://jobs.bnl.gov/job/upton/postdoctoral-research-associate/3437/8059129

- This job post is for multiple openings
- The successful candidate is expected to play an essential role in **FELIX** and **Global Trigger** development in the ATLAS upgrades and other *high-energy physics*, *nuclear physics* and *astronomy* experiments.
  - *Design, develop, prototype, and produce hardware and firmware for the ATLAS experiment*
  - *Evaluate hardware and firmware and characterize system performance*
  - *Participate in system integration of multiple combined systems*

Backup slides

CMOS Cold ASICs Upgrades Implemented



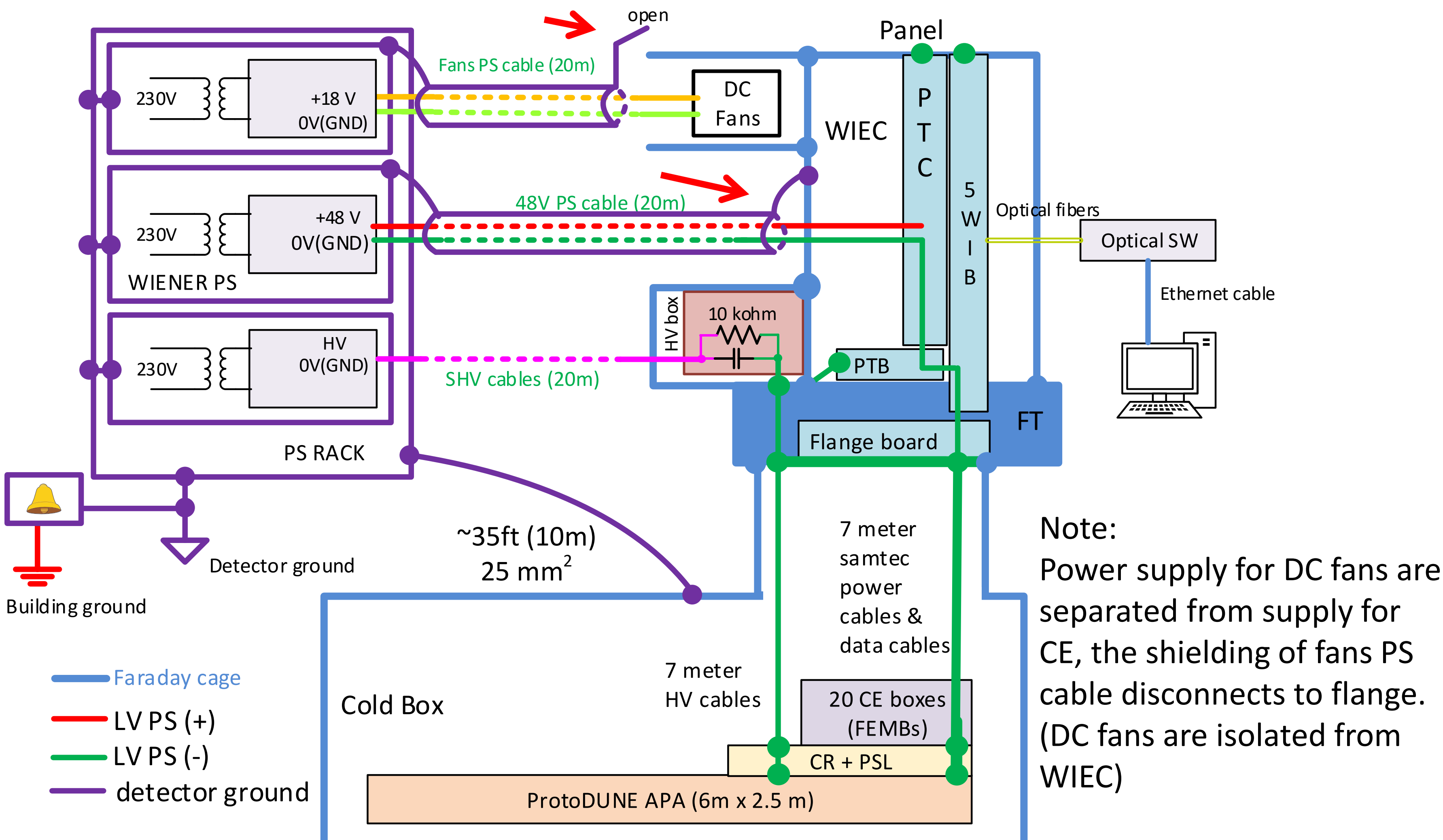


- FE ASIC
  - Built-in 6-bit DAC for calibration pulse generation
  - Built-in analog monitoring output for debug
  - Address pole-zero cancellation and drive capability in buffer-off mode
  - Add higher bias current (1nA and 5nA) options and smart reset
  - Revise BGR start-up circuit and increase ESD protection on I/O
  - ***Will be used to instrument SBND and ProtoDUNE-SP***
- ADC ASIC
  - Implement COLDATA (DUNE baseline design by FNAL, ***prototype expected in FY19***) compatible interface and FE ASIC compatible configuration
  - Address the early saturation and roll-back
  - Implement power-on default configuration and extend soft-control functions
  - Revise BGR start-up circuit and increase ESD protection on I/O
  - Improve ADC INL/DNL → not completely resolved
  - ***Will be used to instrument ProtoDUNE-SP***
  - ***SBND is exploring COTS ADC option***
  - Cold ADC ASIC development is very challenging given the ***amplified mismatch error*** and ***inaccurate simulation model*** in cryogenic temperature

Front End Electronics production at BNL

- Based on DUNE design, **20CE** boxes have been installed on each APA (**120 CE boxes, 15360** electronic channela in total).
- CE boxes were assembled at **Brookhaven National Laboratory** (BNL) and shipped to Cern after a comprehensive set of QA/QC tests.
- Integration tests in LN2 were performed at BNL by a **40%** of DUNE APA (2.8 m x 1.0 m) in a smaller cold box.

Final: CERN Grounding Scheme (with SHV cable connected)



Note:

1. Heater cable is connected but not power applied. The shielding of heater cable is connected to Heater PS but open on WIEC crate (same as Fans PS cable)
2. Two SHV cables (-650V for G plane and 800V for X plane) connect to HV power supply
3. Currently, U plane is shorted to Detector ground somewhere (investigate after cold test). The SHV cable for U plane is disconnected
4. The SHV cable for ED outer is disconnected

Equivalent Noise Charge (ENC) – Integrals
Noise Coefficients A1, A2, A3

$$ENC^2 = \frac{1}{2\pi}\int_0^{\infty} i_{neq}^2 \left|H(\omega)\right|^2 d\omega = \frac{1}{2\pi}\int_{-\infty}^{\infty} \left(\tfrac{1}{2}\right) i_{neq}^2 \left|H(\omega)\right|^2 d\omega$$

$$ENC^2 = \tfrac{1}{2} e_n^2 C_{in}^2 I_1 + \pi C_{in}^2 A_f I_2 + q I_0 I_3 = \tfrac{1}{2} e_n^2 C_{in}^2 \frac{A_1}{\tau} + \pi C_{in}^2 A_f A_2 + q I_0 A_3 \tau$$

$$I_1 = \int_{-\infty}^{\infty} \left[w'(t)\right]^2 dt = \frac{1}{2\pi}\int_{-\infty}^{\infty} \left|H(j\omega)\right|^2 \omega^2 d\omega = \frac{A_1}{\tau}$$

Series white

$$I_2 = \int_{-\infty}^{\infty} \left[w^{(1/2)}\right]^2 dt = \frac{1}{2\pi}\int_{-\infty}^{\infty} \left|H(j\omega)\right|^2 \omega\, d\omega = A_2$$

1/f

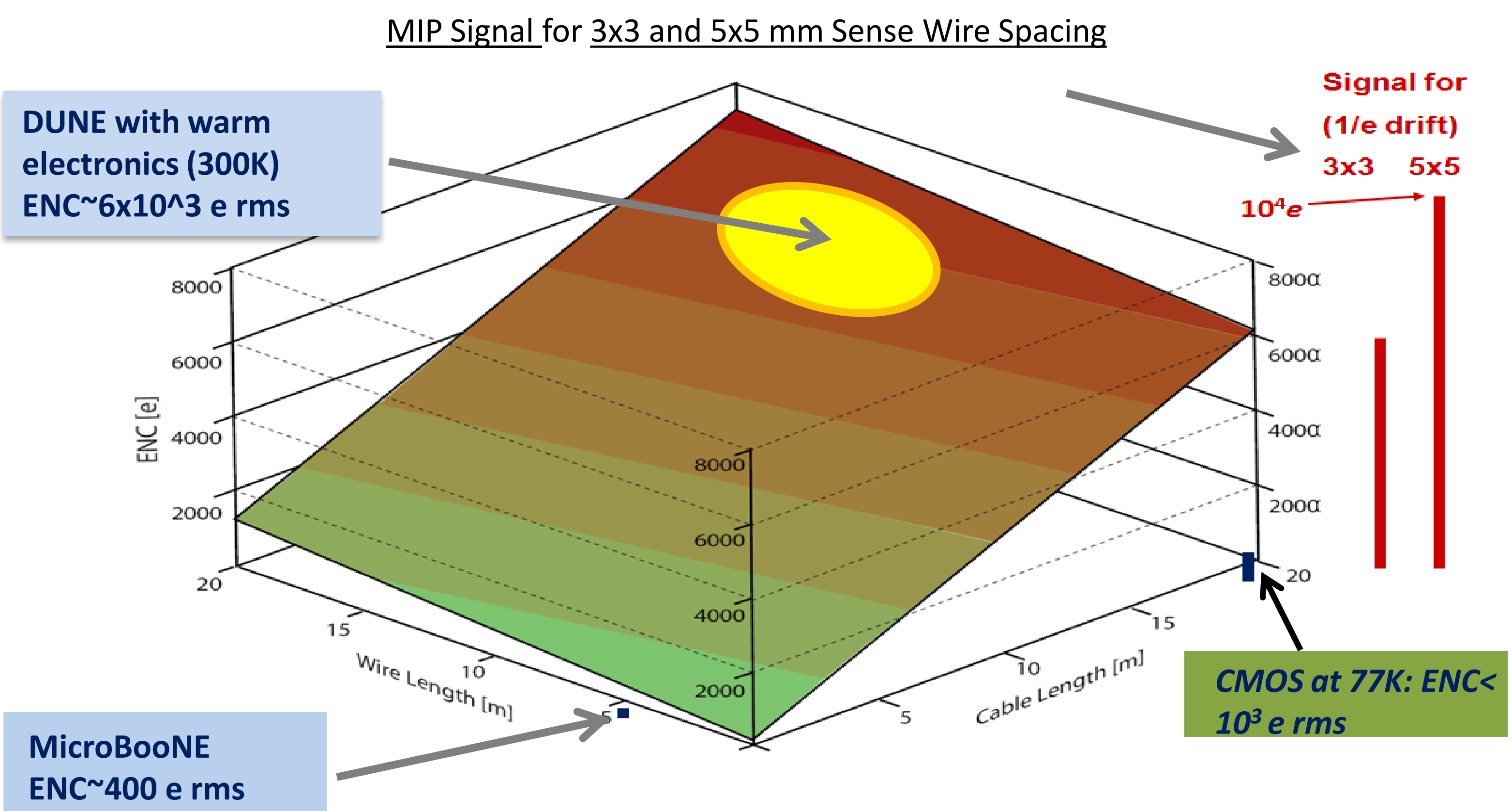
$$I_3 = \int_{-\infty}^{\infty} \left[w(t)\right]^2 dt = \frac{1}{2\pi}\int_{-\infty}^{\infty} \left|H(j\omega)\right|^2 d\omega = A_3 \tau$$

Parallel white

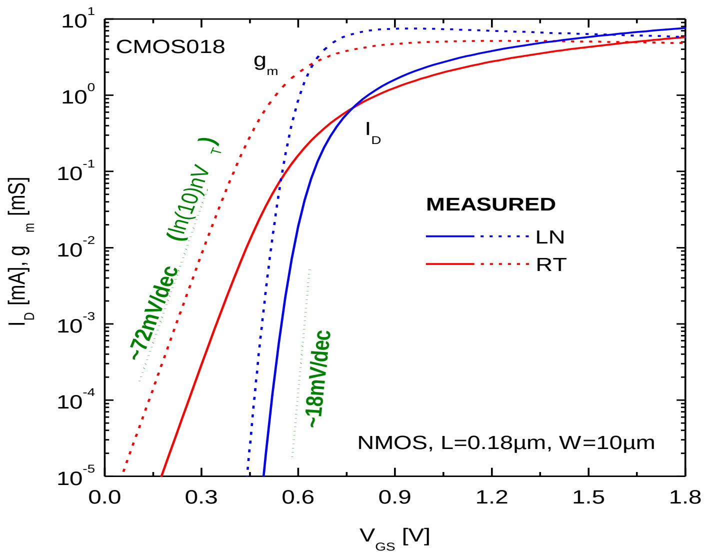
Time domain (weighting function)

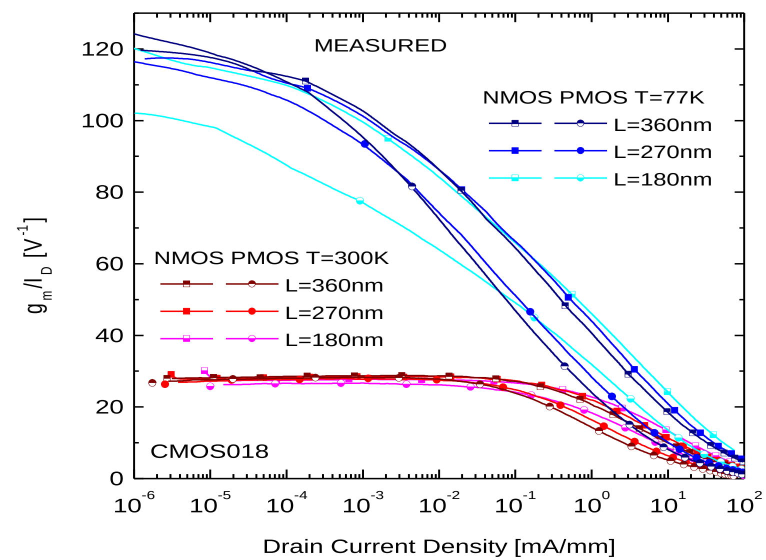
Frequency domain (transfer function)

Noise (ENC) vs TPC Sense Wire and Signal Cable Length for CMOS at 300K and 89K



Cold vs. Warm CMOS: static characteristics vs. T





Transconductance / drain current

$$\frac{g_m}{I_D} \rightarrow \frac{q}{nk_BT} = \begin{cases} \sim 30 \quad at \quad T = 300K \\ \sim 116 \quad at \quad T = 77K \end{cases}$$

At 77-89K, charge carrier ***mobility*** in silicon <u>*increases*</u>, ***thermal fluctuations*** <u>*decrease*</u> with ***kT/e***, resulting in a ***<u>higher</u> gain***, ***<u>higher</u> g_m /I***, ***<u>higher</u> speed*** and ***<u>lower</u> noise***.