

Development of FPGA-based Accelerators for Edge and Cloud using Xilinx Vivado SDx and HLS

Abstract

The Xilinx Vivado High-Level Synthesis (HLS) tool transforms a high-level specification, written in C and C++ into a register transfer level (RTL) implementation that can be synthesized targeting a Xilinx FPGA without the need to manually create RTL. Vivado HLS provides abstraction of algorithmic description, data type specification (integer, fixed-point or floating-point) and interfaces (FIFO, AXI4, AXI4-Lite, AXI4-Stream). Architects get quick verification using C/C++ test bench simulation, automatic VHDL or Verilog simulation and test bench generation. It supports several libraries to accelerate math, video, linear algebra, and DSP functions.

The Vivado SDx environments, consisting of SDAccel™ and SDSoC™, offer familiar application development and runtime experiences for C, C++ and/or OpenCL development to generate hardware accelerators using Vivado HLS. They deliver system level profiling, automated software acceleration in programmable logic, automated system connectivity generation, and libraries to speed programming. The SDSoC development environment is a comprehensive design environment for heterogeneous Zynq® All Programmable SoC and MPSoC deployment. The SDAccel environment enables the user to easily and productively develop accelerated algorithms and then efficiently implement and deploy them onto heterogeneous CPU-FPGA systems. Furthermore, Amazon Web Services (AWS) Elastic Cloud Computing (EC2) offers the SDAccel environment for cloud acceleration. The high performance and high-level of scalability offered by AWS Elastic Cloud Computing (EC2) F1 FPGA instances, paired with the power and ease of use of Xilinx SDAccel and other AWS cloud services, is very appealing for the development of high high-performance FPGA-based accelerated solutions.

This one-day workshop will explain fundamental understanding of high-level synthesis design methodology necessary to develop digital systems using Vivado HLS, followed by an introduction to the SDx environments. Attendees will be able to apply appropriate directives to optimize design performance and create custom peripheral(s) and validate in hardware. The attendees will be able to use SDSoC tool locally to create custom peripheral(s) and accelerators. They will also connect to the Amazon Elastic Compute Cloud (EC2) F1 instances to use Vivado HLS as well as SDAccel tools.

Attendees will use their laptops to connect to the EC2 F1 instances. The laptops should have two USB ports available to do Lab 3 locally.