Session Program

5–10 Jun 2016

20th Real Time Conference

DAQ 1 / Front End Electronics

Padova, Italy
Centro Congressi A. Luciani Via Forcellini, 170/A Padova ITALY

Tuesday 7 June

08:30

DAQ 1 / Front End Electronics

Session | **Location:** Padova, Centro Congressi | **Conveners:** Denis Calvet, Dr Marco Bellato

08:30–09:00

Register-Like Block RAM: Implementation, Testing in FPGA and Applications for High Energy Physics Trigger Systems

Speaker
Jinyuan Wu

09:00–09:20

A 3.9 ps RMS Resolution Time-to-Digital Convertor Using Dual-sampling Method on Kintex UltraScale FPGA

Speakers
Dr Chong Liu, Prof. Yonggang Wang

09:20–09:40

Timing distribution and Data Flow for the ATLAS Tile Calorimeter Phase II Upgrade

Speaker
Fernando Carrio Argos

09:40–10:00

The TOTEM precision clock distribution system.

Speakers
Francesco Cafagna, Michele Quinto

10:00–10:20

A Programmable Read-out chain for Multichannel Analog front-end ASICs

Speaker
Mr Francesco Caponio

10:20