

Introduction

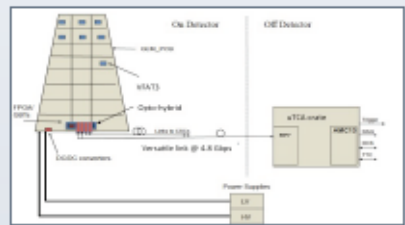
The CMS Collaboration proposes to install trapezoidal Triple-GEM detectors, with dimensions $(990 \times 440 \times 220)$ mm³ in the forward region, $|\eta| > 1.6$, of the CMS muon spectrometer. Triple-GEM detectors can provide precision tracking and fast trigger information, contributing on one hand to provide missing redundancy in the high-eta region and on the other hand to the improvement of the CMS muon trigger.



The challenges for the GEM readout system are numerous: the time resolution should be as good as 5 ns, to unambiguously identify each LHC bunch crossing, the best spatial resolution, ~100 μm, should be ensured at the first level of the CMS trigger system which has a latency of 3.2 μs and the data acquisition should sustain a very high data throughput, of the order of 100 MB/s of trigger data (zero-suppressed) per detector at high LHC luminosity (HL-LHC).

DAQ system architecture

The CMS Collaboration has launched a complete R&D program to develop a new Front-End chip, which should be flexible enough to be used with various Micro Pattern Gaseous Detectors (MPGD), as well as a trigger and data acquisition system based on the most recent developments from the telecommunication industry (μTCA), in line with the other CMS upgrade projects. In this contribution we will report on the design and the expected performance of the CMS GEM readout system, including preliminary results obtained with the first electronics prototypes.



The CMS Triple-GEM detectors are composed of 8 segments in η and 3 columns in φ. Each segment will be readout with the new Front-End electronics VFE3 under design [1]. This binary chip counts 128 channels. It can provide fast "trigger" signals at LHC clock frequency, 40 MHz, as well as "tracking data" upon the CMS Level-1 trigger signal. The "trigger" data consists of a fast "OR" of 2 strips while the "tracking data" corresponds to the full granularity of the detector.

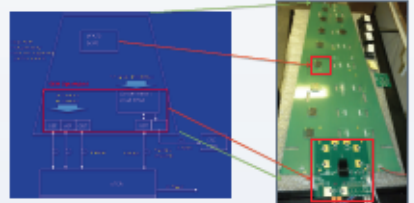
VFE3 features



Trigger and tracking data are sent to the off-detector electronics located in the CMS service cavern. The optical link will be the new Versatile Link, a new radiation hard bi-directional optical link for the LHC upgrade program, developed by CERN. The link operates at a rate of 4.8 Gbps. We propose to use the Qigabit Transceiver (GBT) radiation hard chipset on-detector to transmit the data through the Versatile Link. The VFE3 chip will embed an e-Port [2] to be connected directly to the GBT chipset. The trigger data will be sent in parallel to the Cathode Strip Chamber (CSC) Trigger Hether Board (TMB) to be combined with the CSC data and to improve the Level-1 trigger efficiency of the CSC system.

GEB & Opto-hybrid (OH)

An FPGA will be placed on the detector opto-hybrid to concentrate the trigger signals from the 24 VFE3s, to perform zero-suppression and transmit the data to the CSC as well as to the μTCA off-detector electronics. About 400 I/Os are required to connect the FPGA to the 24 VFE3 chips. To avoid cables along the detector the signals are transmitted through a large PCB, called the GEB (GEM Electronics Board) [3].

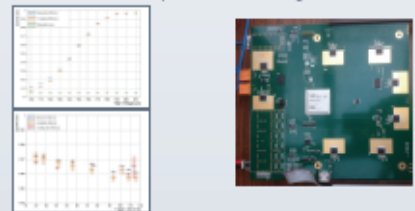


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DAQ system prototypes

Before the installation of the final system during LHC Long Shutdown 2 (2017-2018), three prototyping phases are planned. The first phase consists in setting-up the full VFE3 [6] read-out chain with the first versions of the GEB and of the OH, capable to read-out up to 6 VFE3 chips. For this first version, the OH uses a Spartan-6 FPGA and the μTCA GLIB board is used as data receiver board. The data are transmitted to the DAQ PC through the IPbus protocol. This set-up has been successfully tested in December 2014 with test beams. As an illustration the noise level (~ 30 VFE3 units) is similar to the noise measured with previous GE1/1 detector generations without GEB.



The 2nd version of the GE1/1 DAQ system has been tested with beam in October 2015. The GEB reads-out the 24 VFE3 chips and the OH is equipped with a Virtex-6 FPGA. The DAQ software is the CMS XDAQ. In addition a GEM-CSC integration facility has been set-up at CERN. Synchronization of the GEM electronics with the CSC has been achieved using the AMC13 and the CMS TTC system as source of clock and trigger. GEM trigger data are now transmitted to the CSC TMB and to the AMC13. We have demonstrated the LHC clock recovery from the optical link using a QPLL or a CDE on the OH. In the latest version of the OH, a GBTX chipset has been added on the OH to improve the clock recovery process. Developers are now focused on the use of the VFE3 chip which will become available end of 2016.

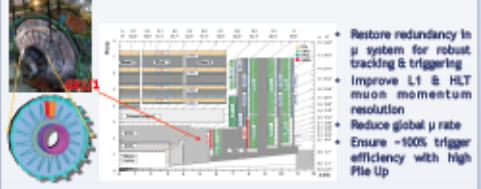
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G. De Lentdecker, on behalf of the CMS Collaboration
 Université Libre de Bruxelles (ULB)

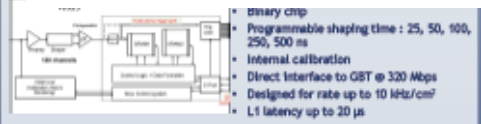
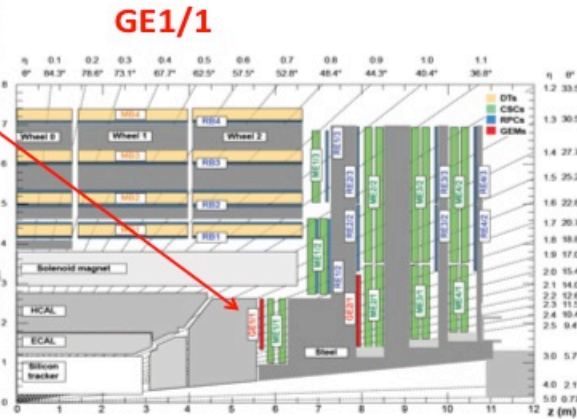
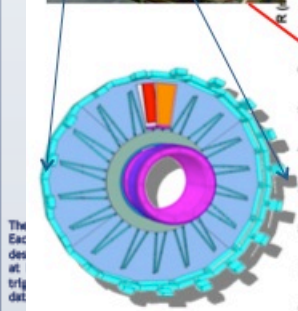
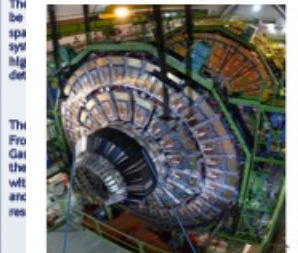
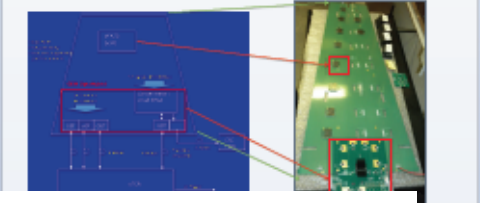
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GEB & Opto-hybrid (OH)

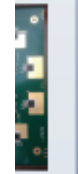
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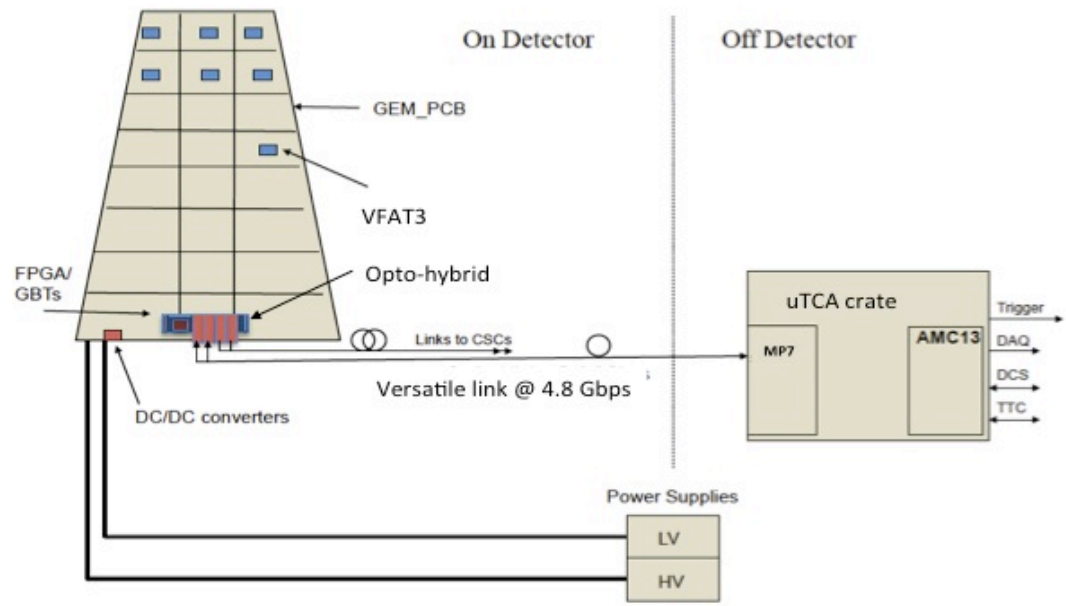
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- Restore redundancy in μ system for robust tracking & triggering
- Improve L1 & HLT

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trigger signal. The "trigger" data consists of a set "OR" of 2 strips where the "tracking data" corresponds to the full granularity of the detector.

VFAT3 features

- Binary chip
- Programmable shaping time : 25, 50, 100, 250, 500 ns
- Internal calibration
- Direct interface to GBT @ 320 Mbps
- Designed for rate up to 10 MHz/cm²
- L1 latency up to 20 μ s

Trigger and tracking data are sent to the off-detector electronics located in the CMS service cavern. The optical link will be the new Versatile Link, a new radiation hard bi-directional optical link for the LHC upgrade program, developed by CERN. The link operates at a rate of 4.8 Gbps. We propose to use the GigaBit Transceiver (GBT) radiation hard chipset on-detector to transmit the data through the Versatile Link. The VFAT3 chip will embed an e-Port [2] to be connected directly to the GBT chipset. The trigger data will be sent in parallel to the Cathode Strip Chamber (CSC) Trigger Hether Board (TMB) to be combined with the CSC data and to improve the Level-1 trigger efficiency of the CSC system.

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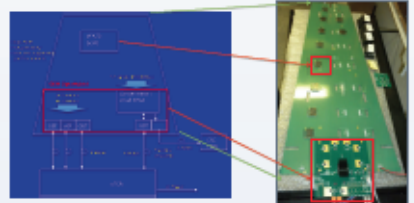
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Photograph showing the GEM readout system for the upgrade of the CMS forward muon spectrometer. The system is designed to improve the trigger efficiency of the CSC system.

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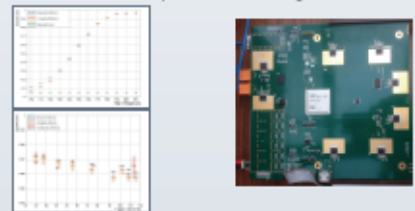


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DAQ system prototypes

Before the installation of the final system during LHC Long Shutdown 2 (2017-2018), three prototyping phases are planned. The first phase consists in setting-up the full VME64x [6] read-out chain with the first versions of the GEB and of the OH, capable to read-out up to 6 VME64x chips. For this first version, the OH uses a Spartan-6 FPGA and the μ TCA GLB board is used as data receiver board. The data are transmitted to the DAQ PC through the iBus protocol. This set-up has been successfully tested in December 2014 with test beams. As an illustration the noise level (~ 30 VME64x units) is similar to the noise measured with previous GE1/1 detector generations without GEB.



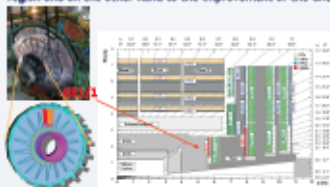
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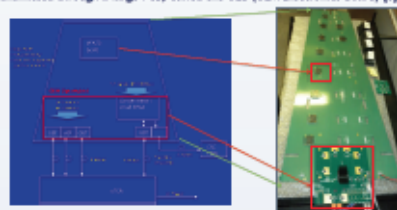
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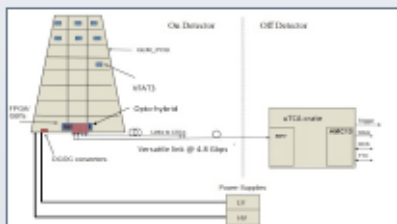


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