20th Real Time Conference

IEEE NPSS NUCLEAR & PLASMA SCIENCES SOCIETY

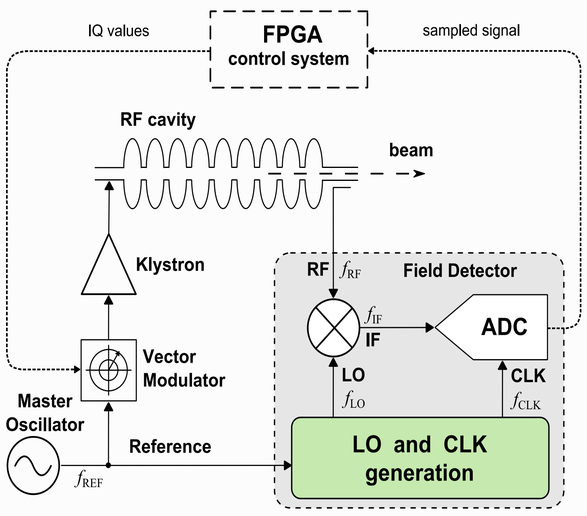
Universal High-Performance LO and CLK Generation Module for LLRF System Receivers

Mateusz Żukociński, Krzysztof Czuba, Maciej Urbański
Institute of Electronic Systems, WUT, Poland

Matthias Hoffmann, Frank Ludwig, Holger Schlarb
Deutsches Elektronen-Synchrotron, Hamburg, Germany

Abstract

A **universal high-performance Local Oscillator (LO) and Clock (CLK) generation module** for Low-Level RF (LLRF) front-end receiver is presented. The LO signal is used in superheterodyne receiver of LLRF field detector. The CLK signal is used as a low jitter sampling clock for analog-to-digital converters (ADC) of the LLRF digitizer. These high performance signals allow precise control of the electromagnetic field in accelerating RF cavities. The presented module offers flexibility and wide selection of generated **LO and CLK frequencies in range from several MHz up to 6 GHz** while maintaining **low noise performance**. This is achieved thanks to modular PCB design and already proven concept of low-noise signal generation. Module reconfiguration can be done by hardware settings and assembly options. System layout ensures signal integrity in wide bandwidth. The module is equipped with remote diagnostics that supports maintaining high LLRF system reliability. The module is packaged in a compact 1U high standard 19” crate what makes it easy to integrate with any LLRF system. The paper describes the concept of the universal LO and CLK generation module (**UniLOGM**) and its realizations in variety of configurations.



Specification

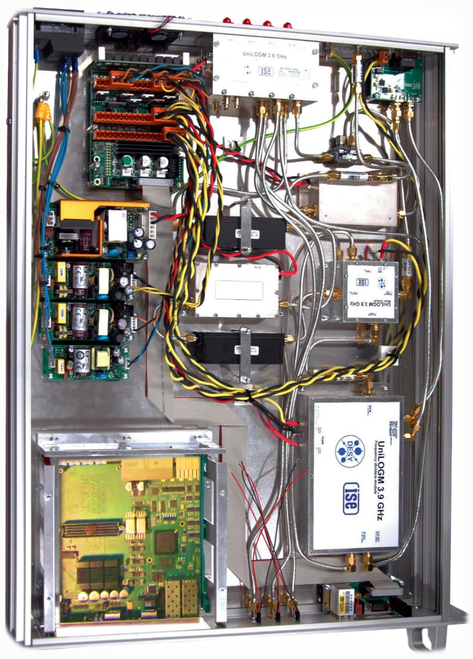
General Electrical Requirements	
Input f_{REF} range	300 ÷ 6000 MHz
Output f_{LO} range	f_{RF} ± max 200 MHz *
Output f_{CLK} range	max 300 MHz *
REF input power	+15 dBm nominal **
REF output power	4 x +13 dBm **
LO output power	4 x +13 dBm **
CLK output power	4 x +13 dBm **
monitor outputs	+ 5 dBm nominal **
LO additive phase jitter	< 3 mdeg RMS ***
CLK additive phase jitter	< 6 mdeg RMS ***
spurious-free range	> 80 dBc
Mains or DC power supply	
supply voltage and current monitoring	
signal power monitoring	

Packaging and functionality
standard 19” crate, 1U height
Rack and benchtop use
SMA connectors for RF
Reset trigger signal (RJ-45)
remote diagnostics
Ethernet communications
power supply protection

* depends on the filters selection
** power levels can be adjusted for individual case
*** integrated over the band 10 Hz ÷ 1 MHz

Rear panel

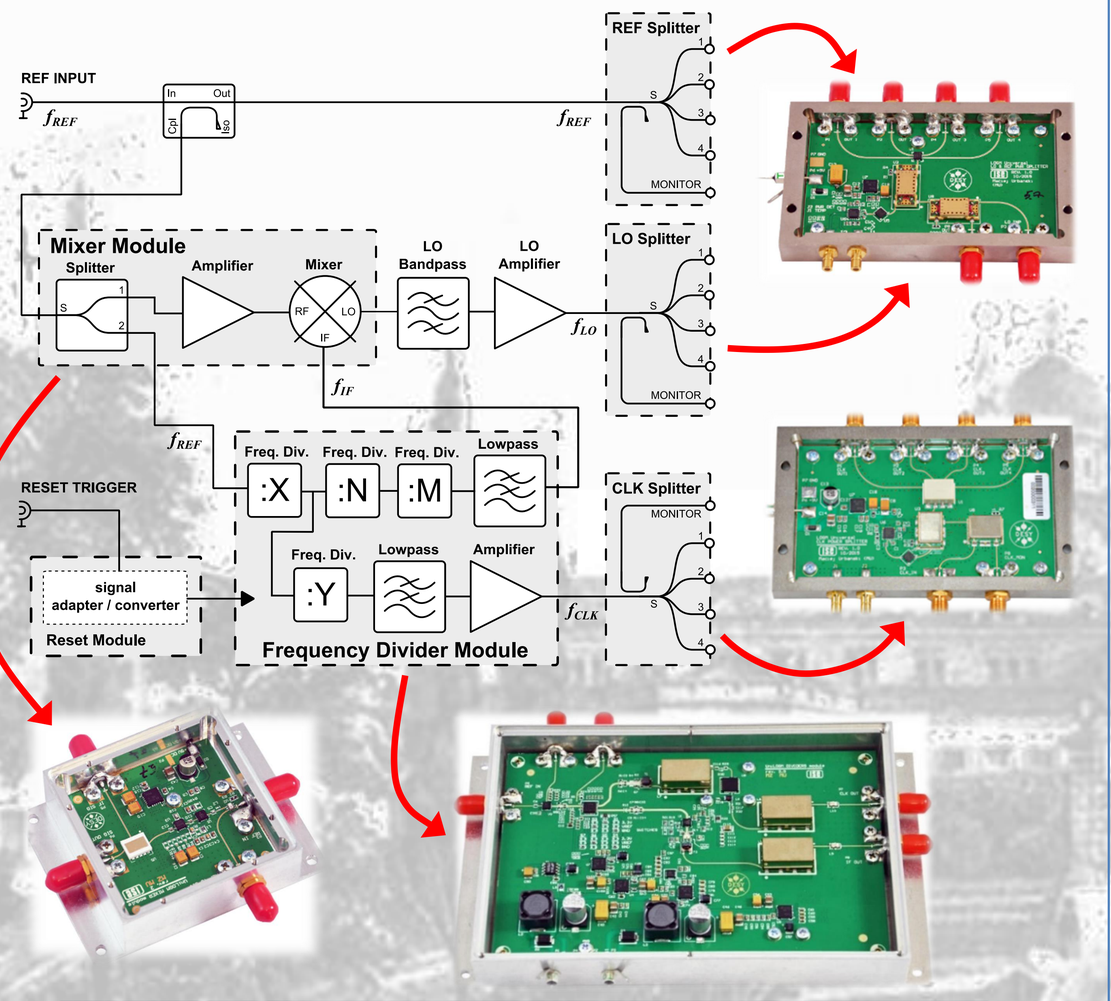
Front panel



UniLOGM crate interior top view

Concept

- Signal synthesis based on frequency dividing and mixing technique
- Single double-balanced mixer used as a frequency converter
- Multistage frequency divider with Reset
- PCB integration and modular design
- Configuration with hardware settings and assembly options

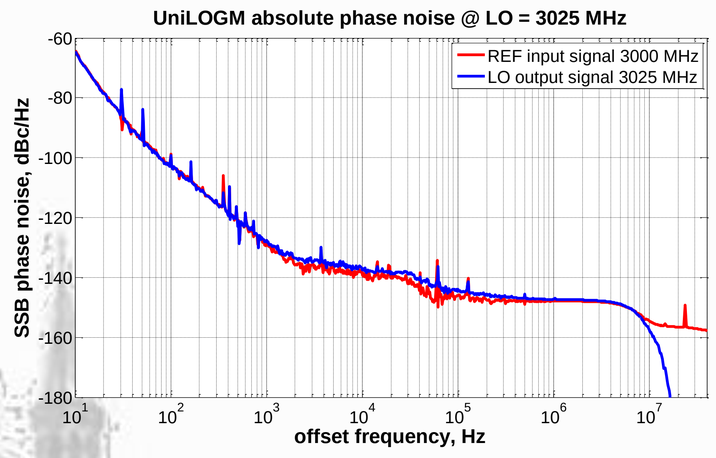


Examples of frequency variants							
f_{REF} [MHz]	X	M	N	Y	f_{LO} [MHz]	f_{CLK} [MHz]	f_{IF} [MHz]
704	2	3	5	3	727.47	117.33	23.47
1300	2	8	3	4	1354.17	81.25	54.17
2856	2	12	10	3	2903.60	119.00	47.60
3000	4	6	10	3	3025.00	125.00	25.00
3900	4	12	6	3	3954.16	81.25	54.16
5712	4	12	10	3	5759.60	119.00	47.60

Performance

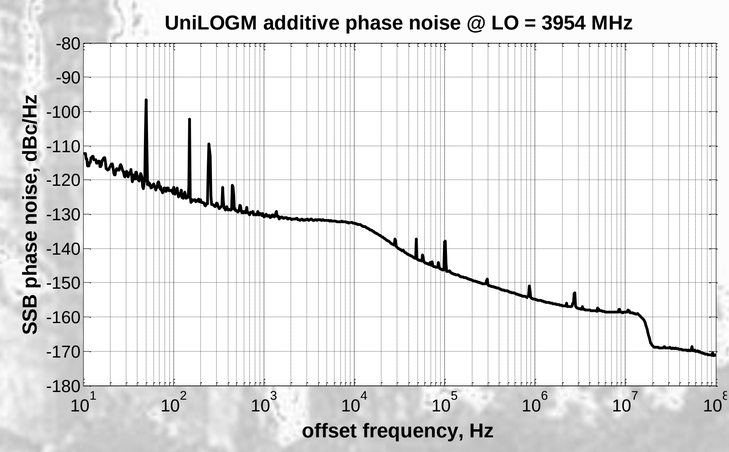
REF 3000 MHz, LO 3025 MHz

LO and REF absolute SSB phase noise characteristics



REF 3900 MHz, LO 3954 MHz

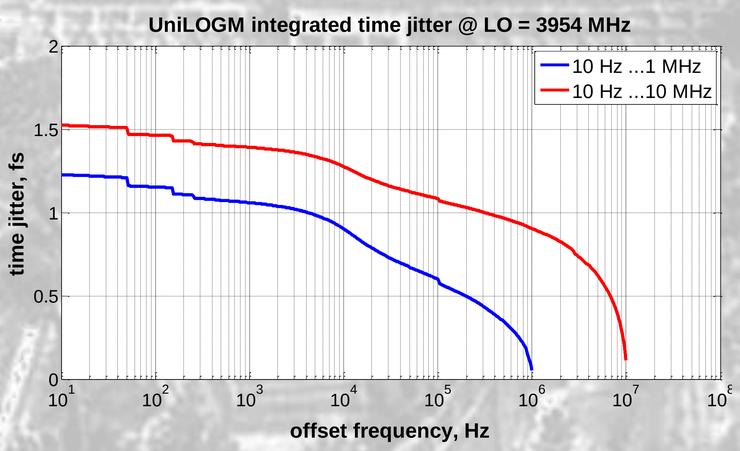
LO residual SSB phase noise characteristic



REF 3900 MHz, LO 3954 MHz

LO residual RMS time jitter = 1.2 fs (1.7 mdeg phase jitter) integrated over [10 Hz ÷ 1 MHz]

LO residual RMS time jitter = 1.5 fs (2.1 mdeg phase jitter) integrated over [10 Hz ÷ 10 MHz]



Contact

M.Zukocinski@elka.pw.edu.pl

CONSORZIO RFX Ricerca Formazione Innovazione

with the sponsorship of the University of Padova — Università degli Studi di Padova

5-10 June 2016 Padova, Italy

INFN