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Optimization of the FPGA Trigger Based on the Artificial Neural Networks for the Detection of Neutrino-Induced Air Showers

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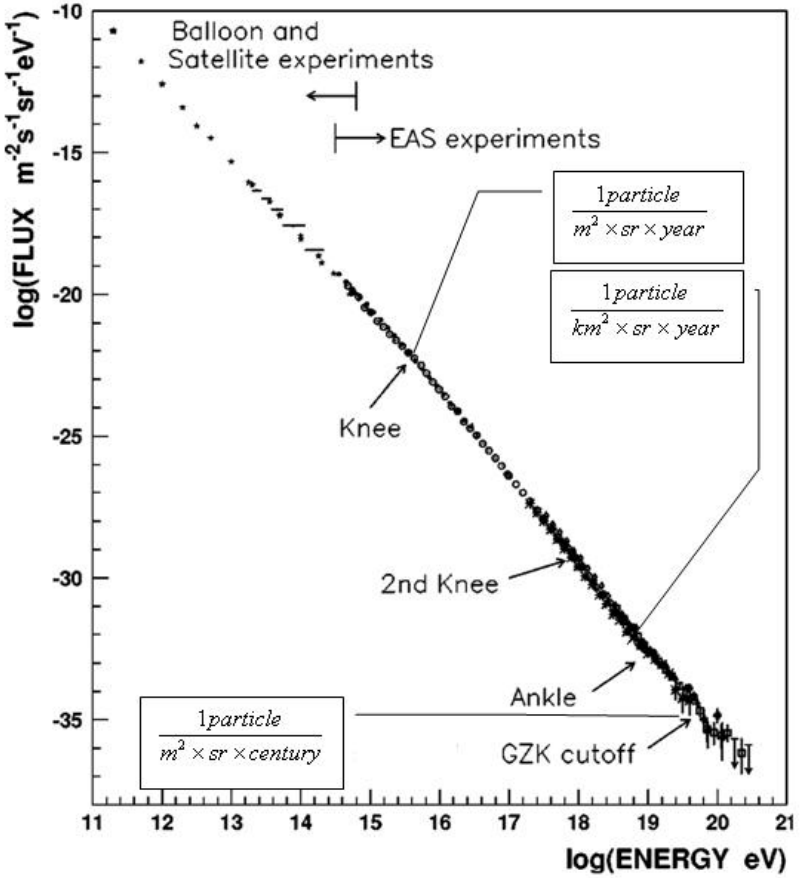
GZK and neutrinos in Pierre Auger



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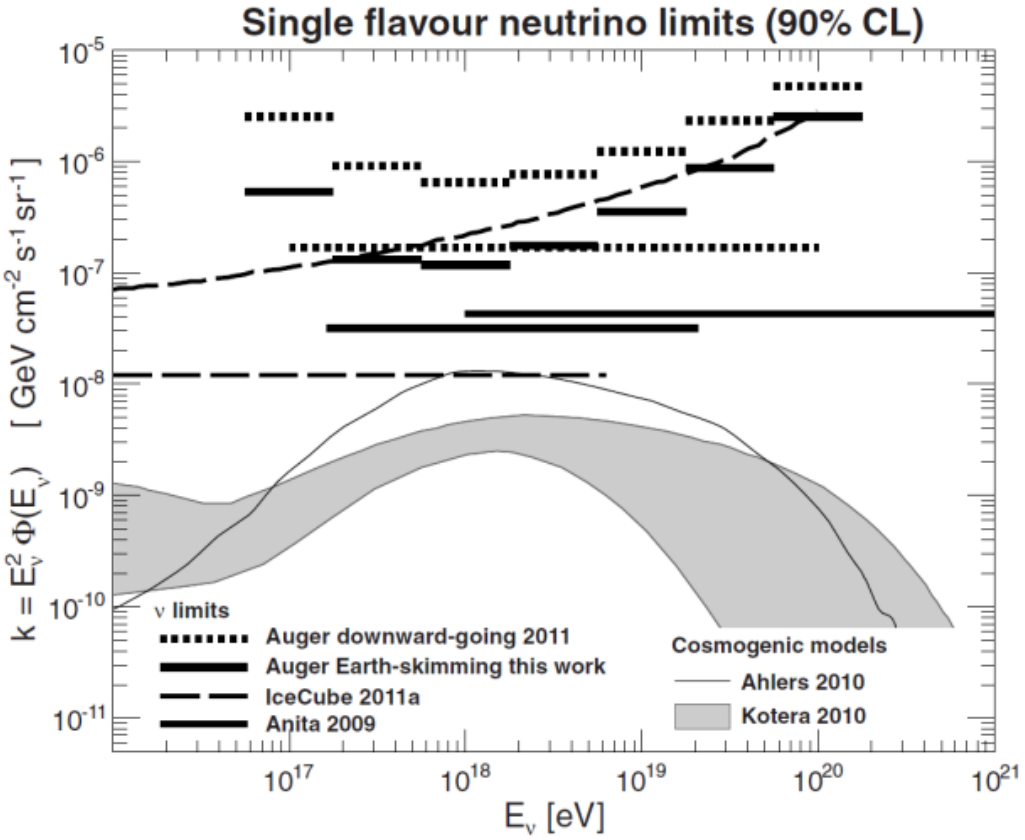
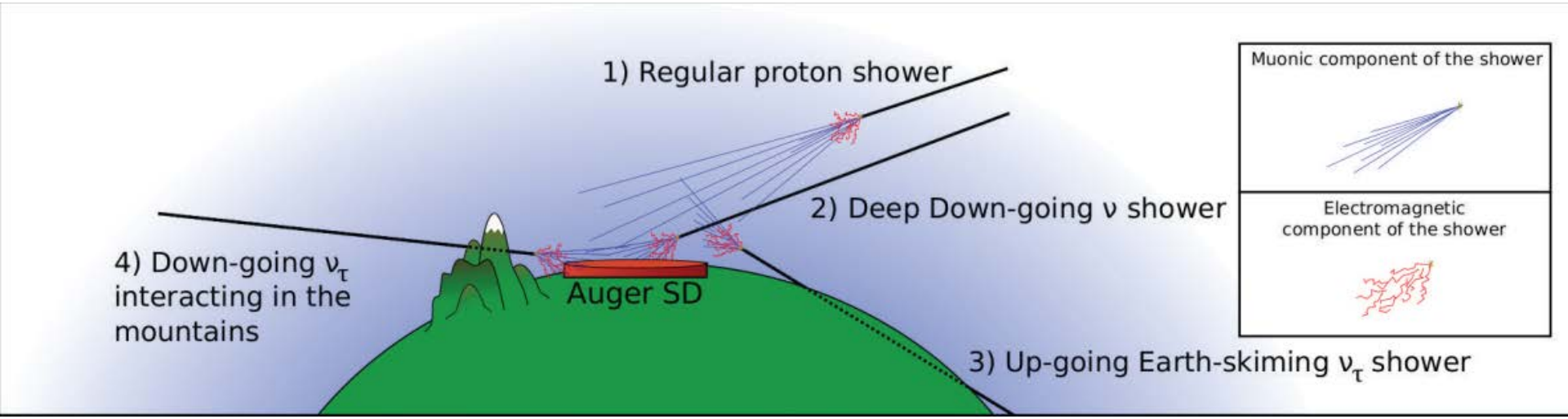
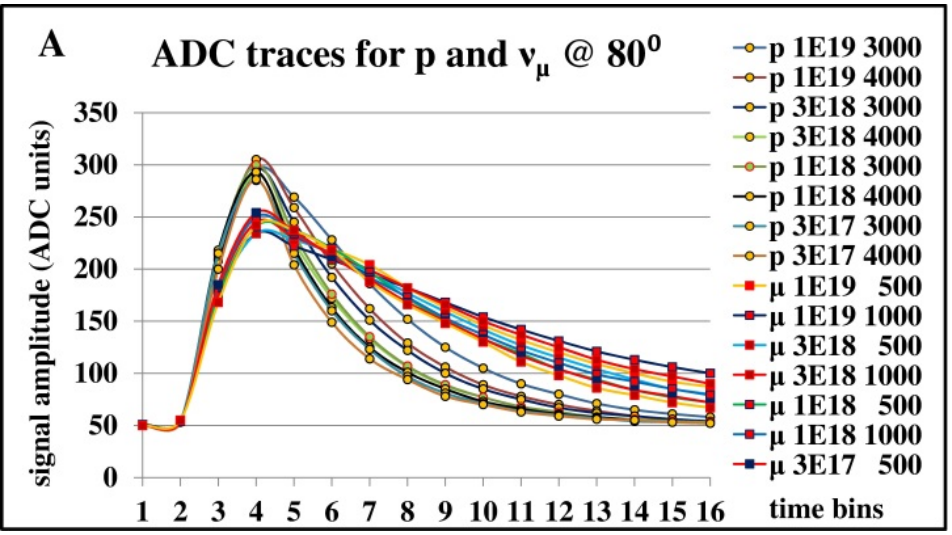


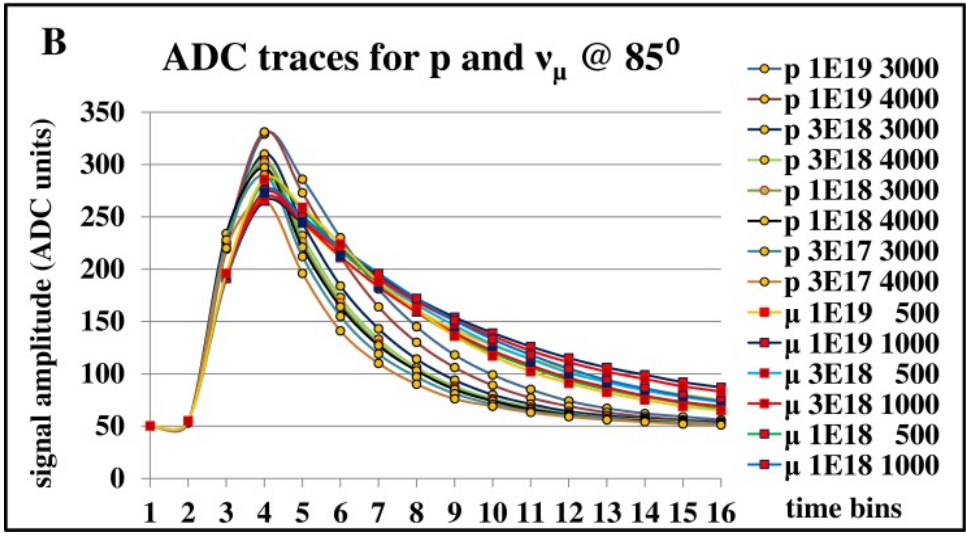
No neutrino candidates

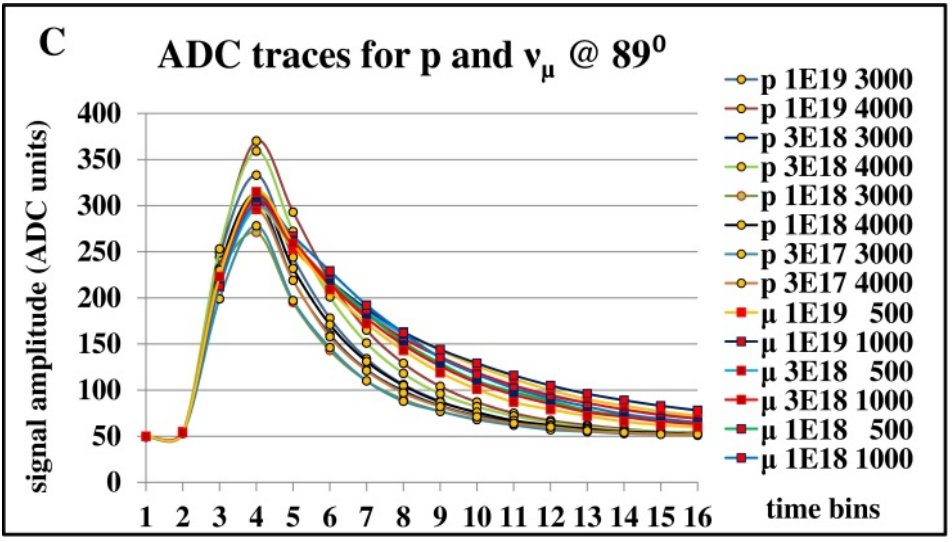
No neutrino candidates have been found, which allows us to place competitive limits to the diffuse flux of UHEνs in the EeV range and above.

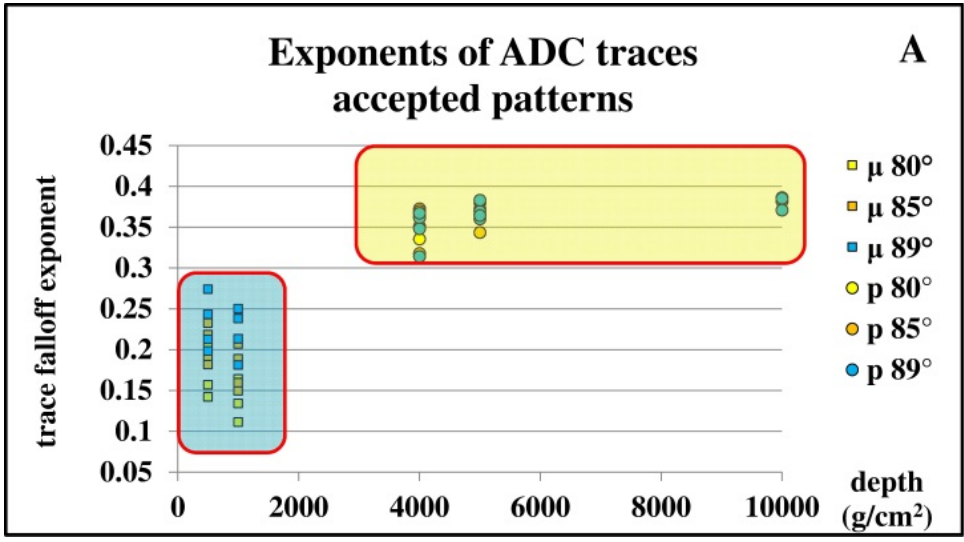


Efficiency

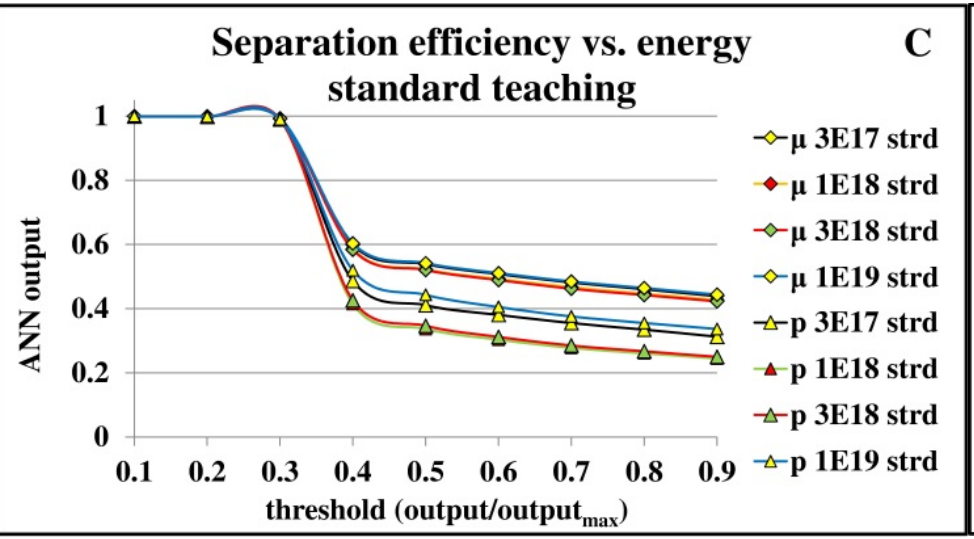

A
ADC traces for p and ν_μ @ 80^0
signal amplitude (ADC units)
time bins
p 1E19 3000
p 1E19 4000
p 3E18 3000
p 3E18 4000
p 1E18 3000
p 1E18 4000
p 3E17 3000
p 3E17 4000
μ 1E19 500
μ 1E19 1000
μ 3E18 500
μ 3E18 1000
μ 1E18 500
μ 1E18 1000
μ 3E17 500

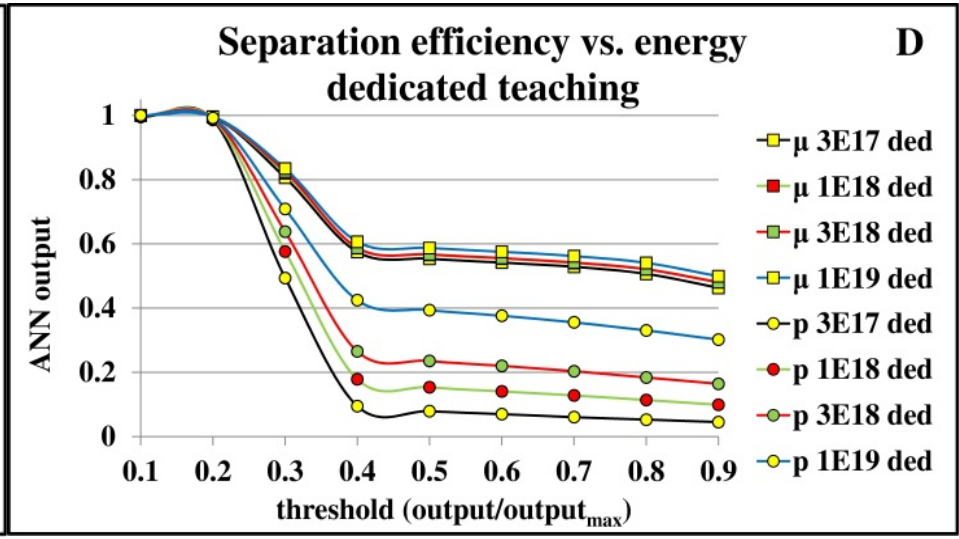

B
ADC traces for p and ν_μ @ 85^0
signal amplitude (ADC units)
time bins
p 1E19 3000
p 1E19 4000
p 3E18 3000
p 3E18 4000
p 1E18 3000
p 1E18 4000
p 3E17 3000
p 3E17 4000
μ 1E19 500
μ 1E19 1000
μ 3E18 500
μ 3E18 1000
μ 1E18 500
μ 1E18 1000

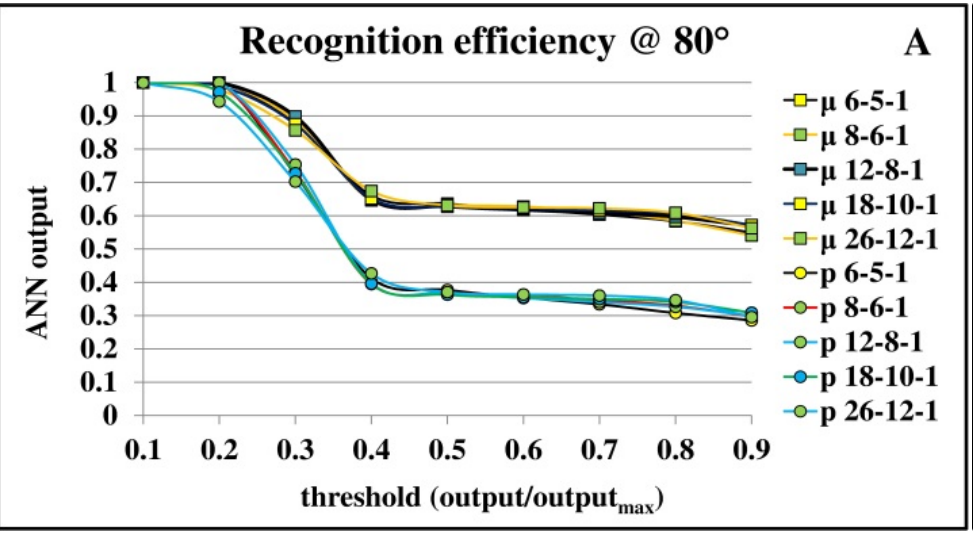

C
ADC traces for p and ν_μ @ 89^0
signal amplitude (ADC units)
time bins
p 1E19 3000
p 1E19 4000
p 3E18 3000
p 3E18 4000
p 1E18 3000
p 1E18 4000
p 3E17 3000
p 3E17 4000
μ 1E19 500
μ 1E19 1000
μ 3E18 500
μ 3E18 1000
μ 1E18 500
μ 1E18 1000

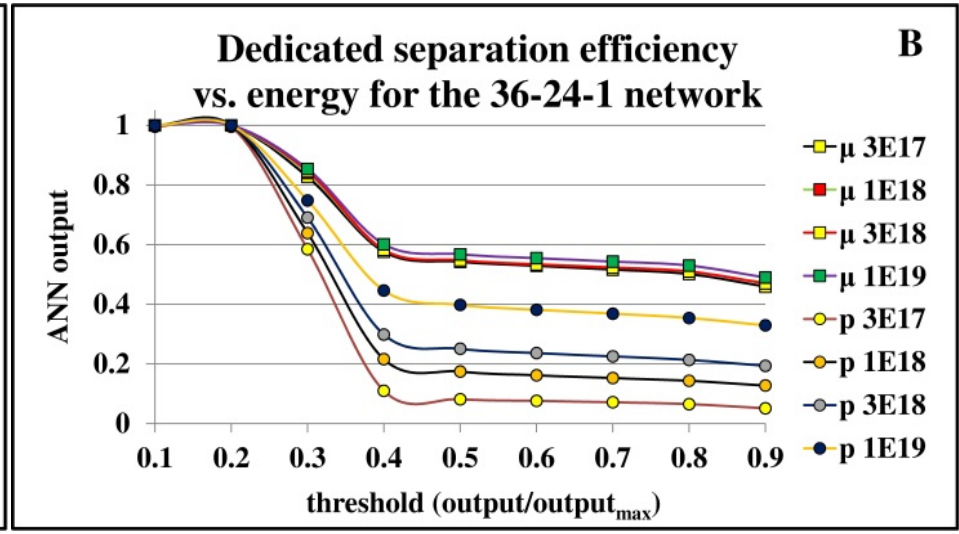

Exponents of ADC traces
accepted patterns
A
trace falloff exponent
depth (g/cm²)
μ 80°
μ 85°
μ 89°
p 80°
p 85°
p 89°

Efficiency


Separation efficiency vs. energy
standard teaching
C
ANN output
threshold (output/output$_{max}$)
μ 3E17 strd
μ 1E18 strd
μ 3E18 strd
μ 1E19 strd
p 3E17 strd
p 1E18 strd
p 3E18 strd
p 1E19 strd


Separation efficiency vs. energy
dedicated teaching
D
ANN output
threshold (output/output$_{max}$)
μ 3E17 ded
μ 1E18 ded
μ 3E18 ded
μ 1E19 ded
p 3E17 ded
p 1E18 ded
p 3E18 ded
p 1E19 ded


Recognition efficiency @ 80°
A
ANN output
threshold (output/output$_{max}$)
μ 6-5-1
μ 8-6-1
μ 12-8-1
μ 18-10-1
μ 26-12-1
p 6-5-1
p 8-6-1
p 12-8-1
p 18-10-1
p 26-12-1


Dedicated separation efficiency
vs. energy for the 36-24-1 network
B
ANN output
threshold (output/output$_{max}$)
μ 3E17
μ 1E18
μ 3E18
μ 1E19
p 3E17
p 1E18
p 3E18
p 1E19

FPGA implementation