How to Build an FPGA-Based DAQ System (This is not a poster title!)

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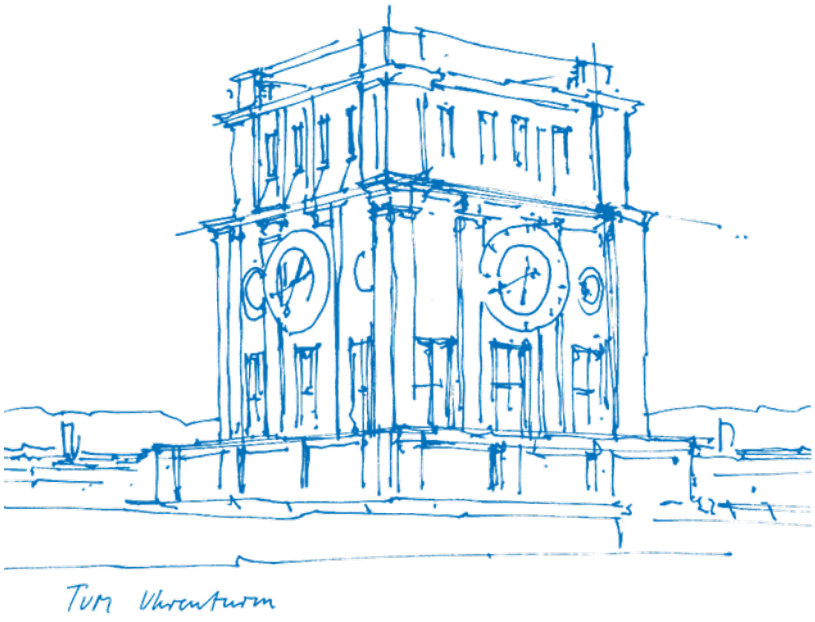


In an ideal world...

1. Take standard cores
2. Adapt to your protocol
3. Interconnect the cores
4. Simulate design
5. Synthesize and use your system

We went the hard way:

We developed several DAQs from scratch

- COMPASS DAQ:
  - **high** number of links
  - **moderate** data rate
- Belle II pixel detector readout:
  - **moderate** number of links
  - **high** data rate
- PENeLOPE DAQ:
  - **low** number of links
  - **low** data rate

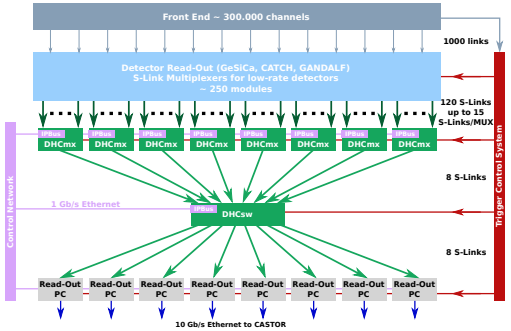


Figure: COMPASS DAQ

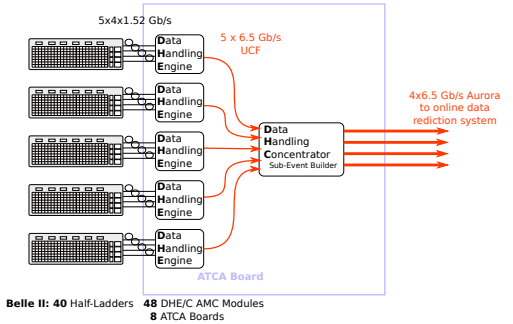


Figure: Belle II pixel detector read-out

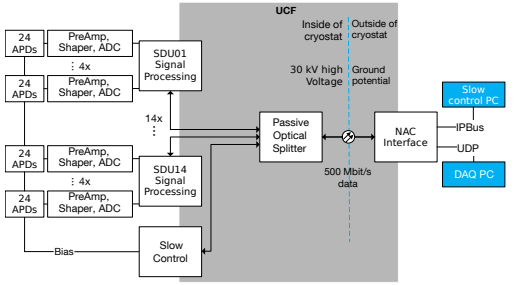
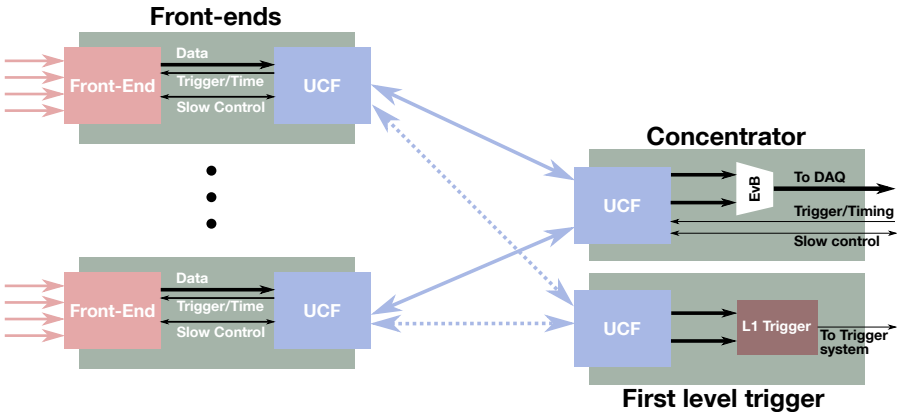


Figure: PENeLOPE DAQ

Intelligent* FPGA Data Acquisition Framework

*Intelligent: self-recoverable and adaptive system

- Main principles
  - self-recovering
  - common hardware design and architecture
  - standard AXI4-Stream interface
- Collection of re-usable IP-cores
  - front-end intefaces
  - communication framework UCF
  - data concentrator / event builder
  - multi-channel FIFO in memory
  - first level trigger logic
  - interface to PC



Poster 143: Intelligent FPGA Data Acquisition Framework