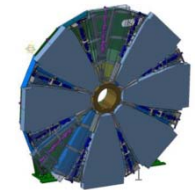


A DAQ Prototype for the ATLAS small-strip Thin Gap Chamber Phase-I Trigger Upgrade

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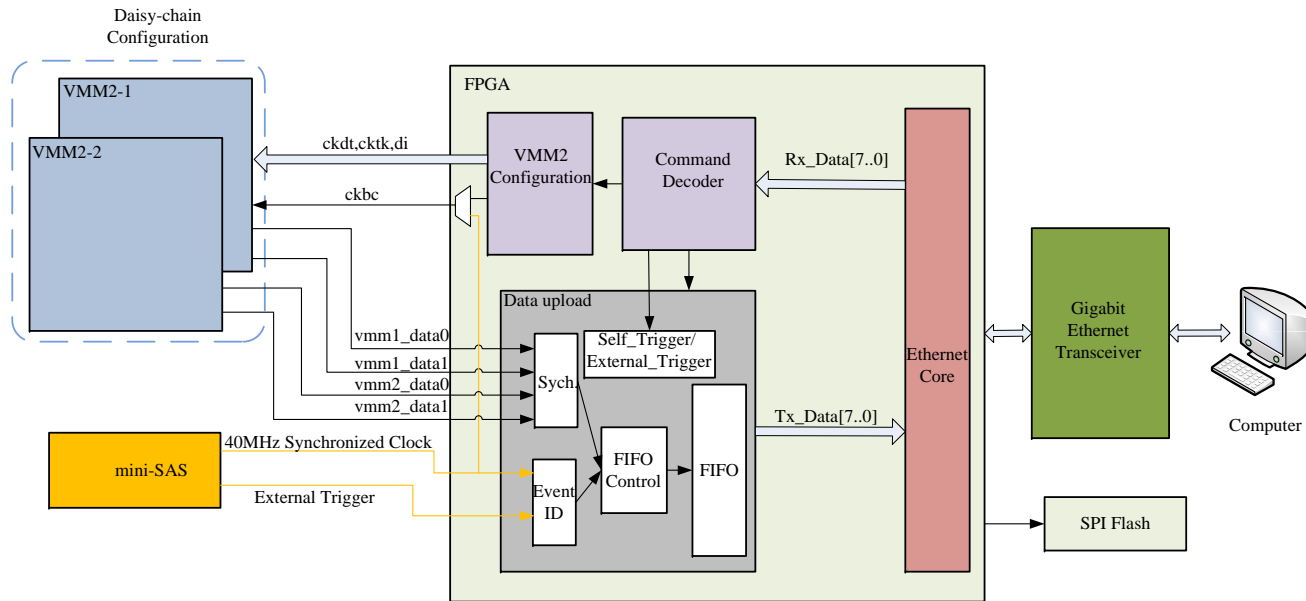


Fig. 1. Schematic block diagram of the DAQ prototype based on the Gigabit Ethernet interface.

The schematic block diagram of the DAQ prototype is illustrated in Fig. 1. The core of the prototype is based on a Kintex-7 FPGA, which is configured by a Serial Peripheral Interface (SPI) flash. Two VMM2s, which are interconnected using a daisy chain, are used to read out the signals from the sTGC detector. The mini-SAS connector is designed to receive the external trigger and the 40MHz synchronized clock. The Ethernet interface is used for connection between the hardware and a computer.

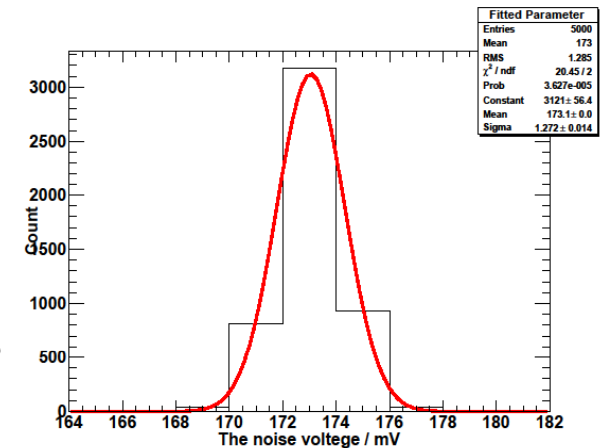


Fig. 2 The output noise of the DAQ prototype shielding the input charge signal.

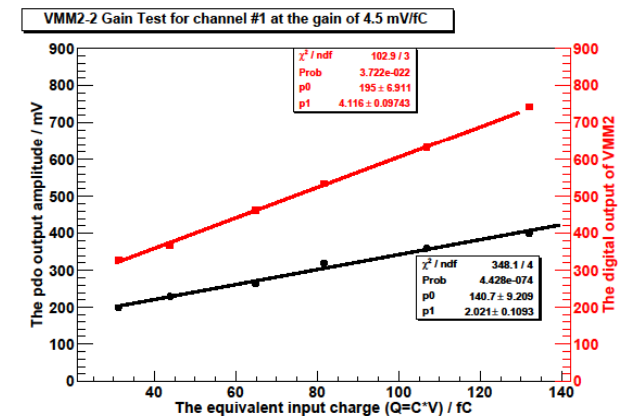


Fig. 3 The linearity test of a channel at the gain of 4.5 mV/fC.

Introduction

Hardware Design

Experimental Results

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1. Introduction

ATLAS [1], [2] is one of four experiments that is located at the Large Hadron Collider (LHC) that being constructed at CERN, Geneva, Switzerland. The ATLAS detector accepts the events from the proton-proton collision at a rate of 40 Mhz. At high luminosity, the performance of the muon tracking chambers, both in terms of efficiency and resolution degrades with the increase of the background rate, especially in the end-cap region. Moreover, the low energy protons, generated in the magnet materials between the inner wheel (SIW) and the end-cap muon detector (EMD), hit the end-cap trigger chambers, thus producing false triggers. In order to cope with these problems, it is proposed by ATLAS collaboration to replace the current muon SIW with the new small wheel (SSW). The thin gap chamber (TGC) technology, developed in 1993 [3], is an important part of the SIW. The smallest TGC (sTGC) in which the strip pitch is much smaller than that of the current ATLAS TGC will be adopted for the upgrade.

In this paper, we will introduce a DAQ prototype based on a high-speed gigabit Ethernet interface. The prototype includes two VMM2 chips, a Xilinx Kintex7 FPGA, and a physical layer Gigabit Ethernet Transceiver (GBT). Additionally, the DAQ implements a high level speeded mini-SAS interface. The Global User Interface (GUI) is written based on C++ application platform, solving the installation and control of the DAQ prototype.

Fig. 1. The case timer of an Ethernet packet without (a) and with (b) the external trigger.

2. Prototype Architecture

The schematic block diagram of the DAQ prototype is illustrated in Fig. 1. The core of the prototype is based on a Kintex7 FPGA, which is configured by a Serial Peripheral Interface (SPI) flash. Two VMM2s, which are interconnected using a daisy chain, are used to read out the signals from the sTGC detector. The mini-SAS connector is designed to receive the external trigger and the 40MHz synchronous clock. The external trigger emerges from a coincidence of the external detector over level in the sTGC detector, used for sTGC efficiency test in the future. The SS11111 Gigabit Ethernet PHY driver is a physical layer device for 100BASE-T, 100BASE-TX, and 10GBASE-T application. In our design, the GBT is configured as the Gigabit Media Independent Interface (GMII). The SFP port is used for connection between the hardware and a computer.

The block diagram of the signal flow in the FPGA is shown in the middle of Fig. 1. The Ethernet core, generated via the Core Generator of the Xilinx ISE software, is embedded in the FPGA. The Ethernet interface is implemented in Media Access Control (MAC) layer, which is a sub-layer of the data link layer. The Ethernet interface accepts the user-defined commands and VMM2 configuration bits. The different commands can be derived from the command decoder. At initialization, all the SFPs and status registers are read. Then, a VMM2 configuration command arrives. The VMM2 configuration module is implemented via a state machine. After the configuration, the VMM2 data (data0, data1) will output when one of VMM2 channels perceives a change signal. Once sending a user-defined data upload command, events from two VMM2s are stored in an internal FIFO. Then these events are sent back to a computer.

Fig. 2. Schematic block diagram of DAQ prototype based on the Gigabit Ethernet interface.

3. Data Format

The data format of an Ethernet packet is illustrated in Fig. 2. The data is transferred via an Ethernet interface. For a scenario without an external trigger shown in Fig. 2(a), each Ethernet packet has 75 events. Each event from VMM2 contains a total of 35 bits, shifted out in parallel to the sTGC data output using 19 clock edges. The total number of an Ethernet packet are 1425 bytes, including a 6-byte destination MAC address, a 6-byte source MAC address, a 2-byte user-defined token and 1422 bytes data from VMM2. For a case with an external trigger, however, an event identification (EI) with 2 bytes is added after every event, which is generated via an internal counter driven by the external trigger signal. The total number of an Ethernet packet for this case are 1422 bytes, illustrated in Fig. 2(b). The 2-byte token means a user-defined command token as value is higher than 1500. It specifies an Ethernet packet length when lower than 1500.

4. Experimental Results

The noise test is carried out after the VMM2 configuration. The signal from the monitor (MO) pin of the VMM2 is captured by a high-bandwidth Tektronix oscilloscope. Fig. 3 shows the output noise of the DAQ prototype. The noise voltage with a Gaussian distribution is listed in an histogram. The root mean square (RMS) is less than 2 mV_{rms}. The noise is mainly contributed by the thermal noise of components, the 1/f noise which results from the parasitic capacitance in the PCB, and the high-frequency noise in digital components such as FPGA. The mean value is 172 mV generated by a stable bandpass referenced baseline.

The VMM2 chip consists of 64 front-end channels and digital processing circuit [6]. In our VMM2 configuration, the continuous mode is used. In this mode, the peak and the time window convert the voltages into currents that are related to the 10-bit ADC and 5-bit ADC, respectively. The 10-bit ADC processes a high resolution ADC conversion for the peak value. The 5-bit ADC is applied to convert the peak timing, which is measured using a Time-Amplitude Conversion (TAC). The TAC stop signal occurs at the next clock period of a linear 12-bit Graycode counter incremented using an external Surch Clock (SC). Each channel is calibrated by a pulser and a 1.2 pF test capacitor. The output is adjustable with a global 1-bit DAC, triggered with an external test pulse clock. The GEM value is sent to the VMM2 with the configuration bit sequence. Each channel has adjustable gain range, offering the analog dynamic ranges. For a given DAC value of the pulser and a given channel gain, we can obtain a histogram of the peak value. Slipping up the DAC value, a linearly test of the VMM2 channel is performed. The linearly test results are illustrated in Fig. 4. The equivalent input Charge (EIC) for the channel is described as $ChEV(1, DAC)$. The slope of the fitted line means the actual channel gain we obtain, slightly less than the nominal value.

Fig. 3. The output noise of the DAQ prototype. Fig. 4. Linearly test of channel gain of 65 mV/C.

5. Conclusions

In this paper, a DAQ prototype based on a Gigabit Ethernet interface has been built for the ATLAS smallest Thin Gap Chamber (TGC) Phase-I upgrade. The DAQ prototype consists of VMM2, FPGA and Gigabit Ethernet Transceiver. The VMM2 performance is discussed in detail. In the early upgrade, the DAQ prototype will be used for the sTGC performance test.

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